Appendix 1 – Acronyms and Definitions

Acronyms

ARC	Ames Research Center
ATE	Automated Test Equipment
AV&V	Automated Verification and Validation
AWL	Automated Wire List
BRSS	Boeing Reusable Space Systems
BOM	Build of Materials
CBM	Condition-Based Maintenance
CDF&TDS	Circuit Design, Fabrication and Test Data System (a database)
COTS	Commercial Off-the-Shelf
DFS	Design for Safety Initiative
DWV	Dielectric Withstanding Voltage
FMEA	Failure Mode and Effects Analysis
JSC	Johnson Space Center
KSC	Kennedy Space Center
MTBF	Mean Time Between Failures
OMM:	Orbiter Major Modification
OMI	Orbiter Maintenance Instruction
OMDP	Orbiter Maintenance Down Period
OMRSD	Orbiter Maintenance Requirement Specification Document
OPF	Orbiter Processing Facility
MIR	Microwave Impulse Radar
PR	Problem Report

PRACA	Problem Reporting and Corrective Action (a database)
SCAD	Smart Computer Aided Design
SCAN	Shuttle Connector Analysis Network (a database)
SIAT	Space Shuttle Independent Assessment Team
SRB	Shuttle Rocket Booster
SWR	Standing Wave Ratio
SWReflectometry	Standing Wave Reflectometry
SSPO	Space Shuttle Program Office
TDR	Time Domain Reflectometry
TFOMS	Testability Figures of Merit Summary
TRL	Technology Readiness Level
WAD	Work Authorization Document
WIRe	Wire Integrity Research

Definitions

Automated Test Equipment

Automated equipment for testing, which ranges from simple switching capability with continuity and isolation checks to equipment capable of identifying the type and location of wiring defects.

Criticality

A relative measure of the consequences of a failure mode and its frequency of occurrences.

Criticality Analysis

A procedure by which each potential failure mode is ranked according to the combined influence of severity and probability of occurrence.

Defect

A wiring anomaly that has not yet progressed to being a fault.

De-mating

The process of separating the male and female parts of a connector.

Dialectric Withstanding Voltage

A test using high voltage to determine that an insulating system meets certain minimum requirements.

Failure Cause

The physical or chemical processes, design defects, quality defects, part misapplication, or other processes which are the basic reason for failure or which initiate the physical process by which deterioration proceeds to failure.

Failure Effect

The consequence(s) a failure mode has on the operation, function, or status of an item. Failure effects are classified as local effect, next higher level, and end effect.

Failure Mode

The manner by which a failure is observed. Generally describes the way the failure occurs and its impact on equipment operation.

Failure Mode and Effects Analysis (FMEA)

A procedure by which each potential failure mode in a system is analyzed to determine the results or effects thereof on the system and to classify each potential failure mode according to its severity.

Fault

A wiring anomaly resulting in either a short or an open circuit.

Hazard

Act or condition posing threat of harm.

Hazard Analysis

Line-item listing of all system hazards, with subjective evaluations of severity, probability, and risk for each.

High Pot (various spellings)

Short for high potential , or DWV testing

Invasive

Requiring de-mating of one or more connectors

Intrusive

See Invasive

Mating

Joining the male and female parts of a connector

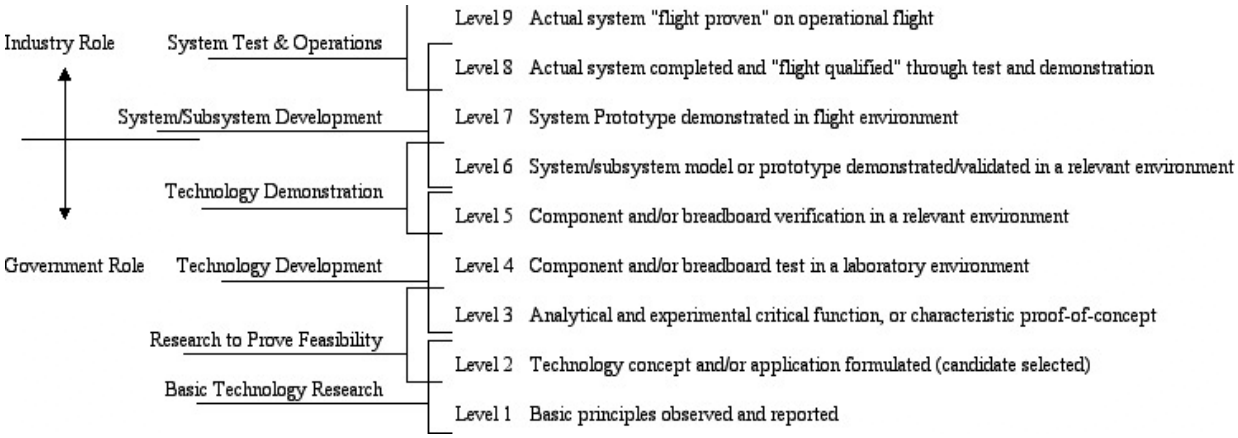
Risk

An expression of the combined severity and probability of loss. The long-term rate of loss, i.e. the loss rate value.

Severity

The consequences of a failure mode. Severity considers the worst potential consequence of a failure, determined by the degree of injury, property damage, or system damage that could ultimately occur.

Technology Readiness Level



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Appendix 2 – Space Shuttle Program Priority Requirements for Wiring

Introduction

During discussions between the WIRe Pilot Study team and the Space Shuttle Program Office (SSPO), it became clear that there were additional areas relevant to Orbiter wire architecture and processing that were beyond what was being covered in the WIRe Pilot Study. SSPO, in conjunction with Kennedy Space Center (KSC) and Boeing Reusable Space Systems (BRSS), developed a list of the most highly desired wiring related tools or technologies for Orbiter operations from their perspective. Due to limited resources and the short duration of the Pilot Study, the WIRe team was not able to prototype or implement the tools. However, because of the significance of the impact these tools would potentially have for Orbiter operations, the WIRe team sought to further define and document requirements for these tools. Listed below is the original tool or technology specified by the SSPO and the WIRe team s assessment of its requirements and importance for Orbiter wiring.

• Shuttle Connector Analysis Network (SCAN) Electronic Wirelist available on the WEB:

SCAN system is a UNIX-Oracle platform: Development of a Web based wire list interface to the UNIX-Oracle system could quickly assist system engineers in the analysis of as built retest requirements.

Assessment:

The requirements for the tools are, for the most part, obvious. SCAN is currently implemented in a client-server-based system, which can only be accessed from client terminals, or through a laborious log-on interface and extremely slow access through a remote terminal. This is inconvenient at best and certainly impedes the use of the tool at Palmdale. Development of a web-based tool would be relatively straightforward, and for configuration control purposes, could either be read-only or password controlled. No technology development is required for this effort and the return on investment is expected to be high. The WIRe team agrees that this recommendation should be implemented.

• Automated Disposition of Repair and Modification of Wire Harnesses

Wire configuration, parts list, configuration currently resides in automated wire list that could be interfaced to standard repair procedures and modifications to ensure flawless dispositions.

Example: Connector removal and replacement, Standard Repair Procedures

Assessment:

Orbiter sub-system engineers reportedly spend about two-thirds of their time developing repair procedures for cable harnesses, in which the procedures contain much duplicated procedural information. The requirement would entail appropriate parsing of connector repair procedure steps linking to the cable harness database, which could either be CDF&TDS or SCAN. If this tool were to be developed, it would be an incremental step to also generate the test procedure that needs to be executed following each repair or modification. This feature would come out of the test management software envisioned by the WIRe team.

• Shuttle Connector Analysis Network (SCAN) Electronic Integrated Schematics:

A graphical schematic interface to connectors and functionality would assist system engineers in the validation analysis of circuitry

Assessment:

This functionality would be of tremendous benefit to Orbiter engineers and technicians. It would simplify and reduce the time involved in tracing signal and wire paths through a subsystem, and as such, reduce the risk of error. It would also provide a better method for determining test configurations and allow engineers to better determine test coverage. This is effectively what the WIRe team explored through the Qualtech TEAMS tool (see Appendix 9), although including the functional information was beyond the scope of the WIRe study. Specific requirements need to be developed to determine the exact fidelity of the tool that would provide the functionality the engineers need. Another issue is that options for implementation need to be assessed. SCAN could be augmented to provide this interface; the design could be ported over to WCAD, a BRSS customization effort (see Appendix 7) and it could be used; a tool could be custom-developed in-house; or if the Digitized Vehicle becomes a reality, the capabilities are likely to already be built in. A tool such as this would clearly provide benefit to the Shuttle Program, but the investment required to implement a tool such as this needs a requirements development phase. A trade-off assessment to fully develop the requirements for this tool and determine the most cost effective plan of implementation should be done.

• Criticality Analysis of Circuitry (Risk Assessment Tool)

Wiring criticality is typically analyzed one circuit at a time. A quick reference tool for identification of criticality may lead to enhancements to testing.

This task is essentially Space Shuttle Independent Assessment Team (SIAT) action #30 that Boeing believes has great merit. Boeing currently maintains wiring redundancy information in paper folders and binders. As one would expect, this storage media makes it difficult to perform searches or to incorporate periodic updates.

SIAT Short Term Recommendation #30: A database that continually evaluates wiring system redundancy for the current design, modifications, repairs, and upgrades should be maintained. System safety should evaluate the overall risk created by wiring failures.

Assessment:

Over the course of investigating automated testing for Orbiter, testing wires of high criticality was considered early in the study. The WIRe team found, however, that criticality was linked to systems and system functions and not wiring. A tool to analyze criticality based not only on system functions, but also considering the wire itself, the routing, and proximity to redundant systems is highly desirable for the Orbiter. At the Government Agency Working Group on Wire, staff from the Naval Air Command also identified the need to include physical routing into risk assessments.

Tools could be developed to aid these criticality assessments, but they would be based on having the design in a state-of-the-art set of CAD tools, along the lines of what the Digitized Shuttle pilot study is investigating. It is possible to portion and classify portions of geometries, such as cable trays, and then have an application program interface (API) developed to extract the cable harness versus routing versus criticality level and evaluate the redundancy. Once a Digitized Shuttle was in place with the appropriate parameters entered in the design, this would be a relatively straightforward activity. Unfortunately, the current state is that the vast majority of cable harnesses are not currently modeled in a state-of-the-art CAD tool, and this would be a significant endeavor.

• Develop Automated Wire Integrity Diagnostic Tool

Not unexpectedly, there has been a great deal of emphasis placed on this capability since the STS-93 AC1 anomaly. Boeing is currently fabricating several wire harnesses with known defects for submittal to select vendors who have advertised some form of fault isolation capability. Each harness will be encapsulated to maintain the integrity of these blind tests. Boeing and NASA-Ames may consider collaborating with the vendor that demonstrates having the most promising technology.

Assessment

The WIRe team has called this capability defect detection , and the team s assessment of current technologies and technology enhancements required is contained in Section 3, of this report. The WIRe team agrees that this capability should be developed and expended a significant portion of its effort in this area. This is a major portion of the recommended follow-on work.

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Appendix 3 – Characterization of Shuttle Wiring and Tools

Characterization of Shuttle Wire

Shuttle wiring is complex, aging, and subject to wear. It is difficult to detect imminent wire failures and localize wire faults. Because of decreased confidence in Shuttle wire integrity, manual wire inspection labor has increased to high levels. This task can only be accomplished during prolonged Shuttle down time. Technology that either helps identify imminent failure, or localizes a fault once it occurs, would save significant cost in time and labor, perhaps offsetting the cost of implementation. The cost of deploying technology that detects immanent failure is justified by the increase in crew and vehicle safety.

Shuttle Wire Features

Personnel at BRSS, Huntington Beach Engineering ran a couple of quick queries on the CDF&TDS database for Orbiter 102 flight 27 (which represents the configuration after Columbia s major modification currently underway in Palmdale). The count listed below excludes payload and mission equipment harnesses.

Number of components, listed in order of frequency, excludes accessory components such as backshells and adapters:

SP	splice	14,600
P	plug	5,137
J	jack	2,231
XF	fuse holder	1,184
S	switch	1,085
TB	term board	999
K	relay	730
MT	transducer	651
E	ground stud	549
CB	circuit breaker	525
(all others)		3,668
	TOTAL	30,834
	TOTAL including accessories	39,184
The count of single conductor wires and cables:		103,870

Actual wire record counts in the CDF&TDS database are higher, because cables are represented by multiple wire records and spare pins and bus bars are also represented by wire records. Single

conductor and cable record count, excluding shield records: 146,189, including shield records: 163,792. Total records, including spare pins: 288,813.

Wire Criticality Types

There has never been an actual criticality analysis conducted specifically on wire harness or individual wire runs. During routine communications, when wire runs are referred to as having certain criticality levels, what is being referred to is the criticality of the signal or function handled by that wire. A risk assessment of the actual wire may not yield the same criticality assessment, partly because the relative probabilities for failure of individual wires are not taken into account, in existing analyses. To really assess criticality on a wire-by-wire basis, a new FMEA oriented toward wire would need to be conducted. This would be expensive and time consuming. Because the wire criticality level is not very meaningful, it would not be useful to prioritize wire testing by this criterion.

BRSS is in the process of reviewing an analysis, originally performed in the early 1990s, of wire routing violations. That original study is in contained in 14 binders. Their review may result in a recommendation to re-rout 127 wires for better separation of redundant systems. Analyses like these are very laborious. To create a true wire-oriented FMEA, and to keep these risk analyses up to date as configuration changes occur to the Orbiter or Payload, is prohibited by cost and the effort required to comb through records and analyze severities and functional criticality.

A system interconnectivity model can be easily created in a commercially available test analysis package based on data imported directly from the CDF&TDS and SCAN configuration databases. Computer assisted analysis can make it economically and practically feasible to periodically update wire risk assessments. Operations managers and QA engineers could use the latest data for wire analysis and overall vehicle risk assessment.

Testpoint Accessibility

Useful forms of Automated Verification and Validation (AV&V) and wire integrity testing identified by the WIRe team usually involves applying a test source at one or both ends of a wire. (Impedance spectroscopy and other methods can make use of impedance measurements between two wires, or between a wire and ground plane, at one connector at one end of a harness.) According to Orbiter maintenance requirements, de-mating a connector pair requires a functional retest of all systems having signals that pass through the connection. Because many different signals can pass through a given connector, the impact of having to do a functional test after a single connector de-mate can have a negative ripple effect on Orbiter processing flow.

An enhanced wire test program, in which wires are periodically tested for integrity for example, should make every effort to take advantage of tests of opportunity , that is, conducting integrity tests for wire runs in which connectors are already de-mated for maintenance, reconfiguration, or payload integration purposes. A test management program would track, and perhaps recommend which de-mated harness to test, over the course of a number of Orbiter flows. The goal would be to maximize wire test coverage, while minimizing impact to Orbiter flow for functional retest.

Some harnesses are routinely de-mated each Orbiter flow. Examples include SRB (but of course, our study focuses on Orbiter), MPS, pryo, and T Zero connectors. Other harness are very often de-mated each flow, such as the Payload Station interface connectors. Time permitting, it might be advisable to apply wire integrity test equipment to these connectors during pre-flight workflow at KSC.

Unfortunately, the entire list of routinely de-mated connectors makes up a small minority of the total number of connectors in the Orbiter. CDF&TDS records indicate there are about 5,000 connectors on OV-102 in its basic configuration (no payload) during the present OMDP at Palmdale. Personnel at KSC ran a SCAN database check of connectors de-mated there, to try to identify how many are commonly de-mated between flows. They looked at a two-month period between January 21 and March 31, 2000, during which time OV-103 and OV-105 were in the OPF, and listed all connectors de-mated in each. They then did a comparison of the two lists, to find which and how many connectors were de-mated in common between the two Orbiters. The results show that out of the approximately 5,000 total connectors in each Orbiter, a total of 720 were de-mated between the two. But only 121 of those were common between them that is, about 7.2 percent of all connectors are de-mated, with only about 2.4 percent in common. So we can say that less than 3 percent of the total number of Orbiter connectors are routinely de-mated from flight-to-flight.

Individual harnesses are daisy chained to a degree, mated together at bulkheads, etc. The percent of all harnesses or maybe more appropriately, what total length of wire in feet can be tested by accessing these 2 to 7 percent of connectors, is not readily known, because a detailed analysis of the SCAN (and CDF&TDS, for lengths) database would be required.

A computerized tool, based on a model of harness interconnection data that included SCAN connector de-mate status could be created to investigate wire test coverage obtained by taking advantage of routinely de-mated connectors. The tool should generate work authorization documents that schedule tests based on known de-mate schedules. SCAN could be adapted to do this, or a commercial-off-the-shelf test management package could be used.

Characterization of Shuttle Wire Failure Mechanisms

The automated and manual tests, together, must detect every wire fault.

Test techniques that detect and locate faults can be evaluated for performance quality for each fault type or the condition of the wire within which the fault occurred. Test techniques that detect flaws or imminent failures can be evaluated for relative success for each type of flaw likely to be encountered in known Shuttle wire failure modes. The known Shuttle wire failure modes will be used for characterizing the relative success for detection by each of the respective test techniques.

Shuttle Program Tools for Wiring

The two Shuttle databases for wire configuration are CDF&TDS and SCAN. Their relationship to each other is shown in Figure 8.

CDF&TDS

CDF&TDS stands for Circuit Design, Fabrication and Test Data System. All Shuttle wire harness design information is contained in this database.

CDF&TDS supports the design, fabrication, and testing of wire harnesses. Shuttle engineering groups enter new harness design, and harness modifications, into the database using the design entry forms. CDF&TDS has libraries of wire harness part numbers, such as connectors, contacts, cable lacing, etc. The database will check new designs and modifications against a built-in design rules checker. CDF&TDS reports generate Engineering Orders (EO) documenting the design changes, and releasable assembly instructions, including manufacturing and inspection notes, in the form of an Automated Wire List (AWL). The EO package sent to Manufacturing will include the AWL, and bill of materials (including wire length estimates), list of required tools, and installation instructions, all generated from CDF&TDS forms. QA will use the AWL as the basis for inspection, recorded in the manufacturing Work Authorization Document (WAD).

Once a new harness is assembled, or a modification is completed in the Orbiter, an Automated Verification and Validation test (AV&V) is performed. In Palmdale, DIT-MCO programmable ATE equipment is used. Test engineers use the CDF&TDS AWL wire data to generate new ATE test programs (or retrieve and modify existing programs on file). In Palmdale, test engineers are experimenting with a DIT-MCO utility, running on a NT machine, which allows them to query the CDF&TDS database and import wire list data into an automatic DIT-MCO test program generator.

The CDF&TDS database is built on Oracle and hosted on a UNIX workstation. System administrators can grant users access to the database in various levels appropriate for the user s authority read only, EO processing, or data-entry.

The CDF&TDS database has been in use since the very beginning of the Shuttle Program. It is under rigorous configuration control, and so has a great deal of integrity as the authoritative source of Shuttle wire harness design configuration. CDF&TDS only contains individual harness design configuration; it does not contain real-time data about the interconnection of harnesses, as the SCAN database does. CDF&TDS connector and circuit information part number, reference designator, wire number, signal name are exported from CDF&TDS to SCAN. SCAN uses this data in a variety of ways, such as for tracing copper path .

SCAN

The Shuttle Connector Analysis Network (SCAN) is a Kennedy Space Center (KSC) software tool which tracks actual mate/de-mate and connector retest verification for each flight and provides accountability for pin-to-pin functional retest of re-mated connectors.

Inputs to SCAN are:

- CDF&TDS wire harness database
- CDF&TDS General Notes Dictionary

- Mission Equipment, Shuttle Launch Site Installation (MECSLSI)
- Crew Compartment Configuration Drawing (CCCD)
- Electrical Change Notice (ECN) defining the 807 patch panel configuration
- Vehicle Diagram (VD)
- MECSLSI LRU Excel file

The primary purpose of SCAN is to insure the integrity of re-mated connectors and their signal paths prior to each launch. Each time a connector pair is de-mated for any reason, SCAN will flag the appropriate functional tests Orbiter Maintenance Requirement Specification Document (OMRSD) necessary to verify correct operation of every signal carried by the connector, upon re-mate.

SCAN was developed at KSC direction in 1989. The database is hosted on a network of UNIX computers. Users must apply for a login account to the system, and their use is restricted to the Orbiter or GSE to which they are granted access. Users log in via Xterminals, to UNIX login accounts, within TCP/IP domains approved by the administrators.

Engineers at BRSS, Huntington Beach, will document the exact as-designed configuration of every Orbiter or payload harness connector mate/de-mate status, prior to launch for each Shuttle flight. Engineers and technicians will document the mate/de-mate status of all connectors during launch flows, configuration changes or maintenance activities in the Orbiter Processing Facilities at KSC, or at Boeing Palmdale facility.

Because the SCAN database contains information about how harnesses are interconnected within the Shuttle, and the up-to-date status of their de-mated state, it could be used as a basis for selecting appropriate connectors for wire test point access. It would be possible to export the SCAN data to a wire interconnectivity model. Test Management Software Tools would use this model to optimize test point selection, tracking wire test coverage, maximizing the number, and lengths, of wire runs to be tested. The Test Management Software Tools would be set up to take advantage of connectors nominally scheduled for de-mate (during launch flow, or for other purposes).

During the WIRe study, the QSI TEAMS tool was evaluated for just this purpose, setting it up to import SCAN connectivity data for the Orbiter MEC1. Failure modes and test point selection were investigated as part of the TEAMS demonstration. This is discussed in detail in Section 3, Evaluation of COTS Test Management Tools, and in Appendix 9, Qualtech TEAMS Model for Test Management.

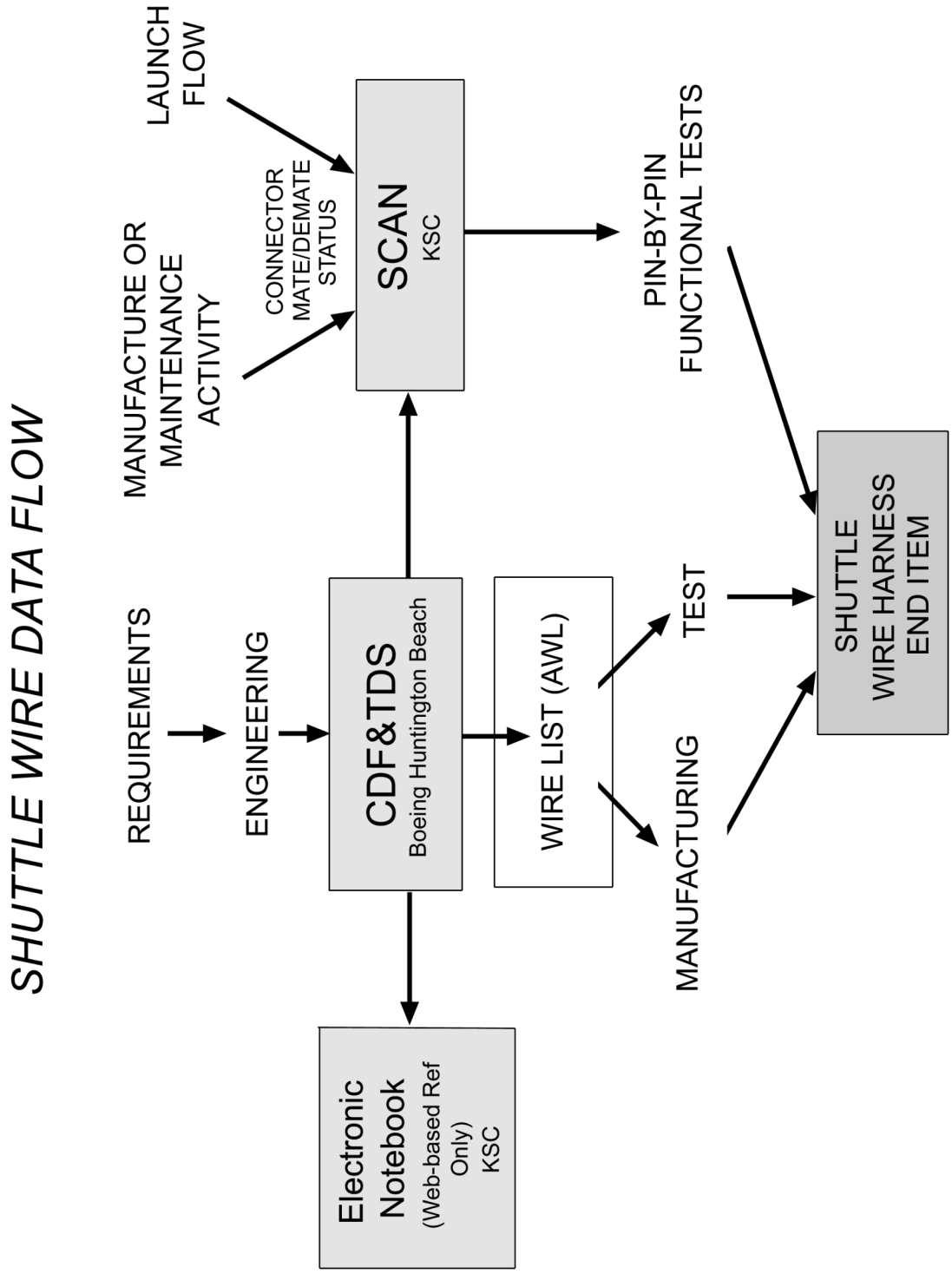

Figure 8. Data Flow Between SCAN, CDF&TDS, Electronic Notebook, and Wire Harnesses.

Shuttle Work Flow

Shuttle turnaround time is tight at Cape Canaveral and at the maintenance facility. Manual wire test techniques are nearly prohibitive due to maintenance schedule impact. Automated test techniques could relieve the problem, but to be practical, must also fit within work schedule constraints.

KSC

The Shuttle launch process flow at Kennedy Space Center is both a tight and complex schedule. It requires a great deal of planning across the line of NASA Flow Director, USA Flow Manager and Vehicle Ops Chiefs to prepare a Process Support Plan (PSP). Accelerated flight rates, to support International Space Station, dictates that the process flow be kept streamlined as possible. KSC may presently be transitioning from using their Ground Processing Scheduling System (GPSS) software tool, to using PeopleSoft, to aid them in managing the real-time flow schedule.

There is no typical launch flow cable reconfiguration set. Although its true that the Shuttle Main Engines, Solid Rocket Boosters, pyrotechnic devices, and other components are removed and replaced each flight, and that Payload Station connectors and other payload connectors are routinely de-mated and reconfigured, the proportion of connectors de-mated each flight is small. Of those, the proportion routinely de-mated each flight is much smaller.

An analysis of one month of flow connector de-mates for OV 103 vs. OV105 was performed to track the number of de-mates common between them that is, the number of routine de-mates from flow-to-flow. This analysis indicates about 700 connectors de-mated on both vehicles, or 350 per vehicle. Of those, only about 129 connectors are de-mated in common between both Orbiters. There are approximately 5,000 connectors on the Orbiter in all.

Even if it were possible to automatically test every harness with a de-mated connector in the course of the launch process flow, it would only be a small subset of the total harnesses in the Orbiter.

De-mating a connector just for wire testing is very costly in terms of schedule time. Every connector de-mated requires a complete functional test of every function on every circuit carried through the connector de-mated. These tests may involve dozens of systems, perturbing the nominally scheduled functional test activities for each system. While testing pyrotechnics, electrical silence must be maintained, so no other test activities can be conducted concurrently. The ripple effect of the schedule impact of de-mating a connector just for wire testing would be difficult or impossible to contain at KSC, even if using automated schedule optimization tools.

Palmdale

Palmdale has time available to unplug connectors to accomplish a full-up wire integrity test. And it could save them time from doing a full-vehicle visual inspection, if they intend to do to the fleet anything like what they did to OV-102.

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Appendix 4 – Wire Integrity Assessment Technologies

Current State-of-the-Art

The WIRe team evaluated a variety of wire integrity assessment equipment. Descriptions of their capabilities are given below.

Vendor / Feature	Continuity	Isolation	DWV	Capacitance	SWR	TDR	Impedance Spectroscopy	Fluid Encapsulation	Automated Testing (viaSwitching Relays)
DIT-MCO	X	X	X	X					X
Eclypse	X	X	X	X	X				X
Cirrus	X	X	X	X					X
Weetech	X	X	X						X
CableTest	X	X	X						X
CM Technologies			X	X		X	X		
Lectromec								X	

Table 1. Currently Available Test Capabilities.

Wire Inspection Technologies												
Technology	Owner	Probability of Near-Term Success (1-10)	Applicability		Damaged Insulation	Damaged Conductor	Damaged Shields	Corroded Connector	Location	Requirements	Limitations
			Shorts	Opens						(Note: In some cases the second end is needed for isolation)	
Visual Inspection		10			X	X	X	*	X	Visual Accessibility	
Visual Inspection, enhanced		10			X	X	X	*	X	Visual Accessibility	
TDR		9	X	X					X	Single end	Sometimes difficulty in locating?
TDR		6				X	X		X	Single end	
TDR		3			X				X	Single end	
SWR	NASA / Eclypse	10	X	X					X	Single end	
SWR	NASA / Boeing	5			X				X	Single end	
Impedance Spectroscopy		7	X	X	X	X				Both ends	
T-wave			X	X	X	X	X		X	Both ends	
Microwave Impulse Radar	LLNL	5		X		X	X		X	Single end	
Continuity		10		X						Both ends	
Isolation		10	X							Both ends	
DWV		8			X					Minimal distance from ground	Minimal distance from ground

Technology	Owner	Probability of Near-Term Success (1-10)	Applicability: Shorts	Applicability: Opens	Damaged Insulation	Damaged Conductor	Damaged Shields	Corroded Connector	Location	Requirements	Limitations
Ionized Gas DWV					X				*	Single end	Fully breached insulation only, min. dist. from ground
Inert Gas DWV	(Cirris)	6			X				*	Single end	Fully breached insulation only, min. dist. from ground
Ultrasonic Guided Wave	LLNL	4				X			X	Single end	30-50' max length
Infrared, magnification		8			X	X	X	*	X	Visual Accessibility	
Thermal Inertia Imaging	LLNL	7			X	X	X	*	X		
Capacitance Measurements		9		X					X	Both ends	
Capacitance Measurements		5			X						
Resistance Measurements		9	X						X		
Conductive Fluid Scanning	Cirris, Lectromec	9			X				X	Nearby ground surface	Break all the way through the insulation
Induced Current Impedance	USAF					X	X	X	X	Physical access, used for conductor corrosion	
Radiographic Imaging		1									
Radio Frequency Techniques						X	X		X		
										(Note: In some cases the second end is needed for isolation)	

Table 2. Wire assessment capabilities of various techniques. * No significant laboratory validation has been performed on this technique.

Dielectric Withstanding Voltage (DWV) "High Pot"

System Summary

Technology Owner

Beyond patent applicability.

Vendor

Numerous available, including DIT-MCO

Description

A high potential (500V and above, typically 1500V to 2500V) is applied to a conductor. The system then looks for any lost current or arcing (to another conductor or to ground) which would indicate a discontinuity in the insulation or dielectric around a conductor. Both AC and DC DWV are used.

System Specifications

Various standards, including UL, IEC, and CSA.

Features and Limitations

DWV testing could, in principle, be used to detect flaws in the insulation or dielectric in Shuttle wiring. There are, however, two major impediments to this. First, depending on the voltage used, the test can result in heating to the extent that it is destructive. Second, because of the thickness of the (double wrapped) Kapton tape on Shuttle wiring, the distance of the conductor from any component to which voltage could leak is excessive. Therefore, the voltage required to detect a defect is generally going to be so great as to cause damage to the wire harness. If alternate gases such as helium are used, the distance can be greatly increased for the same voltage, making it much more practical in the Shuttle environment.

Technology Readiness Level

9

Contact List

Numerous suppliers available for this technology.

Defect Detection Technologies

Time Domain Reflectometry (TDR)

System Summary

Technology Owner

Patents probably expired on the basic technology

Vendor

- Agilent Technologies (formerly an HP division)
- Tektronix
- CM Technologies

Description

A pulse in the form of a single, rapid change in potential is sent down a conductor. Anything along the conductor that changes impedance (changes in resistance, capacitance or inductance) will reflect some energy back along the conductor. In principle these changes could be caused by such things as corrosion, breaks or removal of dielectrics or insulation, frayed or broken shields, changing the configuration of a wire or even changing the configuration of neighboring wires or ground planes. In practice, the changes seen will depend on sensitivity of the TDR instrument, care taken in making measurements and interpretation of data.

These measurements could, in principal, give information about the existence of defects, the kind of defect and the location of defects. There is the potential for developing a magic bullet of wire testing, but the present reality is far from achieving this potential because no one has attempted to draw the information out of the data in any rigorous analyses.

This instrument consists of a pulse generator and sensing equipment to recognize reflections of the pulse from conductor features, which result in a change in impedance. It is attached to one end only of a conductor. It uses an assumed velocity of the pulse to determine the location of the feature. According to Agilent, it can locate a feature to a tolerance of about 0.5 cm in a line 60 or more feet (1,828 cm) long. Other manufacturers claim less exact location sensing capability.

Features and Limitations

This system could be used as a means of identifying and locating defects in the conductor or shielding. Some claims have been made as to the possibility of using it to locate insulation defects also, but we

do not yet have verification of this. Accomplishing this task might require some enhanced signal processing and is probably not currently feasible.

Automated testing is not currently being used, though some efforts have been put forth to develop it. Most effective use of TDR would require development of this technology. Automation of TDR will also require development of signal analysis capability.

Contact List

- Agilent Technologies
- CM Technologies Sheldon Lefkowitz
- Tektronix

Standing Wave Ratio (SWR)

System Summary

Technology Owner

Patents probably expired on the basic technology

Vendor

- Agilent (formerly an HP division)
- Tektronix
- CM Technologies

Description

The Standing Wave Ratio is a measure of impedance matching. It can be used to compare the overall condition of a wire with that of a known control. This is a lumped parameter in the sense that it measures the net ability of a complete wire path to support a particular frequency. It can therefore be used as a pass-fail measurement of wire impedance. It will probably be most sensitive to opens, shorts, corroded or damaged connectors, and breaks in shielding. With proper switching technology it could be automated.

Classical SWR or Standing Wave Ratio measurements have long been used to characterize impedance matching in antennas by applying a sinusoidal voltage at one frequency, measuring the reflected voltage, and computing the ratio as:

SWR = (1-rho)/(1+rho) where rho is the reflection coefficient.

The ideal case where there is perfect impedance matching (no reflected power) gives SWR = 1 and the worst case where all power is reflected gives SWR = infinity. A typical acceptable value is 1.5.

CM Technologies uses a set of discreet SWR measurements to help characterize wires. They speculated that the range of frequencies they typically use for nuclear power plant applications might be too low to fully characterize Shuttle wiring.

Features and Limitations

SWR can be used to identify opens and shorts. It can contribute to finding other defects as well. It does not have any locating capability.

Contact List

- Agilent Technologies
- CM Technologies Sheldon Lefkowitz
- Tektronix

Standing Wave Reflectometry (SWReflectometry)

System Summary

Technology Owner

NASA

Vendor

Eclypse (current exclusive licensee from NASA)

Description

The instrument is described as an Impedance Based Cable Tester. It is attached to one end only of a conductor. It sends a spectrum of frequencies down the conductor, and depends on a reflection of a portion of the signal from features of the conductor which result in a change in impedance. By examining the frequency (or frequencies) at which a standing wave occurs, the feature can be located.

Specifications

This system can used as a means of identifying and locating hard faults in a conductor. It is not currently able to locate defects in the insulation, but could possibly, using enhanced signal processing, be made to do that. Doing this, however, would involve a significant amount of work.

Contact List

Eclypse	Chris Teal	909 947-8839 x30	cteal@eclypse.org
Eclypse	Skyy Jacquet, Applications Specialist	909 947-8839 x24	
Dynac Corp	Pedro Medelius, Inventor	321 867-3322	

Ultrasound

According to Joe Heyman at Langley Research Center, the state of the art ultrasound equipment is unlikely to help in existing wiring, although he feels that newly designed self-monitoring systems could apply current ultrasound techniques. Ultrasound could be developed further to be applied to existing wiring systems.

System Summary

Technology Owner

Undeveloped technology

Vendor

Lawrence Livermore National Laboratory (LLNL)

Description

Various modes may be envisioned for the use of ultrasound in the inspection of wires. First, is to send ultrasonic energy down the wire, using it to inspect the conductor. Second, one might envision using ultrasonic energy transmitted through the wire to inspect the insulation. Finally, it might be possible to induce ultrasonic vibrations radially into the insulation as a means of inspecting either the insulation or the conductor.

Lawrence Livermore National Laboratory (LLNL) has done some development of ultrasonics, using a pipe as a wave guide. This might be extended to use of the wire as a wave guide for inspection of the wire itself.

System Specifications

None available.

Features and Limitations

Ultrasonic energy is generally reflected from surfaces and interfaces between materials of different acoustic characteristics. It is likely that a suitable couplant could be found to permit longitudinal inspection of the conductor. This technique has not, however, been used in practice for wire inspections, and other techniques (TDR, SWR, and resistance and capacitance measurements) exist that are probably more effective. This technique would probably be limited by attenuation to no more than 30 to 50 feet of wire, and it would be used for inspection of the conductor only. Further difficulty would be expected with stranded wire.

Ultrasonic energy induced radially into insulation might be used to inspect the insulation. Techniques might be developed to accomplish this, but accessibility will undoubtedly be a problem for a very large percentage of the wiring.

Technology Readiness Level

3

Contact List

Nancy Del Grande

Lawrence Livermore National Laboratory (LLNL)

Network Analyzer

System Summary

Vendor

Agilent

Description

Network analyzers are common tools for characterizing the frequency response of communications networks. In this case a swept sinusoidal voltage is applied to a cable and impedance values over a range of frequencies (from 300KHZ to GHZ) are measured from reflection coefficients. These data are typically transformed into the time domain and used to locate faults. Hewlett Packard literature says it works best when the cable impedance is near 50 ohms. Boeing Shuttle test engineers at

Palmdale use an HP8328A network analyzer to find impedance mismatches in controlled impedance cables. Network analyzers send a swept-frequency or chirp sinusoidal voltage down a wire. Reflections of the signal are measured through a directional coupler and ratioed with the incident signal. The data are transformed into the frequency domain for display.

Features and Limitations

Locates and resolves discontinuities and mismatches versus distance.

Shows good accuracy when the unknown impedance is close to the characteristic impedance, hence a narrow impedance measurement range.

The network analyzer is more appropriate for measuring global properties of a cable rather than measuring local characteristics.

This equipment may only be good for monitoring overall health of a cable, not for locating specific faults.

Contact List

Agilent	Sales Representatives	Colorado
	Jim Hardin	Mountain View, CA
	Field Engineer	

Phase Gain Analyzer

System Summary

Vendor

Agilent

Description

Gain-phase analyzers like network analyzers generate a swept sinusoidal voltage and measure current generated by the voltage across an accurately known low-value resistor. The frequency range (~40HZ up to 110MHZ) is lower than network analyzers. The Boeing/Rockwell personnel have used an HP4194A gain-phase analyzer in their wire testing research. Agilent describes this measurement as an 'auto-balancing bridge method'. Apparently a variable frequency current (not voltage) is sent through the 'device under test' as well as a reference resistor. In a proposal to the FAA one company claims to be able to locate defective insulation in a cable to within a centimeter using a phase gain analyzer from HP which is the primary reason that it being considered for use.

Features and Limitations

Advantages include wide frequency coverage and high accuracy over a wide impedance measurement range.

The disadvantage is that higher frequencies (40MHZ) are not available.

The phase gain analyzer is more appropriate for measuring global properties of a cable rather than measuring local characteristics.

This equipment may only be good for monitoring overall 'health' of a cable, not for locating specific faults.

Contact List

Agilent	Sales Representatives	Colorado
	Jim Hardin	Mountain View, CA
	Field Engineer	

Infrared Inspection

System Summary

Technology Owner

Unknown. May be public domain. Some work is reportedly being done in this area by a private sector company.

Vendors

Materials Technologies Corporation

Description

Wiring is subject to some resistive heating when a current is passed through it. Infrared techniques might be used to identify hot spots where thin or missing insulation allows greater heat transfer. Various techniques are used to enhance the ability to see very small increases in temperature, or to magnify the section of wire under inspection, for better visibility.

Materials Technologies Corporation has developed, under contract with the Air Force, an infrared unit capable of viewing all surfaces of a wire (assuming accessibility) at the same time, with magnification capability to 60X.

Lawrence Livermore National Laboratory (LLNL) has done development work on a system using thermal inertia with an infrared video camera as a means of identifying subsurface conditions. This system has not yet been used for wiring inspection. Because of the structural complexity of a wire bundle , it is likely that this will not have great application.

System Specifications

Defects to 100µm, thermal variations of 0.02°C

Features and Limitations

Since this could be essentially a visual inspection, and perhaps be done by a machine, it could be made very non-intrusive. Conversely, if the inspection is performed in a very non-intrusive fashion, it could provide access to a very small portion of the wires. It has the advantage of providing recording capability if required.

Technology Readiness Level

9

Contact List

TBD

Resistance Ratio

System Summary

Technology Owner

Probably public domain.

Vendors

- DIT-MCO
- CableTest

Description

Sensitive resistance measurements can be made to approximate the ratio of the lengths of cable from a short to each end of the cable. Location can probably be pinpointed to approximately 5-10% of the length of the cable.

System Specifications

Currently unknown.

Features and Limitations

Limitation on the accuracy is related to the impedance of the cables and the contact between the cable and ground. The technique requires access to both ends of the cable.

Technology Readiness Level

9

Contact List

None available.

Capacitance Ratio

System Summary

Technology Owner

Probably public domain.

Vendors

- DIT-MCO
- CableTest

Description

Sensitive capacitance measurements can be made to approximate the ratio of the lengths of cable from an open to each end of the cable. Location can probably be pinpointed to approximately 5-10% of the length of the cable.

System Specifications

Currently unknown.

Features and Limitations

Limitation on the accuracy is related to the capacitance of the overall system, including a function of the distance of the cable in question to the surrounding shield or cables. The technique requires access to both ends of the cable.

Technology Readiness Level

9

Contact List

None available.

Radio Frequency Techniques / Electromagnetic Emissions

Reverse Geometry X-Ray Inspection

System Summary

Technology Owner

Dr. Dick Albert, Digiray Corp.

Vendor

Digiray Corp. San Ramon, CA 94583

Description

Utilizes an x-ray source that uses the raster of a tube that is shaped like a television picture tube (comprised of several scanning electron beam tubes). The object is placed far enough away from the detector so most of the deflected x-rays dissipate. The detectors can be made very small, preventing pickup of off-course x-rays, thereby virtually eliminating image degradation.

Features and Limitations

When compared to other non-destructive inspection technologies (as part of an USAF-sponsored engineering support task, Northrop Grumman Corp. s Surveillance & Battle Management Systems Team) the Reverse Geometry X-ray method was found superior for non-contact and non-line-of-sight inspection. Methods compared were thermal imaging, acoustic emission, eddy current, ultrasonic, visual, and conventional x-ray.

Discussions with Digiray Corp., however, indicate that defect –to-specimen size associated with 12 to 16 gauge wire is below the detection threshold even for this technique.

Contact List

Dr. Dick Albert, Digiray Corp, President, 925-838-1510.

Data Analysis Methods

Neural Networks

Description

Neural networks will not work with time-dependent data. It needs a more discrete sets of data features instead of thousands of raw data points, what is needed is a more finite set of numbers that assign a value to some feature such as overall impedance, overall resistance, or impedance at a specific frequency. Neural networks could be applied if the health of a wire could be characterized using a set of features represented by numbers such as:

1. Overall resistance
2. Overall impedance
3. Locations of discontinuities
4. SWR at specific frequencies
5. Amplitudes of discontinuous features of TDR signals

However, these are just examples and it is very unlikely that this set of features will actually characterize the health of a wire to the degree needed to locate all wire defects. With such data in a neural network, one would assign weights to features and classify the health of the wire based on the weighted values of those features.

Features and Limitations

It will be likely necessary to apply filters such as wavelet analysis to the raw data both to locate and classify defects. Neural networks are probably not required for identifying the existence of some defects. A discontinuity in a TDR signal implies a discontinuity in the conductor. If this occurs at an unexpected location in the wire, it implies a defect exists there. Identifying location in the wire, however, could require a neural network.

If location of defects within connectors is needed, by neural network methods, such as broken pins, then the set of features needed to characterize the health of a wire may grow into the hundreds. While this is not necessarily a problem for neural networks, it would require the number of training data sets acquired to increase by at least the same order of magnitude. A follow-up conversation can be held once the WIRe team has acquired actual test data.

Wavelet

Description

In order to automate testing of Shuttle wiring, test signals must be processed and analyzed to extract relevant information. A signal processing method developed in the last fifteen years is wavelet analysis. Wavelet functions are convolved with test signals to generate both time and frequency information about features of the test signals. Wavelet analysis is closely analogous to Fourier analysis, where sine or cosine functions are convolved with test signals to de-synthesize those signals into their frequency components. Wavelet analysis is not universally better than Fourier analysis or other signal processing methods. It is more efficient in representing localized, transient signals and can be used to extract both time and frequency information, so that not only are signal features extracted by the analysis, they can be assigned to particular parts of the signal.

Seven years ago, one of the developers of wavelet analysis, Dr. Ingrid Daubechies, cautioned that wavelets are not an ultimate solution, but rather another new tool. Nevertheless, the reputed ability of wavelet analysis to efficiently extract transient signal features and to localize these features will be a valuable tool in wiring testing. If time-domain reflectometry (TDR) is to be used to locate faults in cables, impedance changes along cables that can occur due to shorts, open circuits, shielding breaks and so on, will yield transient features in the TDR signal that may best be recognized and localized using wavelet analysis.

Features and Limitations

In 15 years wavelet analysis has already been broadly applied in a variety of disciplines, but it is not the kind of universally known tool that Fourier analysis has become over two centuries of development. Hewlett-Packard or Tektronix provide spectrum analyzers that uses Fourier de-synthesis, but no wavelet analyzer boxes are available. Commercial analytical software is being sold (e.g. MATLAB, from The MathWorks, Mathematica, from Wolfram Research) that includes strong wavelet analysis capability.

The current methods of wire testing (continuity , isolation, and DWV tests) and any new methods that produce a single data point would not benefit from wavelet analysis or any older signal processing methods. TDR signals are used to test cables, and automated analysis of those signals is needed. Software will be required to extract interesting signal features and categorize and interpret those features.

It is clear that wavelet analysis could be used (possibly in conjunction with other signal processing methods) to extract the signal features, but it would require some development to adapt it to this particular application. The process would be evolutionary, but the more clear-cut faults like shorts and open-circuits would probably be relatively trivial to locate and even interpret. The more subtle problems of locating signal features due to insulation or shielding damage would depend on proving the capability of TDR to exhibit those features and developing intelligent code to interpret what wavelet analysis extracts.

Appendix 5 – Test Bed Descriptions

Test Bed Development

The proof of concept for the Automated Verification and Validation (AV&V) technology was demonstrated by designing and fabricating a workable test bed. The test bed needed to support a thorough investigation of both wire harness configurations and wire fault evaluations. Both in-house personnel and outside vendors would need access to and utilization of the test bed.

It was determined that there should be three (3) separate wire harnesses to best cover these needs.

1. A configuration harness (covering AV&V) to test smart ATE systems
2. A signal wire harness with known faults (using 22-gauge wire)
3. A power wire harness with known faults (using 12-gauge wire)

Each harness was designed using the same guidelines to eliminate any unintended variations. They would have a solid conductive backplane for grounding purposes. They would lay flat, with no hinging of ground plane or wires, to prevent changes and wear to the wire as configured. There would also be ample room around the harness as it was secured in a coil pattern to the backplane. The final guideline was to follow proper wire harness assembly rules with no sharp radius curves and to use proper cable clamping techniques.

For ease of shipment, all three wire harnesses were constructed in tray type boxes that could be latched together as one unit and easily secured into one shipping container for ease of travel. This allowed tests to be conducted at various locations.

The following photographs, Figures 9, 10, 11, 12 show individual wire harness trays and the combined harness box being stowed into the shipping container. The size of each tray was 48 inches x 30 inches x 2 1/2 inches. The overall weight of the shipping container with the test bed inside was approximately 170 pounds.

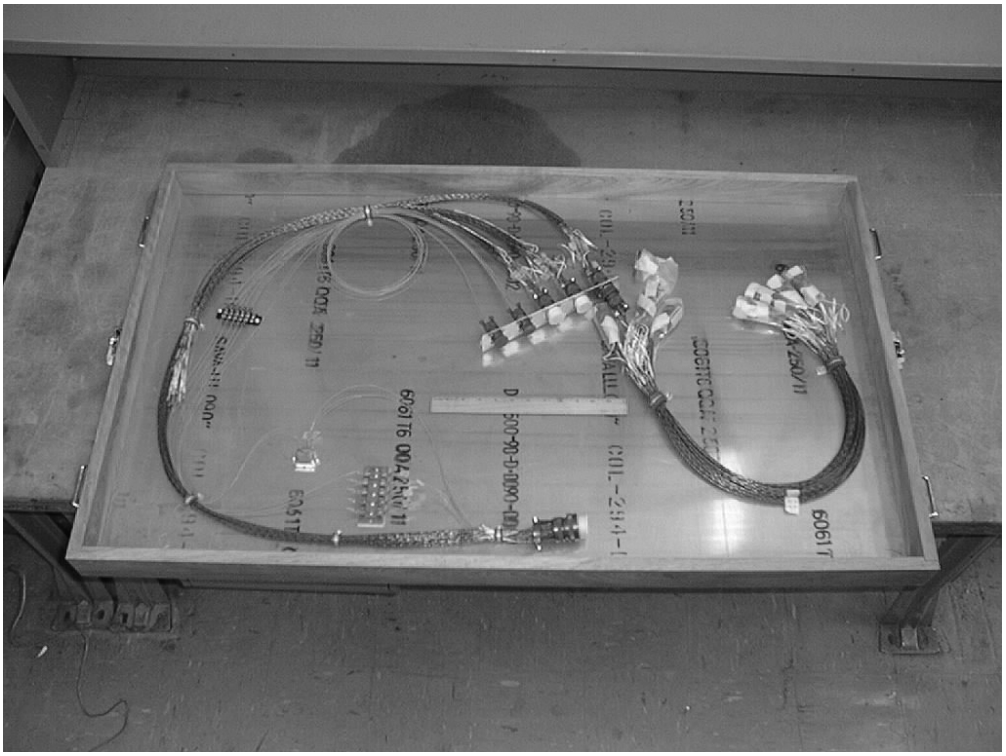

Figure 9. Configuration Wire Harness with Tray.

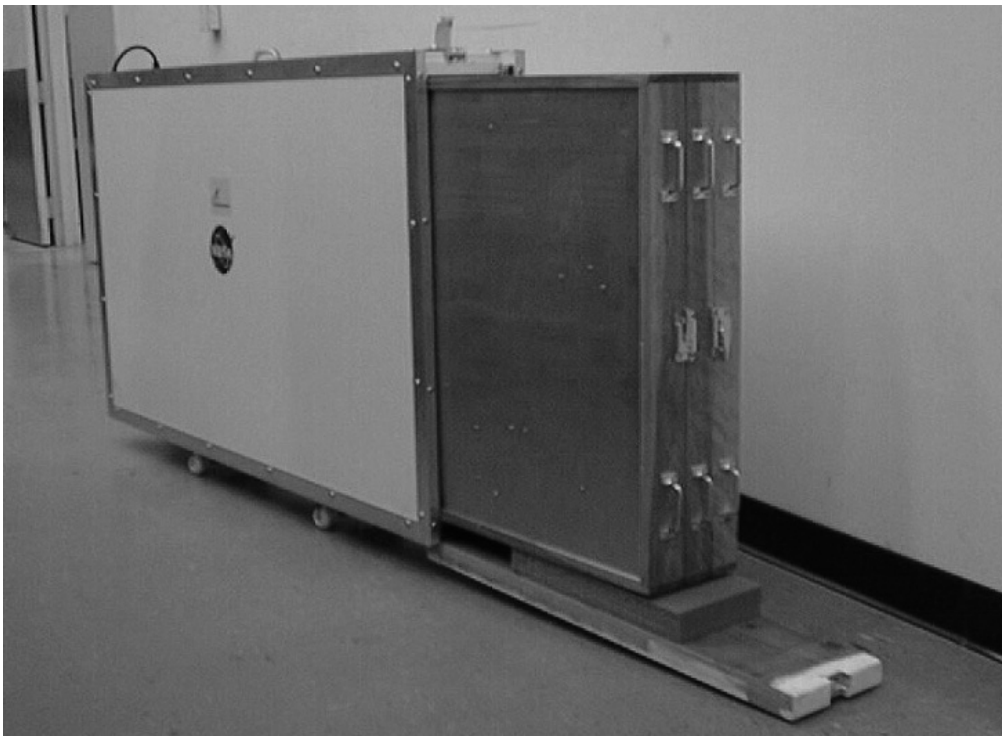

Figure 10. Three Wire Trays Loading into the Shipper.

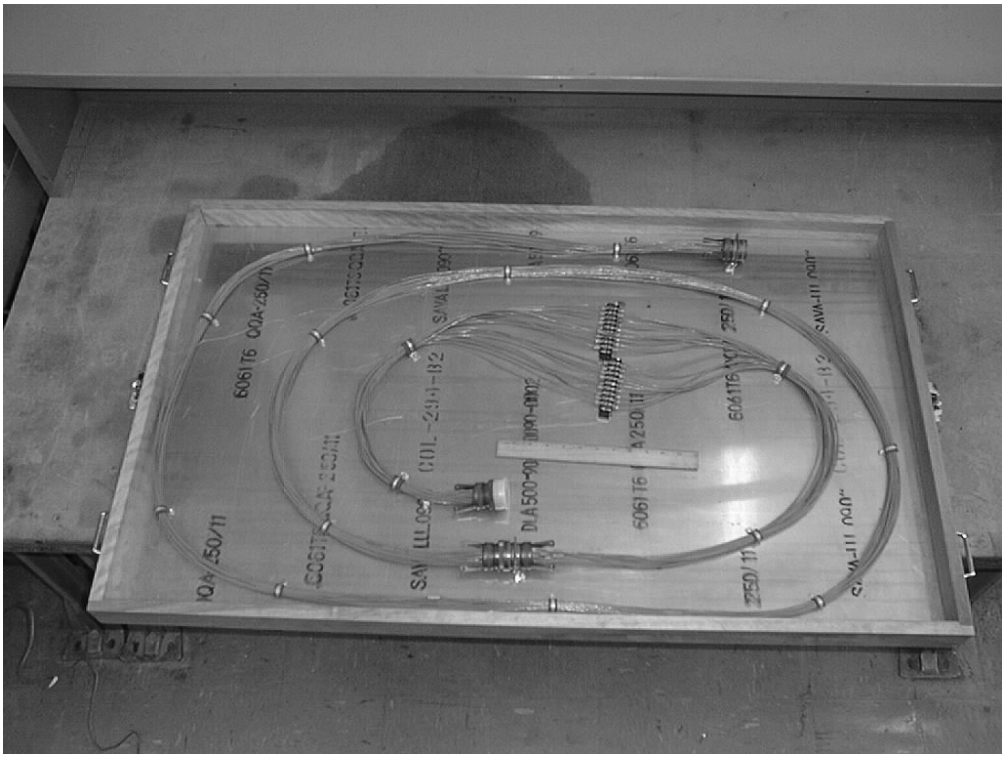

Figure 11. Signal Wire (22 Gauge) Fault Harnss and Tray.

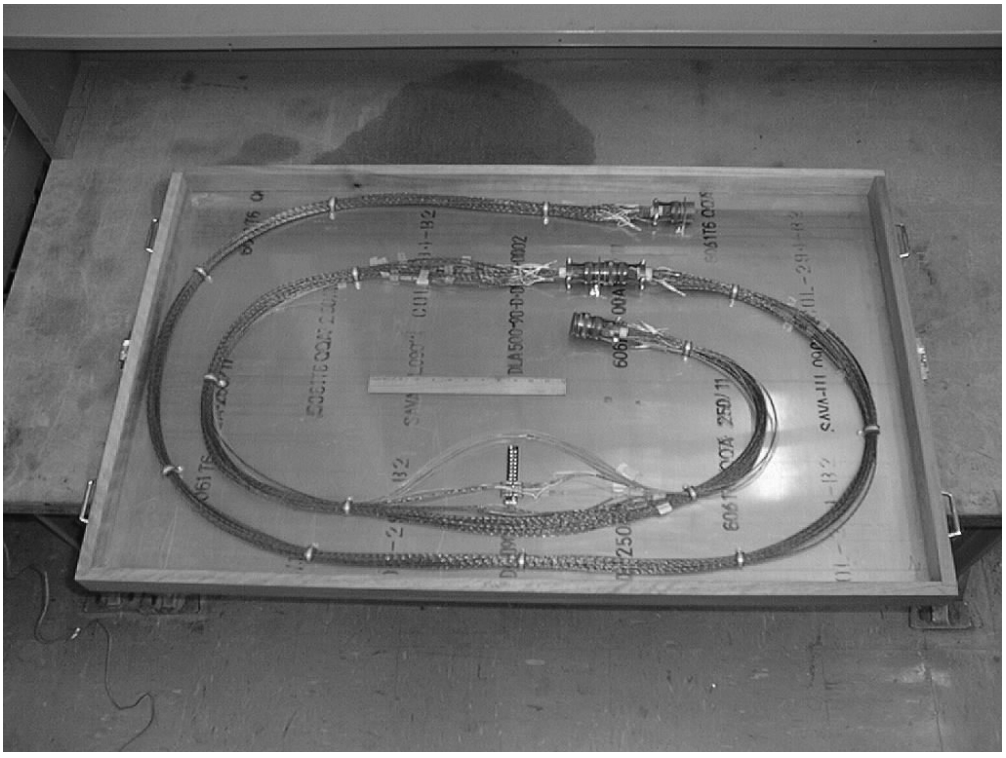

Figure 12. Signal Wire (12 Gauge) Fault Harness and Tray.

AV&V Test Bed Wiring Diagram

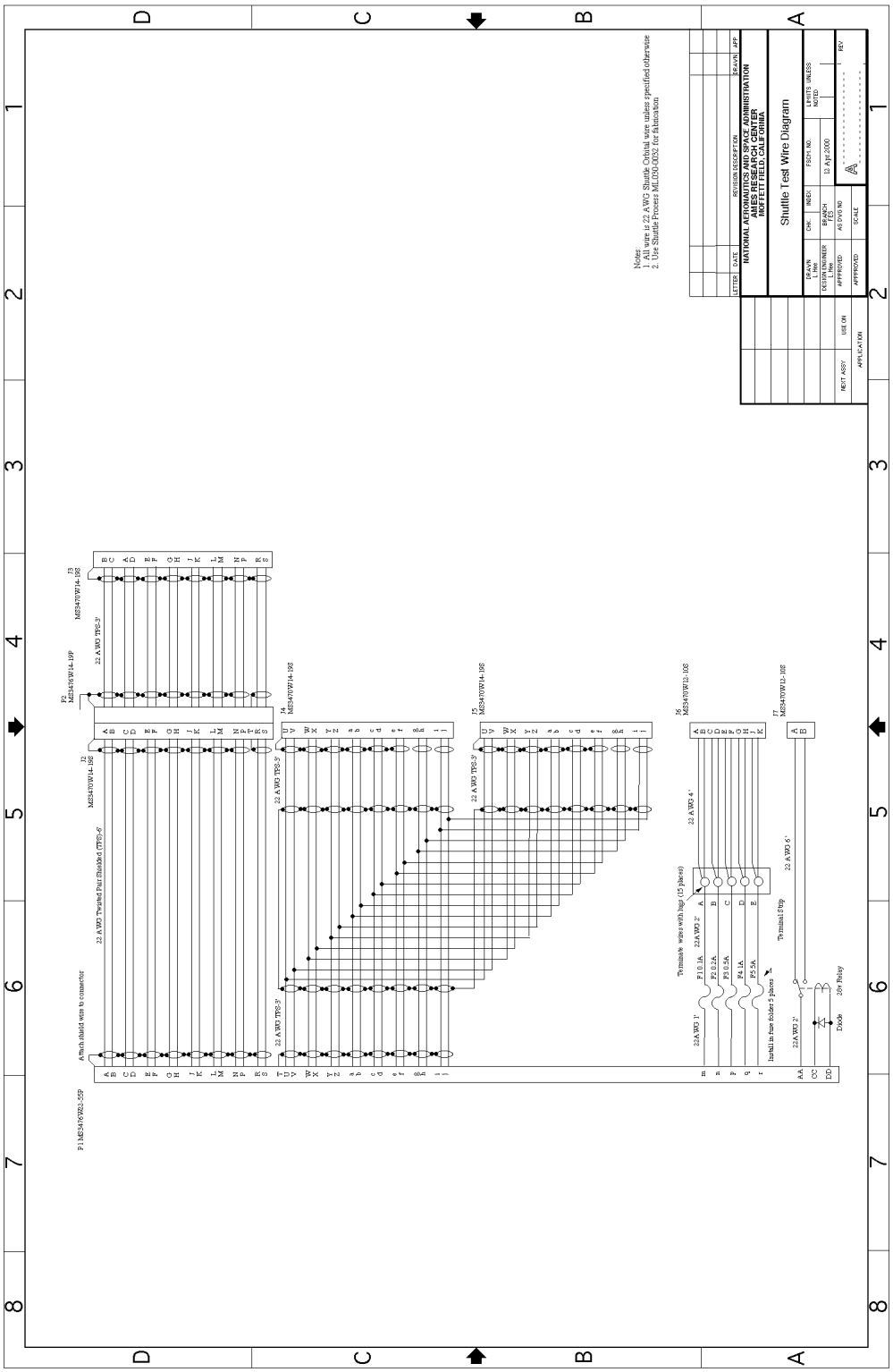

Figure 13. Test Bed Wiring Diagram.

Description of the AV&V Test Bed

The AV&V Test Bed was designed to represent a typical Orbiter wire harness assembly. The design of the wiring diagram is shown in Figure 13.

The AV&V test bed was fabricated utilizing new Orbiter wire provided by KSC and fabricated with accepted Orbiter guidelines. It should be noted all connectors on the AV&V test bed were not space-qualified hardware, since time limit on the Pilot Study prevented the acquisition of the space-qualified connectors. The WIRe team members decided to use MIL SPEC connectors to not introduce any anomalies to the AV&V demonstrations. A photograph of the AV&V test bed is shown in Appendix 6.

AV&V test bed bill of materials

Item	Quantity	Unit	Description	Part Number
1	1	Ea.	55 pin connector	MS3470A20-55P
2	1	120 Ft.	22 AWG twisted shielded pair	C2TS
3	1	79 Ft.	22 AWG twisted pair	C2T
4		Ea.	19 pin connector	MS3471A14-19S
5	1	Ea.	19 pin connector	MS3471A14-19P
6	2	Ea.	10 pin connector	MS3471A12-10S
7	1	Ea.	28Volt Relay	
8	1	Ea.	Terminal Block	
9	1	Ea.	0.1 Amp Fuse	
4	1	Ea.	0.2 Amp Fuse	
5	1	Ea.	0.5 Amp Fuse	
6	1	Ea.	1.0 Amp Fuse	
7	1	Ea.	5.0 Amp Fuse	

Table 3. AV&V Test Bed Materials.

Description of the Integrity Test Beds

Two test beds were built for the purpose of demonstrating wire integrity test equipment. The WIRe team introduced a number of kinds of defects in each of the cables, and carefully recorded the types and locations of defects. The defects were meant to be representative of the kinds typically found in the Orbiter.

Signal Wire Integrity Test Bed

The following table describes the known defects introduced in the Signal Wire (22 gauge) Integrity Test Bed.

Harness #22-1 (No defects)				
Total Length = 10 feet, male connector one end, female the other				
Pin	Gauge	Type	Conductor	Socket
A	22	TP	1	A
B	22	TP	2	B
C	22	TP	1	C
D	22	TP	2	D
E	22	TP	1	E
F	22	TP	2	F
G	22	TP	1	G
H	22	TP	2	H
J	22	TP	1	J
K	22	TP	2	K
L	22	TP	1	L
M	22	TP	2	M
N	22	TP	1	N
P	22	TP	2	P
R	22	TP-S	1	R
S	22	TP-S	2	S
Backshell	Shield	TP-S	S	Backshell
T	22	TP-S	1	T
U	22	TP-S	2	U
Backshell	Shield	TP-S	S	Backshell
V	22	TP-S	1	V
W	22	TP-S	2	W
Backshell	Shield	TP-S	S	Backshell
X	22	TP-S	1	X
Y	22	TP-S	2	Y

Backshell	Shield	TP-S	S	Backshell
Z	22	TP-S	1	Z
Pin	Gauge	Type	Conductor	Socket
a	22	TP-S	2	a
Backshell	Shield	TP-S	S	Backshell
b	22	TP-S	1	b
c	22	TP-S	2	c
Backshell	Shield	TP-S	S	Backshell
d	22	TP-S-CI	1	d
e	22	TP-S-CI	2	e
Backshell	Shield	TP-S-CI	S	Backshell
f	24	TP-S-CI	1	f
g	24	TP-S-CI	2	g
Backshell	Shield	TP-S-CI	S	Backshell
h	24	TP-S-CI	1	h
I	24	TP-S-CI	2	I
Backshell	Shield	TP-S-CI	S	Backshell
j	24	TP-S-CI	1	j
k	24	TP-S-CI	2	k
Backshell	Shield	TP-S-CI	S	Backshell
m	24	TP-S-CI	1	m
n	24	TP-S-CI	2	n
Backshell	Shield	TP-S-CI	S	Backshell
p	24	TP-S-CI	1	p
q	24	TP-S-CI	2	q
Backshell	Shield	TP-S-CI	S	Backshell
r	24	TP-S-CI	1	r
s	24	TP-S-CI	2	s
Backshell	Shield	TP-S-CI	S	Backshell
t	24	TP-S-CI	1	t
u	24	TP-S-CI	2	u

Backshell	Shield	TP-S-CI	S	Backshell
v	24	TP-S-CI	1	v
w	24	TP-S-CI	2	w
Backshell	Shield	TP-S-CI	S	Backshell
x	24	TP-S-CI	1	x
y	24	TP-S-CI	2	y
Pin	Gauge	Type	Conductor	Socket
Backshell	Shield	TP-S-CI	S	Backshell
z	24	TP-S-CI	1	z
AA	24	TP-S-CI	2	AA
Backshell	Shield	TP-S-CI	S	Backshell
BB	24	TP-S-CI	1	BB
CC	24	TP-S-CI	2	CC
Backshell	Shield	TP-S-CI	S	Backshell
DD	24	TP-S-CI	1	DD
EE	24	TP-S-CI	2	EE
Backshell	Shield	TP-S-CI	S	Backshell
FF	24	TP-S-CI	1	FF
GG	24	TP-S-CI	2	GG
Backshell	Shield	TP-S-CI	S	Backshell
HH				HH

DC = damaged conductor

DC* = exposed conductor, very minor damage

M5 = 5 mm Missing Insulation (one side only)

M1" = 1" of missing outer insulation 360 degrees

Dmgd Shield = 25% cut, plus abrasion to strands

Missing Shield = 0.25" missing shield

Harness #22-2 (Defects as indicated)

Total Length = 7 feet, male connector one end, female the other

Pin	Gauge	Type	Conductor	Defect 25" from Male Conn.	Splice 31" from Male Conn.	TB Output Sockets	Defect 4" from Conn.	Socket
A	22	SC	1					A
B	22	SC	1					B
C	22	SC	1		C, Hanging			C
D	22	SC	1		D, Hanging			D
E	22	SC	1		E	E		E
F	22	SC	1		F	F		F
G	22	SC	1	M5				G
H	22	SC	1					H
J	22	SC	1	M1"				J
K	22	SC	1					K
L	22	SC	1	DC				L
M	22	SC	1					M
N	22	SC	1					N
P	22	SC	1					P
R	22	TP-S	1					R
S	22	TP-S	2					S
Backshell	Shield	TP-S	S					Backshell
T	22	TP-S	1		T, Hanging	T		T
U	22	TP-S	2		U, Hanging	U		U
Backshell	Shield	TP-S	S					Backshell
V	22	TP-S	1	M1"				V
W	22	TP-S	2					W
Backshell	Shield	TP-S	S					Backshell
X	22	TP-S	1	Dmgd Shield				X
Y	22	TP-S	2					Y
Backshell	Shield	TP-S	S					Backshell
Z	22	TP-S	1	Expsd Cndctr				Z

a	22	TP-S	2					a
Backshell	Shield	TP-S	S					Backshell
b	22	TP-S	1				Dam.Shield	b
Pin	Gauge	Type	Conductor	Defect 25" from Male Conn.	Splice 31" from Male Conn.	TB Output Sockets	Defect 4" from Conn.	Socket
c	22	TP-S	2					c
Backshell	Shield	TP-S	S					Backshell
d	24	TP-S-CI	1					d
e	24	TP-S-CI	2					e
Backshell	Shield	TP-S-CI	S					Backshell
f	24	TP-S-CI	1		Butt Splice			f
g	24	TP-S-CI	2		Butt Splice			g
Backshell	Shield	TP-S-CI	S					Backshell
h	24	TP-S-CI	1	M5				h
I	24	TP-S-CI	2					I
Backshell	Shield	TP-S-CI	S					Backshell
j	24	TP-S-CI	1	M1"				j
k	24	TP-S-CI	2					k
Backshell	Shield	TP-S-CI	S					Backshell
m	24	TP-S-CI	1	M1"	Butt Splice			m
n	24	TP-S-CI	2					n
Backshell	Shield	TP-S-CI	S					Backshell
p	24	TP-S-CI	1				Dam.Shield	p
q	24	TP-S-CI	2					q
Backshell	Shield	TP-S-CI	S					Backshell
r	24	TP-S-CI	1				M5	r
s	24	TP-S-CI	2					s
Backshell	Shield	TP-S-CI	S					Backshell
t	24	TP-S-CI	1	Dmgd Shield				t
u	24	TP-S-CI	2					u
Backshell	Shield	TP-S-CI	S					Backshell
v	24	TP-S-CI	1	Msng Shield				v

w	24	TP-S-CI	2					w
Backshell	Shield	TP-S-CI	S					Backshell
x	24	TP-S-CI	1				Dam.Shield	x
y	24	TP-S-CI	2					y
Backshell	Shield	TP-S-CI	S					Backshell
z	24	TP-S-CI	1				Msng Shield	z
AA	24	TP-S-CI	2					AA
Pin	Gauge	Type	Conductor	Defect 25" from Male Conn.	Splice 31" from Male Conn.	TB Output Sockets	Defect 4" from Conn.	Socket
Backshell	Shield	TP-S-CI	S					Backshell
BB	24	TP-S-CI	1	DC				BB
CC	24	TP-S-CI	2					CC
Backshell	Shield	TP-S-CI	S					Backshell
DD	24	TP-S-CI	1	Expsd Cndctr				DD
EE	24	TP-S-CI	2					EE
Backshell	Shield	TP-S-CI	S					Backshell
FF	24	TP-S-CI	1				DC*	FF
GG	24	TP-S-CI	2					GG
Backshell	Shield	TP-S-CI	S					Backshell
HH								HH

DC = damaged conductor

DC* = exposed conductor, very minor damage

M5 = 5 mm Missing Insulation (one side only)

M1" = 1" of missing outer insulation 360 degrees

Dmgd Shield = 25% cut, plus abrasion to strands

Missing Shield = 0.25" missing shield

Wire Type

SC = single conductor

TP-S = twisted shielded pair

TP-S-CI = twisted shielded pair, controlled impedance

Table 4. Known Defects in the Signal Wire (22-gauge) Integrity Test Bed.

Power Wire Integrity Test Bed

The following table describes the known defects introduced in the Power Wire (12 gauge) Integrity Test Bed.

Harness #12-1 **Harness #12-2**

Harness 12-1, Length 15 feet				**Harness 12-2, Length 6 feet**				
		Defect 80" from male			Splice at 31" to	Terminal Block	Defect 3" from socket	
Pin	Gauge		Socket	Pin	Output Sockets	Output Sockets	3"	Socket
A	12		A	A		A		A
B	12		B	B		B, Hanging		B
C	12		C	C		C		C
D	12		D	D		D, Hanging		D
E	12		E	E		E		E
F	12		F	F		F	M5	F
G	12		G	G		G		G
H	12	M5	H	H		H		H
J	12		J	J		J		J
K	12	M1"	K	K		K		K
L	12		L	L		L		L
M	12		M	M		M	M1"	M
N	12		N	N		N		N
P	12		P	P		P	DC	P
R	12		R	R		R	SC	R
S	12	DC	S	S		S		S
T	12		T	T		T		T
U	12		U	U		U	OC	U
V	12		V	V	In-line Splice	V		V

Defect Distribution:

8 Undamaged Conductor end to end, terminal block in second harness

1 Undamaged Conductor end to end, butt splice in second harness

2 Hanging tee in second harness, no flaws

1 Undamaged first harness, M5 in second

1 M5 in first harness, undamaged second

1 Undamaged first harness, M1" in second

1 M1" in first harness, undamaged second

Flaw Type Codes

M5 = missing insulation, 5 mm

M1" = 1" x 360° missing insulation

DC = damaged conductor

OC = open conductor

SC = shorted conductor

Table 5. Known Defects in the Power Wire Integrity Test Bed.

Appendix 6 – Product Demonstrations and Evaluations

Automated Test Equipment Features

General ATE Features

Aerospace, nuclear power plant, and communication industry methods for testing cable/wire harness were surveyed to compile a list of Commercial Off-the-Shelf (COTS) Automatic Test Equipment (ATE) manufacturers. Table 6 lists all ATE systems evaluated. In general, the ATE evaluated was found to be similar in features and test techniques. Differences were found in portability and the number of switchable test points per unit.

Common features to most ATE systems include the ability to import wire list data; automatically generate test procedures; self-learn a known good wire harnesses; conduct continuity, isolation, and DC DWV test; archive test data, and generate test data.

To conduct a continuity test, the ATE system applies a small voltage on each input connector pin and checks that the voltage is measured on the corresponding output pin. Via a series of relay switches, a Pass / Fail report is generated for each connector / pin. During this phase of the test, the ATE also conducts a resistance check to verify that the measured resistance is correct for the wire gauge, length, etc.

To conduct an isolation test, the ATE applies a small voltage on each input connector pin and checks all the pins on all output connectors. If a voltage is measured on an output pin that should be isolated from the input pin —that pin is not isolated and the failure is reported.

To conduct the Dielectric Withstand Voltage –(also known as High Pot) test, the ATE checks for insulation integrity by applying a high DC or AC voltage on each input connector pin and monitors for a disruptive discharge. The purpose is to determine whether insulation materials and spacing is adequate. The value of the voltage leakage resistance is important, requiring high accuracy DC digital measurement

Current Orbiter Test Requirements

The current Orbiter wire harness test requirements are specified in Electrical, Harness checkout; Requirements for; Shuttle Obiter Vehicle —ML0201-003 Dated December 6, 1999. Excerpts of the document are provided below. Refer to this document for complete specifications.

General requirements

Electrical Isolation All tests shall be accomplished without causing damage to wire harnesses, connectors, and equipment. Wire, cable, harnesses being tested shall not be connected to electrical or electronic components, units, or assemblies (Black Boxes) during performance of the test.

Piercing of insulation It is mandatory that all tests be made at wire or cable terminations.

Test Sequence The test sequence shall be as follows:

Continuity Test

Isolation Test

High Potential Test

Continuity Test All wires and cables shall be tested for continuity in accordance with applicable engineering drawing or wire list. Excluding the resistance of test cables and equipment, the resistance shall be in accordance with the table below.

Wire Size (AWG)	Maximum Resistance
26 thru 24	5 Ohms
22 thru 20	2 Ohms
18 thru 1/0	1 Ohms
Cable Shields (2)	3 Ohms

Wire Size Resistance Limits

Isolation Test All wires and cables shall be verified to be isolated prior to high potential testing. The isolation test is to be performed on all test points as specified in section 4.4. Isolation shall be verified by performing an open circuit resistance test.

High Potential Test. The Test Voltage shall be 1500 Volts DC, plus or minus 75 volts. The test dwell time shall be a minimum of 2 seconds but not exceed 2 minutes. Leakage current shall be less that 0.5 milliamperes. At the completion of high potential test, each conductor shall be grounded to prevent damage to vehicle electrical subsystems.

Installed Harness On initial harnesses installation continuity, isolation, and high potential test shall be performed on all wire harnesses. The test voltage shall be applied between the following points:

Between each conductor and all other conductors in the same connector.

Between each conductor and the connector shell.

Between each conductor and ground.

Between each conductor in a harness enclosed in metallic conduit or metallic braid and the conduit or braid.

ATE Vendors Evaluated

Vendor	Auto Learn	Auto Test Generation	Interfaces w/ database	Interface w/ "Smart" CAD	Test Analysis Tools	Report Generation	Demo Equipment
DITMCO	X	X	X	X	X	X	X
Eclypse	X	X	X	X	X	X	X
CK Tech	X	X	X		X	X	X
CM Tech					X	X	X
Cirrus	X	X	X			X	X
CAMI	X					X	
Cablescan	X	X	X			X	
WeeTech	X	X	X			X	
CableTest	X	X	X	X	X	X	X

Table 6. Automated Test Equipment Vendors and Features Evaluated.

CableTest

Test Equipment Description

The Model MPT 5000L Series Tester Wiring Analyzer is a Portable Base system, suitable for 19-inch rack mounting. Dimensions of the MPT500L are 17.5 w x 15 h x 21 d and the unit weights less than 70 lbs.

CableTest model MPT5000L can be configured to test over a 100,000 test points. The model demonstrated was configured for 1,200 test points with eight switching cards each with 150 points per card. The Model MPT5000L can be configured for both low voltage (0.1 to 28V at 0.1 to 2.5mA) and high voltage (50 to 3500VCD +/- 5%) testing capabilities. CableTest measurement sensitivity is as follows:

Connection Resistance: 0.1Ω to 400KΩ +/- 1% +/- 50mΩ

4-Wire Resistance: 0.01Ω to 100Ω

High Voltage Insulation Resistance: 1Ω to 50 MΩ (can be configured to 10GΩ)

High Voltage Dwell: 0.001 to 600 seconds (fully programmable)

Capacitance: 100pF to 1000µF +/- 2% +/-10pF

The MPT switching module dwell time is programmable for each test techniques; continuity, isolation, and DWV. Valid Dwell times range is 0.001 to 600 seconds – 1% (relay activation, etc.).

Test Setup

The MPT5000L was connected to the AV&V via a set of test adapter cables that CableTest fabricated utilizing AV&V mating connectors provided by NASA.

Test Preparation: CableTest fabricated a total of five test adapter cables that connected the model MPT to the AV&V wire harness. Each adapter cable had a DB-50 connector for the MPT connection, and a GFE connector for the AV&V wire harness connection. The time required to fabricate and ring-out these adapter cables was approximately 1 man-day

CableTest manually entered the expected wire list utilizing the AV&V wire harness drawing. The wire list can be used to auto-generated a test procedure program, or can be used to validate the resulting wire list created from the self-learn function. During the demonstration, the manually entered wire list was used to validate the self-learned created wire list. The time required to manually enter the wire list was approximately 0.5 man -hour. It should be noted that in place of manual entry, the CableTest software package CTPG could be configured to import wire data directly from a known good database such as CDF&TDS.

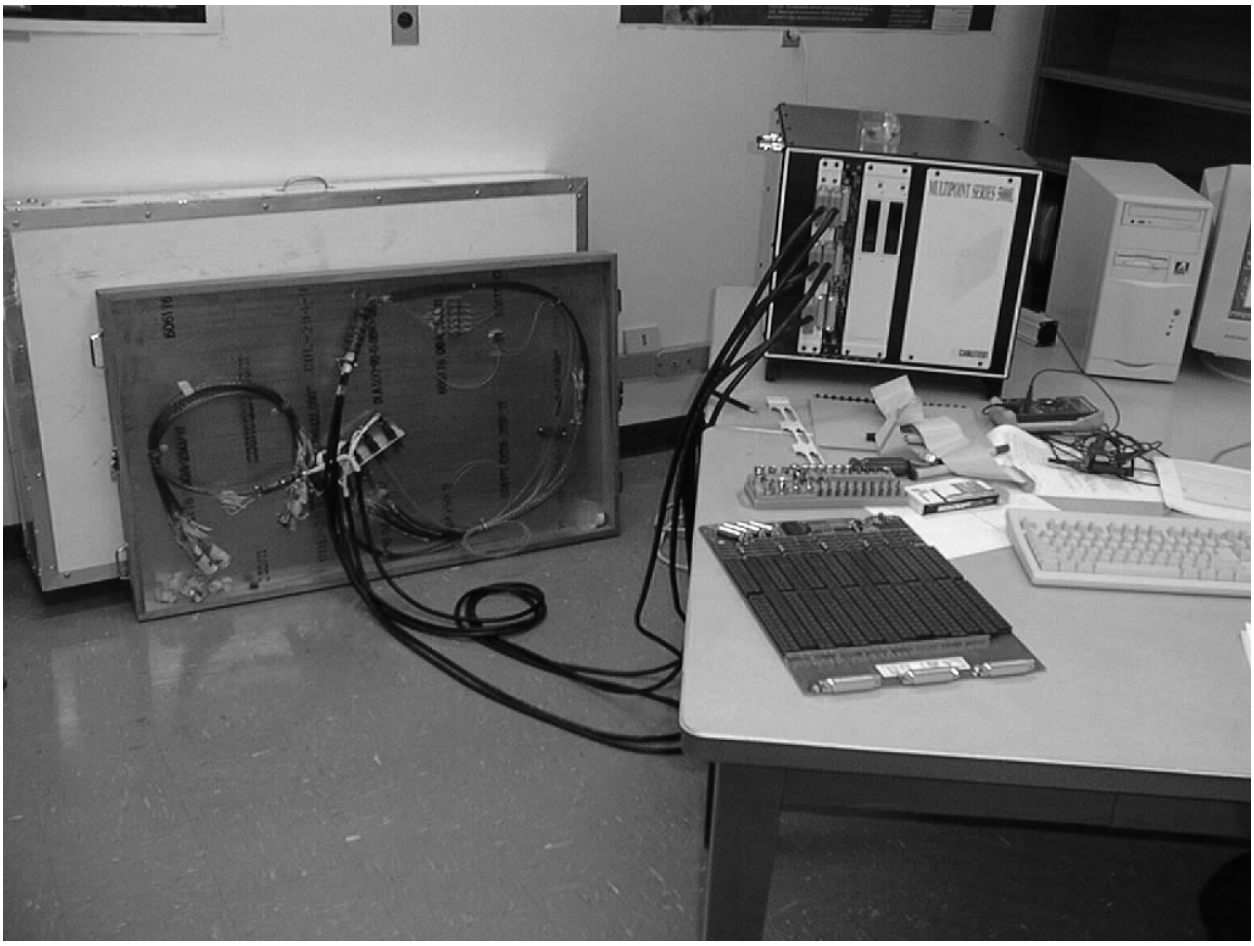

Figure 14. CableTest Demonstrates Its ATE on the Test Bed.

Setup time: To unpack the ATE system, unpack AV&V wire harness, connect PC to ATE system, connect the ATE system to the AV&V wire harness, took approximately 20 minutes. The first feature demonstrated was the self-learn feature. The resulting net list generated from the self-learn was checked against the expected wire list manually generated from the wiring diagram (Figure 13). The self-learn net list was incorrect. After 15 minutes of troubleshooting , it was found that the test adapter cables were not connected correctly to the MPT500L. Switching the test adapter cables to the correct configuration at the MPT5000L and executing a new self-learn yielded the correct net list. This net list was used to generate a test program. This demonstrated that the ATE systems could be easily connected in the wrong configuration. Therefore a self-learn function can be used to validate proper equipment setup prior to conducting a full test procedure.

Special Features

CableTest literature states that the software package CTPG will automatically generate test programs directly from databases, spreadsheets, wire list, or CAD/CAM systems including automatic

programming for components (resistors, capacitors, diodes, etc) . This was not demonstrated during the AV&V demonstration.

Test Conclusions

Overall, the MPT500L completed a successful demonstration of the methods of conducting self-learn features to validate proper equipment setup, and generate test procedures. Even though the software application CTPG was not demonstrated, the application seems promising and it is recommended that this package be purchased to evaluate test procedure generation from CDF&TDS. This demonstration did show that correct test setup is critical.

The MPT5000L successfully executed continuity, isolation, and DC DWV test in less that 3 minutes. This system was found to be well packaged, and once the system was connected correctly, testing of the wire harness es were easily and quickly conducted.

Vendor Contacts

CableTest International Inc.	Thomas Neal	(905) 475-2607	http://www.cabletest.com

Cirrus Systems Corporation

Test Equipment Description

Cirris demonstrated model 1500V Touch1. The Touch1 is a portable, extremely compacted and well-packaged unit. It should be noted that KSC is currently using Cirris model CH+ to test SRB and GSE wire harnesses. Dimensions of the touch1 are 22 W x 9 H x 6.5 D and the unit weights 25.4 lbs.

The Touch1 can be configured to test up to 1024 test points, and can execute low voltage (5 Volts @ 6mA maximum current) and high voltage (50 - 1500 VDC +/- 5% 50-1000VAC+/- 5%)tests. The Touch1 measurement sensitivity for connection resistance is 1Ω to 100Ω +/- 0.1Ω also 500Ω, 1MΩ, 5MΩ +/-10%, for 4-Wire Resistance: 0.001 to 10Ω +/-2%, for High Voltage Insulation Resistance: 5MΩ to 1GΩ +/-10%, and for capacitance 5nF to 100µF+/-10% +/-0.02nF (relative measurements to 10pF).

The Touch 1 switching module dwell time is programmable for each test technique. Dwell time can be set to between 10ms to 120s.

Test Setup

Test setup was extremely fast. Within 10 minutes, the Touch 1 was unpacked, connected to the AV&V wire harness, and successfully conducted a self-learn. The resulting wire list from the self-

learn option can be copied to a floppy disk for off-line work on a desk-top PC or viewed and edited on the Touch1 3.5 x 4.5 graphical touch screen.

Test preparation: Cirris fabricated a total of two test adapter cables that connected the Touch 1 to the AV&V wire harness. Each adapter cable had a Shielded .050 D type connector for the MPT connection , and a GFE connector for the AV&V wire harness connection. The time required to fabricated and ring-out these adapter cables was approximately 1 man-day.

Cirris did not manually create a wire list from the AV&V. The net list created with the self-learn option allow with a library of per-defined test scripts allowed a quick (less that 2 minutes) creation of a test procedure program for the AV&V wire harness.

Special Features

The Cirris SPC Link software application is used to develop test procedures, collect statistical process control (SPC) data, and retrieve this data in ASCII text file format for use in an external data analysis tool. SPC can also be utilized to receive wire list data from CDF&TDS and automatically generate test procedures.

Test Conclusions

Overall, the Touch 1 was found to be an extremely compact and well-packaged system and successfully demonstrated full self-learn, continuity, isolation, and DC DWV functions. Offline test programs can be developed on a desktop computer utilizing Cirris s SPC Link software package and copied to floppy disk that can be loaded in the Touch 1

The Touch1 successfully executed continuity, isolation, and DC DWV test in less than 3 minutes. This system was found to be extremely well packaged, but some what limited to a small number (1024) of test points. It can easily be used as a portable system that could be carried on the Orbiter for wire testing.

Vendor Contacts

Cirris Systems	Richard Chamberland	(800) 441-9910	http://www.cirris.com

CK Technologies

Test Equipment Description

The Model CKT1175is a multiple buss switching system architecture that consist of two basic units: The Control console unit and the switching system unit. Dimensions and weight of the two units are: Control unit: 22 w x 12.25 h x 18.75 d and 70.5 lbs.; Switching unit: 17.8 w x 12.25 h x 18.75 d and 50.5 lbs.

The CKT1175 can be configured to test up to 96,000 points per Control Console configuration. For large system multiple Control Console configurations can be utilized. The CKT1175 can execute either low voltage, (0.25VDC to 28VDC) or high voltage, 0.25VDC to 1500VDC test techniques. It is programmable for current from 2.5µA to 10A.

The CKT1175 measurement sensitivity for connection resistance is 1Ω to 500Ω +/- 0.3mΩ,, for 4-Wire Resistance: 0.01 to 50Ω +/-1mΩ; for High Voltage Insulation Resistance: 10Ω to 500KΩ +/-1%, or 10KΩ to 100MΩ +/-2%, or 100MΩ to 1GΩ +/-5%; and for capacitance: 5nF to 100µF+/-10% +/-0.02nF (relative measurements to 10pF).

The CKT1175 switching module dwell time is programmable for each test technique. Dwell time can be set to between 1ms to 1,000 seconds in 1mS steps.

Test Setup

The test setup, consisting of unpacking the ATE system (CKT1175)—control unit and switching unit — connecting the CKT1175 to a PC, and connecting the AV&V wire harness, took approximately 30 minutes. Once connected, the system conducted a self-learn on the AV&V wire harness in approximately 3 minutes. The resulting wire list can be used to generate a test procedure or be edited and used to generate a test procedure.

Test Preparation: CK technologies fabricated a total of six test adapter cables that connected the model MPT to the AV&V wire harness. Each adapter cable had a DB-50 connector for the CKT1175 connection, and a GFE connector for the AV&V wire harness connection. The time required to fabricate and ring-out these adapter cables was approximately 1 man-day.

CK Technologies manually entered the expected wire list utilizing the AV&V wire harness drawing. The wire list can be used to auto-generated a test procedure program or to validate the resulting wire list created from the self-learn function. During the demonstration, the manually entered wire list was used to validate the self-learned created wire list. The time required to manually enter the wire list was approximately 0.5 man-hour. It should be noted that in place of manual entry, the CK Technologies software package AWARE can be configured to import wire data directly from a known good database such as CDF&TDS.

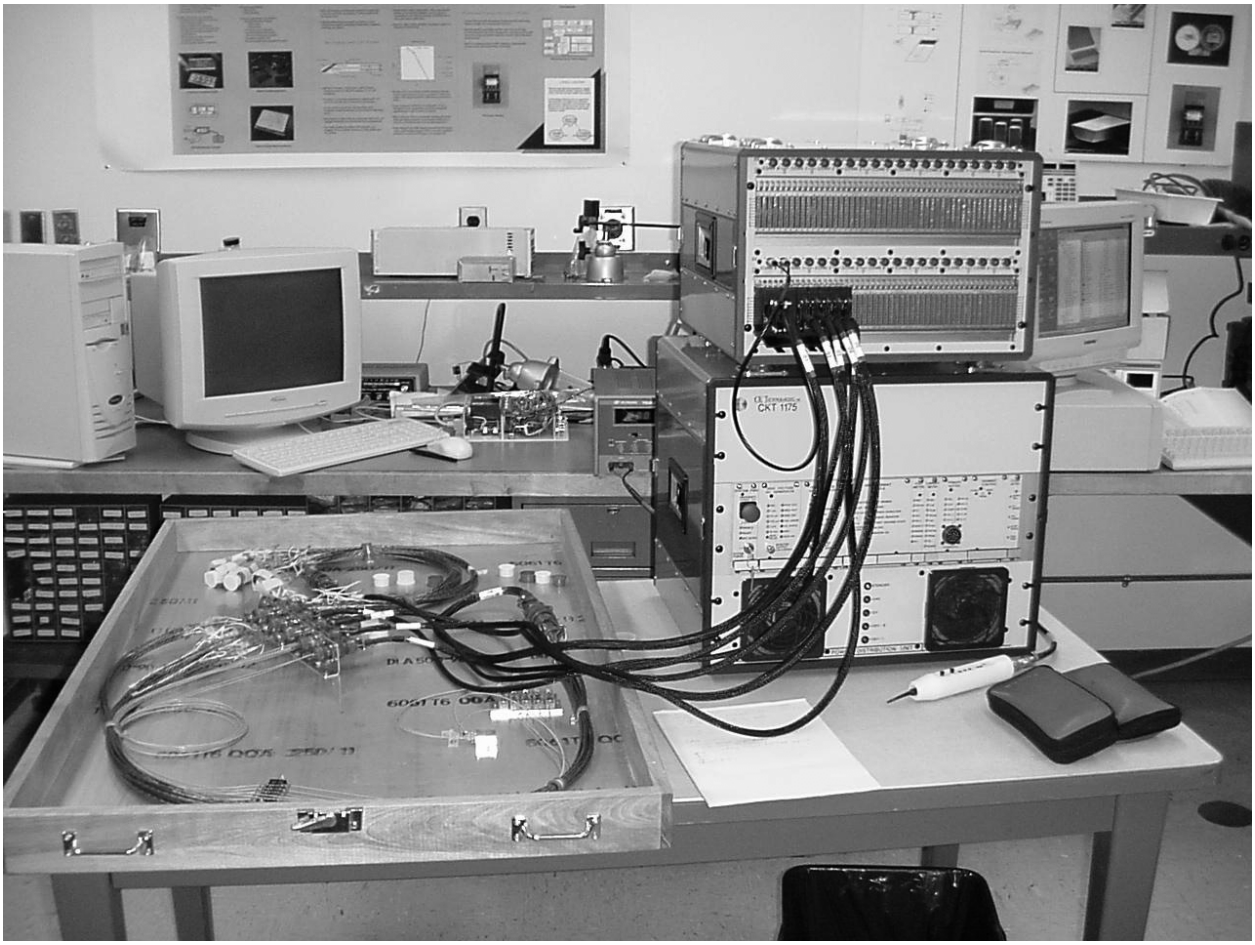

Figure 15. CK Technologies Demonstrates Its ATE on the Test Bed.

Special Features

The CK Technologies AWARE software application was found to be the most user-friendly tool to import wire list and generate test procedures. This application has many features that go beyond the needs of a project such as the Orbiter. Features include auto-generation of the parts list, connect list, wire list, and test setup hookup instruction. This application seems promising and it is recommended that it be purchased to evaluate complete test functions including automatic test procedure generation from CDF&TDS.

CK Technologies is the only ATE vendor that had a product with capabilities to program the ramp rate for Insulation Resistance Testing.

Test Conclusions

Overall the CKT1175 was found to be a very robust and user-friendly ATE system. The system executed the array of standard test (continuity, isolation, and DC DWV) in approximately 2 minutes. This system is big and heavy and can not be considered a portable unit.

The AWARE software application has many features that are beyond the needs of an existing project such as the Orbiter. Features include auto-generation of part list, connect list, wire list, and test setup hookup instruction. This application ability to import external wire list data to automate the test setup phase seems promising and it is recommended that this package be purchased to evaluate these test functions.

Vendor Contacts

CK Technologies	Karl Zimmerman	805-498-6787	http://www.ckt.com
	Jonathan Bruer	805-498-6787	

DIT-MCO

Test Equipment Description

The Model 2115 is a benchtop 1500 Volt model that is currently being used at Palmdale to bench-check Orbiter wire harnesses. The Palmdale model 2115 has been mounted on a movable chart so it can be positioned near the Orbiter to conduct wire harnesses testing on the vehicle. Palmdale also recently purchased a DIT-MCO model 2508 to be used to check complex large wire harnesses. Dimensions and weight of the 2115 are: 1) Main unit: 23.75 W x 11.87 H x 20.5 D and 98 lbs. (1000 test points); and 2) External Test Unit: 11.8 W x 11.87 H x 20.5 D and 55lbs.

The Model 2115 can be configured to test from 1,000 to 5,000 test points. The 2115 can execute Low Voltage testing. (0.225VDC to 29.75VDC); High Voltage testing (30VDC to 2000VDC); and constant current testing 5mA to 2A.

The model 2115 measurement sensitivity is: for connection resistance: 100Kto 9.99MΩ +/- 3%; for High Voltage Insulation Resistance: 500M to 1000MΩ +/-1%.; DC dielectric (DWV) testing —250 to 1500VDC at a maximum current of 5.0mA to detect 10 mircoseconds or longer breakdowns or arcs.

The Touch 1 switching module dwell time is programmable for each test technique. Dwell time can be set to between 0.001 to 1638 seconds.

Test Setup

The test setup consisted of unpacking the ATE system (model 2115) main unit and PC, connecting the 2115 to a PC, and connecting the AV&V wire harness took approximately 20 minutes. Once connected, the system conducted a self-learn on the AV&V wire harness in approximately 3 minutes. The resulting wire list can be used to generate a test procedure or be edited and used to generate a test procedure.

Test Preparation: DIT-MCO fabricated a total of 3 test adapter cables that connected the model MPT to the AV&V wire harness. Each adapter cable had a DB-50 connector for the 2115 connection, and a

GFE connector for the AV&V wire harness connection. The time required to fabricate and ring-out the adapter cables was approximately 1 man-day.

DIT-MCO imported a spreadsheet containing the to/from wire list data for the AV&V wire harness. Using the DIT-MCO software application WIRESORT, the wire list was generated from the imported wire list data. The time required to import the wire list data and generate the wire list was approximately 10 man-minutes. It should be noted that most of the 10 minutes was used to manually re-format the spreadsheet data. The auto-translator could be developed to reduce the amount of time to less that 1 minute. The wire list could be used to auto-generate a test procedure.

An alternative method of generating a test procedure is the self-learn method. The self-learn method function was completed in approximately 2 minutes. This included both generation of the wire list and creation of a test procedure.

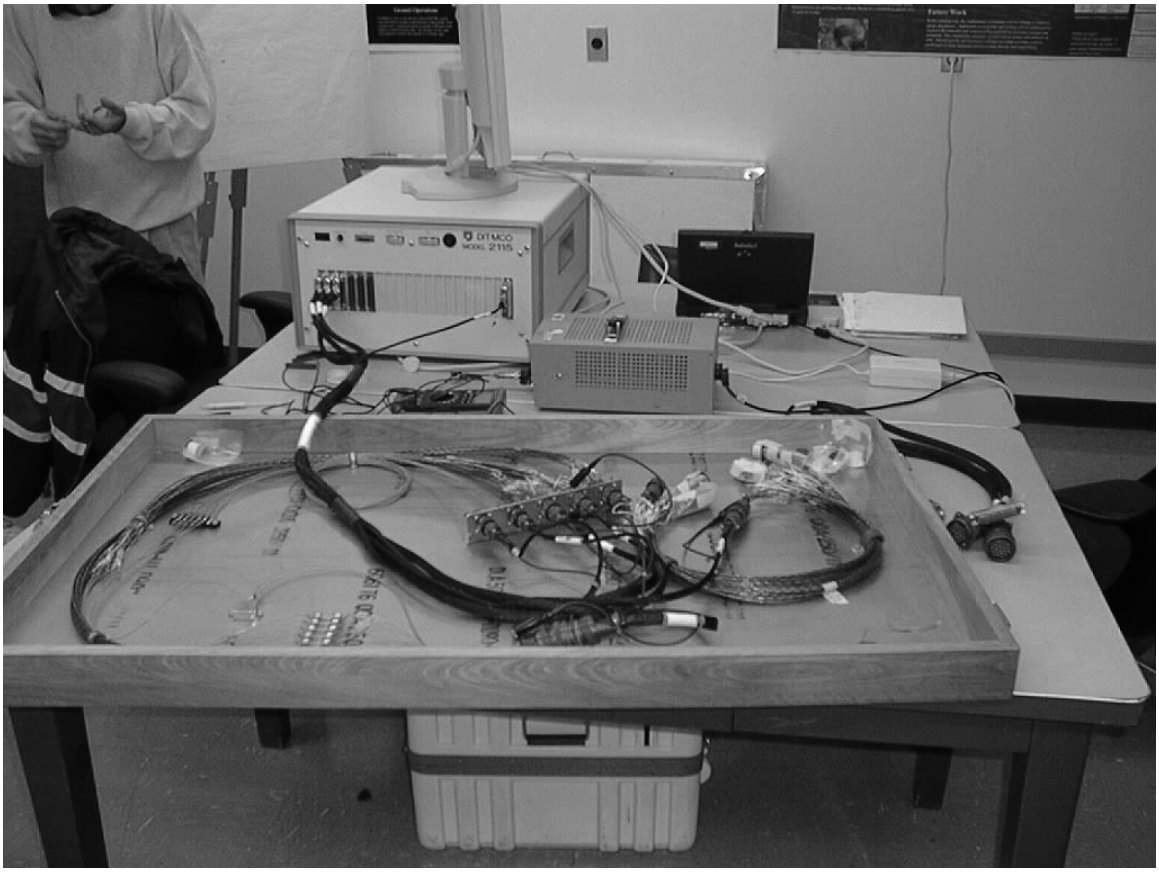

Figure. 16. DIT-MCO Demonstrates Its ATE on the Test Bed.

Special Features

DIT-MCO has several software applications for development and execution of test procedures. Test program development features include a TestEdit application, which provides easy GUI windows to create test procedures, and Self-Programming application, which utilizes the TESTExecutive software to create a test program using a known good wire harness.

DIT-MCO can also interface with GRCI Multilinx to present the learned wire harness in a graphical format.

It should be noted that the results of self-learn can not detect intermediate connections.

Relays and fuses are also not detected during a self-learn exercise. In a complex wire harness with multiple intermediate connectors, such as on the Orbiter, results of self-learn may be limited.

Overall DIT-MCO has a proven, complete ATE system. DIT-MCO systems have been most commonly used ATE system within the aerospace industry. These systems were used during all phases of fabrication of the Orbiter. Boeing Palmdale has recently purchased two new DIT-MCO systems —model 2115 and model 2508.

Test Conclusions

DIT-MCO demonstration of the model 2115 demonstrated a complete Automatic Test Equipment system. Features included continuity, isolation, and DWV testing . The complete array of test took approximately 2 minutes to complete. All measured data were archived in an ASCII file that could easily be exported to third party data analysis tools.

DIT-MCO software applications appear to be extremely versatile and user-friendly. The demonstration of the ability of importing spreadsheet of wire data from a source such as CDF & TDS to generate test program could be extremely useful for the Orbiter.

Vendor Contacts

DIT-MCO	Charlie Jennings	609-268-7312	http://www.ditmco.com
	Tracy Brown	909-357-4803	

Wire Integrity Assessment Test Bed Demonstrations

Boeing

Test Equipment Description

HP4194A Phase Gain Analyzer with Labview interface

Test Technology Employed

Standing Wave Ratio. The Phase Gain Analyzer was used to send a 1 volt swept sine wave over a range of 100Hz to 40MHz, typically taking less than 10 seconds per conductor, and the resulting current was measured. On the display, the x-axis read frequency and the y-axis impedance.

Test Setup

The 22 gauge WIRe Integrity Test Bed was utilized. Connections were made using test leads, and data read through a Labview interface, storing 400 data points over the frequency range.

Special Features

The distinguishing characteristic of the Boeing testing tool is the analysis ability. They have not yet provided their analysis of our test bed.

Test Conclusions

Not yet available.

Vendor Contacts

Dan Rogovin, Boeing

Martin Kendig, Senior Scientist, Rockwell Science Center, 805 373-4241, mwkendig@rsc.rockwell.com

CM Technologies

Test Equipment Description

High Resolution TDR on card in PC

Test Technology Employed

High resolution TDR, DWV, Lumped Capacitance, DC and AC Resistance, Reactance, Polarization Ratio

Test Setup

Both the 12 and 22 gauge Integrity Test Beds were utilized. Test setup was by test leads to individual wires, sometimes jumping together all of the pins other than the one being examined.

Special Features

TDR card in a PC.

Evaluation based on measurement of multiple characteristics of the wire.

Test Conclusions

Interpretation of the test requires a knowledgeable operator. The combination of multiple test characteristics of the conductor was unique to CM Technologies. This technique has been demonstrated to successfully detect smal defects.

Vendor Contacts

Sheldon Lefkowicz, CM Technologies

Cirrus

Test Equipment Description

Cirris 1500V Touch 1 tester, capable of DWV and various other measurements, with switching capability

Tektronix DMD53, Digital Multimeter

Innovative devices built up on short notice: inflatable conductive gas confinement device, electrical contact brush for conductive fluid

Test Technology Employed

DWV

DWV with inert gas

Conductive liquid with DMD53 in capacitance mode, measuring AC resistance

Test Setup

Both the 12 and 22 gauge Integrity Test Beds were utilized. Cirris Touch 1 tester was used to cycle through the conductors, using an adapter harness and connector to mate with one end of the Test Bed wiring harness.

An inflatable conductive enclosure with a helium atmosphere, connected to ground on the Touch 1 tester, was used in DWV mode. The DWV voltage was cycled through the various conductors and easily identified a wire with a very small nick. With an air atmosphere, this nick was not identifiable.

As a second test, a small metal handled brush was used as a probe(wetted with deionized water with 20ppm NaCl) and run over the section of wire with the same very small defect. (It is possible that the water might be replaced with an ionized gas). The nick was easily identified.

Special Features

Enhanced ability to detect very small wiring defects because of the much lower breakdown voltage of the Helium used inside the conductive cover.

Wet electrical contact brush.

Test Conclusions

Easily found very small defects using either technique. Minimal water was used because of the brush technique employed. It would not, however, be possible to get to the center of a wire bundle with water using this technique.

Vendor Contacts

Richard Chamberland

Cirris Systems Corporation

1991 Parkway Blvd.

Salt Lake City, Utah 84119

801 973-4600 x638

Paul Smith

Cirris Systems Corporation

Eclypse

Test Equipment Description

Handheld proprietary SWR unit as developed by Dynacs Co., Inc.

Test Technology Employed

SWR (owned by NASA)

Test Setup

Tested the 12 gauge Integrity Test Bed, using individual test leads connected to two pins at a time. No automation.

Special Features

Handheld unit, simple direct readout of fault type and distance to fault (after calibration for wire characteristics).

Test Conclusions

Successfully identified the two faults (one short, one open) in the harness, and found the length of the good wires in the test bed.

Vendor Contacts:

Chris Teal, (909) 947-8839 x30, cteal@eclypse.org

Alan Fergusen, (909) 947-8839

Appendix 7 – Tools Evaluated for Test Management

Seven software packages were investigated during this study. The purpose was to determine the capabilities of current CAD tool features relevant to Shuttle Orbiter wire design in conjunction with test management and risk analysis. The number of CAD packages available is large compared to the number mentioned in this report, but the WIRe-relevant features of each is similar to those listed here. This selection is not meant to imply a preference of one brand over another.

Software Packages Evaluated

Name	Main Purpose	Source
TEAMS	Test Sequencing and "Design for Testability" Analysis	Qualtech Systems, Inc.
MultiLinx	(Multidiscipline) System Architecture and Integration Modeling	GRC International, Inc.
WireWorks	Design and Documentation of Electrical Power and Control Systems	Intergraph Corp.
Wiring-CAD (WCAD)	Design and Documentation of Electrical Wiring with Specific Customizations for Shuttle (Modified LogicalCable)	Mentor Graphics/Boeing
Promis•E	Design and Documentation of Electrical Power and Control Systems	ECT International, Inc.
SCAN	Trusted Database of Current Wiring Configuration and Connector Mate/Demate Status for Shuttle Orbiters	NASA
CDF&TDS	Database of Wiring Designs for Shuttle Orbiters	NASA

Table 7. Purposes of CAD Packages Evaluated.

Because Orbiter wiring design is static, changes to front-end CAD tools will have minimal impact on automated wire integrity testing capabilities. The data relevant to automated wire testing has already been captured in Circuit Design, Fabrication and Test Data System (CDF&TDS) and Shuttle Connector Analysis Network (SCAN). These databases are the first point in the design process where the data represents the entire Orbiter in a digital format. Prior to entry in CDF&TDS and SCAN, the data are stored either digitally or on paper. Unfortunately, most of the design is on paper. The non-static designs, mostly consisting of payloads and their Shuttle/payload interfaces, are most likely to

have been converted to digital data. Although estimating the cost of digitization of the entire Shuttle is the responsibility of another DFS study called Digital Shuttle , the cost can be assumed to be high in terms of both money and effort. Therefore, modifications to the front-end CAD tools will not have a system-wide impact on the Shuttle design process.

Boeing Reusable Space Systems (BRSS) is using Wiring-CAD (WCAD), a modified version of Mentor Graphics Logical Cable (L-Cable) for Payloads wiring design. They have a continuing collaboration with Mentor Graphics, enhancing the capabilities of the software, focusing specifically on Shuttle design requirements. Part of BRSS s software choice was based on L-Cable s ability to share data with CATIA, which is used by BRSS for 3D mechanical design. Of the various CAD packages surveyed, W-CAD is most likely to improve the efficiency of the Shuttle wire design process with the least impact to budgets and current design efforts. For this reason, Boeing/Mentor Graphics should be encouraged to continue work on W-CAD, although the results of this study show that more benefits to automated wire testing can be gained by adding tools to work with SCAN data instead of upgrading front-end CAD tools.

Products	TEAMS	MultiLinx	WireWorks	WCAD	Promis-E	SCAN	CDF&TDS
Feature							
Automatic Test Generation		X					
% Test Coverage Analysis	X						
Trend Analysis	X	3					
Test Results Archive	X	X					
Fault Propagation Analysis	X	X					
Automated/Assisted Harness Cascade		4		X			
Design Output: Drawings		X	X	X	X		
Design Output: Lists, Reports*		X	X	X	X	X	X
Component Detailed Definition		X	X	X	X	X	X
Database Accessible (API)	X	X	X	X	X	X	X
Design Import from Test Data (AutoLearn)				1			
Design Import from Old STS Doc System				1			
Wiring Design Automation Tools			X	X	X		
Rules-Based Design Checking		X		X			X
In-Use on current Shuffle work				X		X	X
Handles Multiple Configurations		X	2	2		X	

Table 8. CAD/Analysis Software Capability. Many features are not currently available in some products, but can be added if requested/funded by the customer.

*** Typically, ASCII formatted wire lists are used to generate test programs. [1] Manually assisted, not fully automated. [2] Handles variants and options, but PDM recommended for Shuttle Program use.**

[3] Can chart results. Analysis requirements not specified. [4] Can do "Copper Path" Tracing

Features of Interest

Automatic Test Generation

Automated Test Equipment (ATE) typically comes with software to generate test programs automatically from ASCII wire lists. A simple harness wire list can be generated from every package examined in this study. However, additional intelligence is necessary to generate an appropriate wire list for an end-to-end test of installed harnesses. The software must be able to trace the wire paths through the system to be tested from harness to harness to generate the end connector pin mappings. Also, the various test modes should be included in the program with some intelligence feature. For instance, not all wires can be tested at high voltage. Some wires may lead to components that should not be exposed to any automated testing. The CAD/Analysis tool sending the data to the program generator needs to have all of the rules built-in.

Percent Test Coverage Analysis

Not all wiring in the Orbiter is appropriate for automated testing. Therefore, a tool to determine the amount of test coverage for a given series of tests would be highly desirable. Also, the ability to optimize for the fewest or easiest test procedures that give the highest coverage would decrease the cost of testing.

Trend Analysis

Test results need to be archived, so data comparisons can be made. The test outputs yield pass/fail information but can also show the actual tested values. By comparing the results from several tests over time, it may be possible to predict some failures. If testing is not done in exactly the same way each time, trending will not be relevant, so if new test procedures were generated each test run, this feature would be less important. A standardized set of test procedures would be necessary.

Fault Propagation Analysis (FPA)

Having a system-aware tool that can do Fault Propagation Analysis (FPA) will ensure that a standard FPA is generated for the incorporation of any design into the Orbiter. The FPA capability can also be used to generate diagnostic trees to facilitate troubleshooting of any wiring anomalies.

Automated/Assisted Harness Cascade

Tracing a signal path from wire to wire through a series of harnesses is a necessary activity when developing a test program because the test program must be configured based on the connector/pin arrangement at each end. For automated testing, the ability to trace all paths from an entire connector is desired. The ability to step through the harness fan-out, level by level, can assist in determining appropriate end connectors for testing purposes. For full automation, the capability to generate test programs for a list of accessible end connectors is desired.

Design Output: Lists, Reports, Drawings

These standard design deliverables are available in some form from every application surveyed. Typically, ASCII formatted wire lists are used to generate test programs, so the tool associated with test program generation should have this output capability.

Component Detailed Definition

Front-end CAD tools may not need to have specific part information in order to generate a schematic, but the detailed part data needs to be defined at some point so that tools downstream in the design flow will have complete information for system analysis.

Accessible Database

The detailed part information needs to be accessible in formats that may not be standard in the CAD package. If the database is accessible, then custom data extraction can be developed as needed for automation.

Design Import from Test Data (Autolearn)

If sufficient information can be derived from Autolearn data to generate schematics, then digitization of current designs can be accomplished using existing hardware, instead of painstakingly transferring designs from paper drawings to CAD. Unfortunately, very little detail can be gleaned from test data besides end connector pin continuity, and even that has some inherent ambiguities. Therefore, this feature has little practical value. Significant human input is still necessary.

Design Import from Legacy Documentation

The ability to import designs from legacy documentation would allow for quick digitization from paper media. As for existing digital data, BRSS s W-CAD has a custom tool to extract data from CDF&TDS. However, the thousands of paper sheets of integrated schematics would have to be hand-entered.

Wiring Design Automation Tools

Component libraries, the ability to drag and drop components into a schematic, smart wires that know to move with the attached component when rearranging the schematic, and tools to auto-arrange components for ease of viewing are all design automation tools that make wiring design quicker and easier. Choosing a CAD package without these would offset any automatic wire test capabilities by decreasing design productivity.

Rules-Based Design Checking

This capability constrains the design to specific standards and prevents the designer from making mistakes such as assigning incompatible connector mates or choosing the wrong type of wire. The presence of this capability implies that rules could be added to improve testability of the design.

Effectivity/Configuration Management

Managing Effectivity involves configuration management of not only the design but also every serialized variation and instance of the design. In the Shuttle case, every Orbiter variation must be uniquely tracked, as well as every variable system within each Orbiter. For testing purposes, this allows for tracking the test history of each component and determining the correct test procedure for the specific Orbiter harness(Es).

In-Use for Shuttle Development

CAD tools that are already in use for Shuttle design do not require significant initial monetary investment. The money has already been spent, and the personnel are already familiar with the software. Any existing customizations made to the software are Shuttle-specific investments. They increase its suitability for Shuttle design when compared to more generic CAD packages.

QSI TEAMS

Evaluation of TEAMS for Test Management

Qualtech Systems, Inc. performed a study to determine the feasibility of automatically creating a model for a subset of the Shuttle wiring that would contain the necessary information to diagnose and repair wiring problems within the entire Shuttle. The TEAMS product consists of a set of software tools for test sequencing and design for testability analysis in complex systems, real-time monitoring and diagnostics, as well as maintenance support through the use of a portable maintenance aid. TEAMS uses a cause-effect modeling strategy called multi-signal flow graphs that relates the fault propagation through a system, failure attributes, system function, and monitoring points in a hierarchical model that can be graphically derived. The model can be analyzed to quantify the testability of a system, which is a measure of the extent to which a system can be tested for the presence of failures. A highly testable system implies a high degree of fault coverage and fault isolation, as well as shorter testing times and lower life-cycle costs. The models also support generation of an FMECA and reliability measures, which can support the assessment of risk for the system.

The MEC1 subsystem was the subject of this study. All of the wiring information required for creating the wiring model was supplied via a Shuttle Connector Analysis Network (SCAN) Electronic wire list. This partial wire list contained all the wiring information relative to the MEC1 assembly. Using this NASA supplied SCAN wire list, QSI concurrently created manual and automatically generated wiring models for all wire paths associated with connector J3 on the MEC1 assembly. This

provided the means to verify that the automatically generated model accurately portrayed the actual Shuttle wiring. Once it was ascertained that the automatically generated model was identical to the one created manually, the wiring model for the remaining Shuttle wiring was automatically created, which would have been a monumental task if done manually.

The approach taken with this model was to create a library of connector and wire types and interconnect them as per the SCAN wire list. The manual wiring model was begun by making some basic assumptions relative to failure modes of components, level of repair, and testing methods.

For failure modes, the following assumptions were made:

- Connector pins
    - Open - caused by pushed or bent pins.
    - High Resistance —possibly caused by corroded pins or poor contact with mating pin.
    - Short (Hard short or Low Impedance) —possibly caused by a bent pin shorting to an adjacent pin or a piece of metal shorting two or more pins.

For level of repair, it was assumed that pins in connectors would be repaired or replaced rather than replacing the entire connector, therefore Open and High Resistance failure modes were modeled as aspects of the connector pin (see Figure 17).

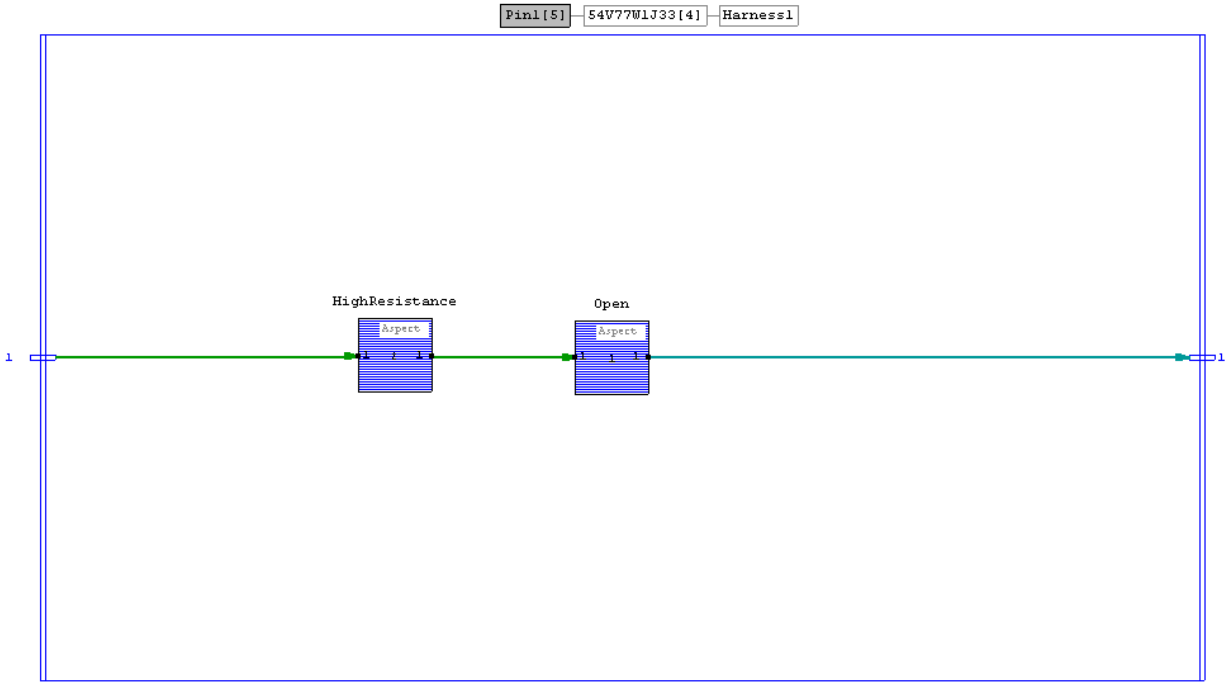

Figure 17. Connector Pin Module.

Should one of these failure modes occur, the connector pin (labeled Component) would be called out. Hard Shorts and Low Impedance shorts were labeled as Component (see Figure 18).

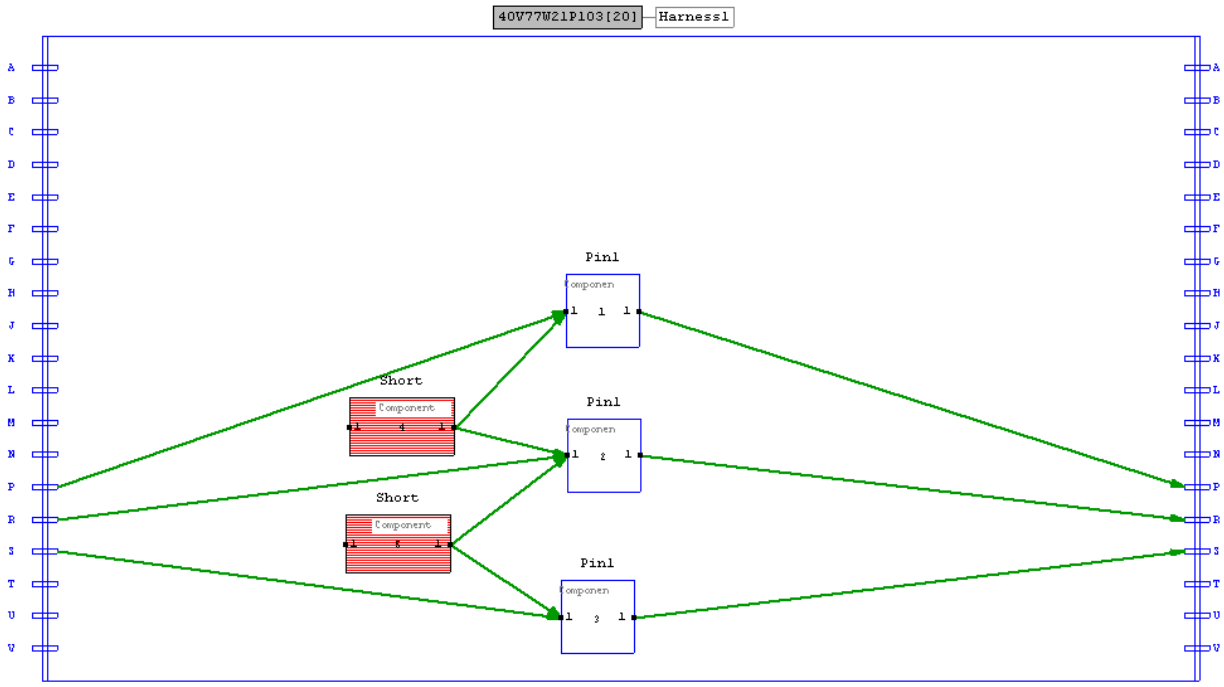

Figure 18. Connector Module.

Should one of these failure modes occur, the short between the two pins would be called out. The model assumes that the connectors are flat edge type and therefore only adjacent pins will short. If physical layout drawings of each connector type were provided, the model could be updated to include any additional adjacent pin shorts.

- Wires
  - Open —broken conductor
  - High resistance —broken or frayed conductor making partial contact
  - Short to ground (Hard short or Low Impedance) —cut in insulation allowing wire to short to ground or make partial short to ground
  - Short to shield (Hard short or Low Impedance) —cut in insulation allowing a shielded wire to short to its shield or make partial short to shield
  - Short between wires (Hard short or Low Impedance) —frayed or cut in insulation allowing two wires to short together or make partial contact

The wires were modeled based on their type (conductor, twisted pair, twisted pair shielded, etc.). A library of modules was created depicting the different wire types as indicated in the SCAN wire list. For wire paths, these wire types were labeled as repairable/replaceable. Wire bundles are uniquely

defined by the Wire Type and Cable Descriptor fields of the database. The wires and their failure modes were placed within these wire type modules. If a wire bundle is comprised of three twisted wires, and one of those wires was to open, the maintainer is instructed to replace all three twisted wires, as it is unlikely he would untwist and replace only the defective wire. The failure modes within each wire type include shorts between any wire pair as well as a short between any wire and shield. Opens and High Resistance failure modes were modeled for each individual wire path (see Figure 19).

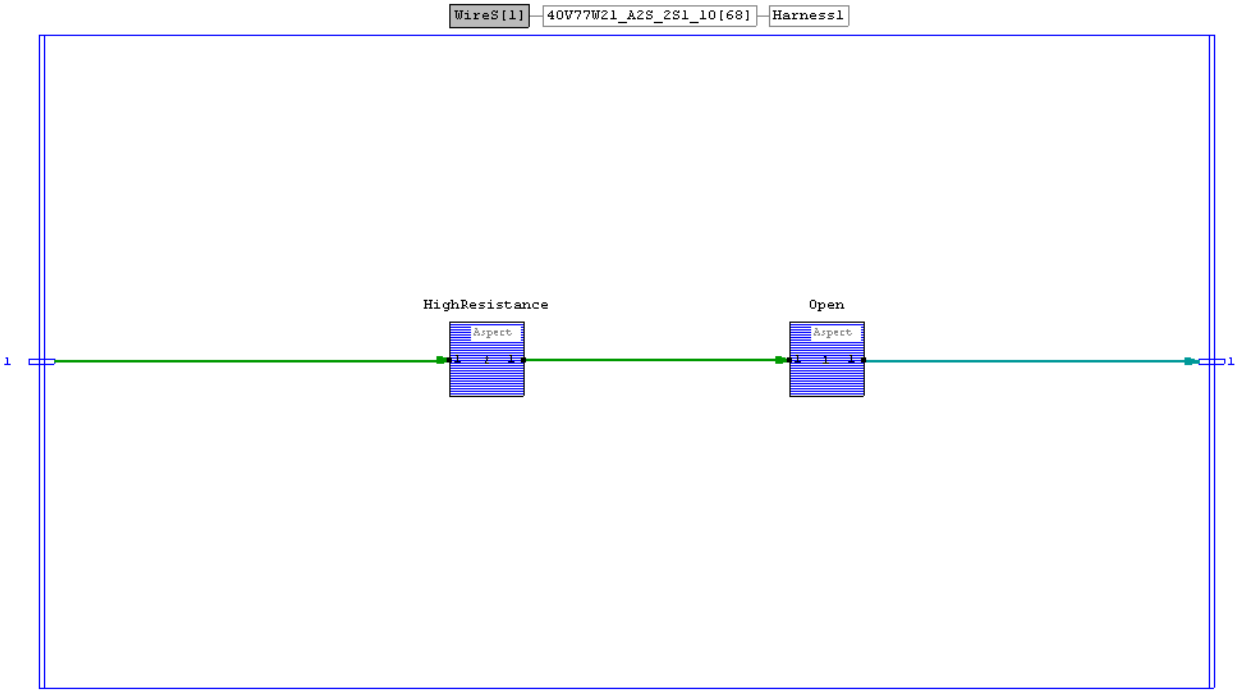

Figure 19. Wire Path Module.

Should one of these aspects fail, the wire bundle (labeled Component) would be called out. The same is true for Hard Shorts and Low Impedance shorts (Figure 20).

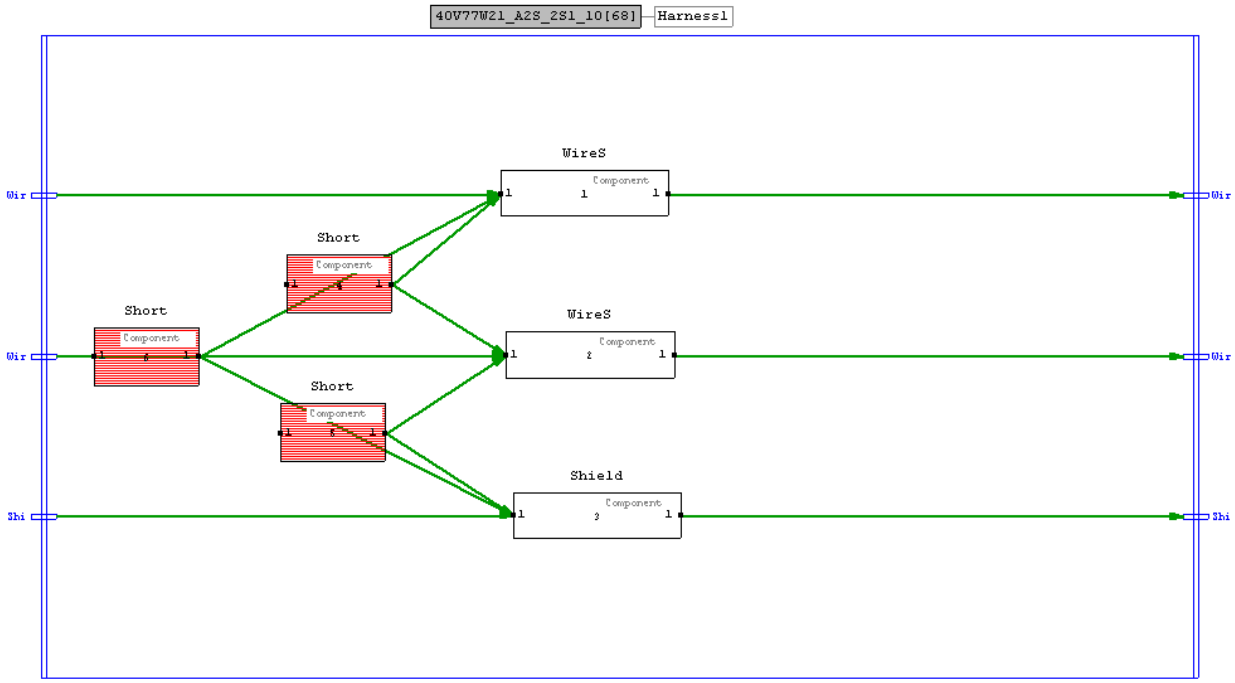

Figure 20. Wire Type Module.

If these assumptions for level of repair are later found to be incorrect, the model can easily be updated. If, for example, it is determined that a particular harness cannot be repaired and must be replaced as an entire assembly, then the repair label of that particular harness would be updated, leaving the previously defined repair labels for the other harnesses intact.

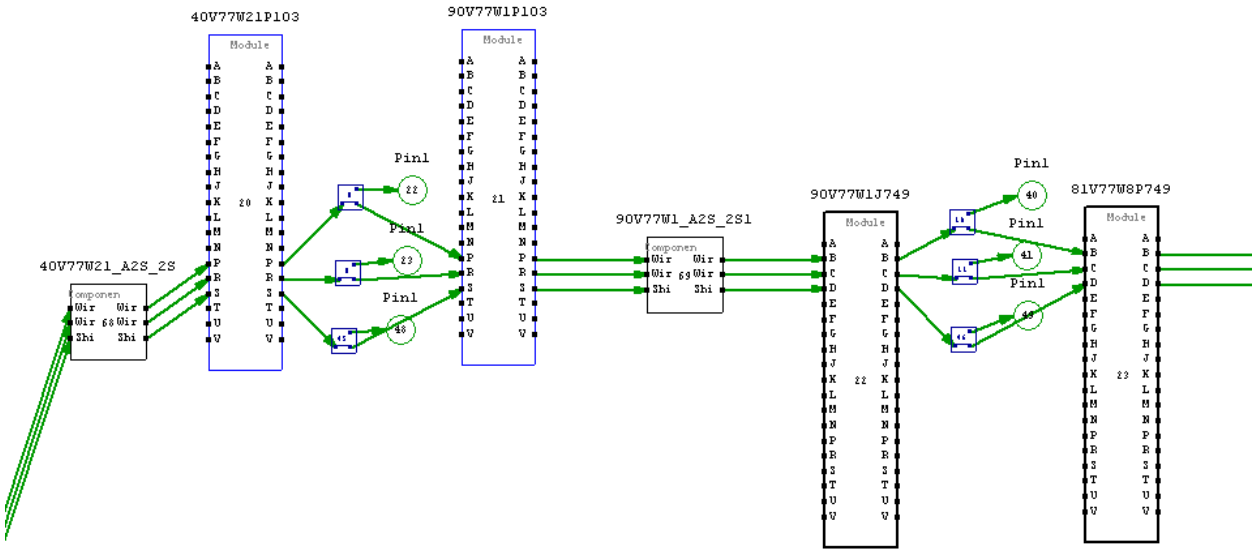

Figure 21. Partial Wiring Harness Model.

Switches were placed on the outputs of each connector (Figure 21). These switches simulated de-mating the connectors from one another. Connectors are de-mated to provide access to test points, which ultimately provide fault isolation. We have created System modes, which should be used when running the analysis. The first one is labeled CompleteHarness . Selecting this mode will simulate all connectors being mated to their mating connector with the exception of the last connector in each wire path. Running the analysis in this mode will generally result in large ambiguity groups caused by the inability to fault isolate paths containing multiple wires and pins. The second system mode we have created is called DisconnectAll . Selecting this mode will simulate all connectors being de-mated, thus allowing testing on the pins of all connectors. Running the analysis in this mode will result in much smaller ambiguity groups. Additional system modes can be defined or changed as needed. If it is known that some connectors in the wiring harness cannot be accessed, then system modes can be defined to allow de-mating of all but these connectors.

The next step was to add all the necessary tests to detect all of the failure modes. The tests defined for this wiring model are as follows:

Continuity —This will detect open wires and open pins

DC Resistance —Involves measuring DC resistance through a wire path. It will detect open wires, open pins, and high resistance paths caused by corroded pins, poor contact with mating pins, and broken or frayed wires making partial contact. It will also detect wires shorted to ground

Complex Impedance —This will detect pin shorts (Hard and Low Impedance) as well as Hard and Low Impedance wire shorts, shorts to ground and shorts to shield.

Noise Figure —This test will check for High Frequency Crosstalk and Loss Attenuation. It will detect high resistance pins and wire paths, low impedance pin and wire shorts, as well as hard shorts in pins and wires

High Voltage —This test will detect high resistance failures in both pins and wires.

The testability analysis produces reports that provide information that can be used to verify the resulting test strategy. The results of the analysis are presented in a number of formats. The first one is the Testability Figures of Merit Summary (TFOMS) Report. The TFOMS Report for this model is illustrated in 22.

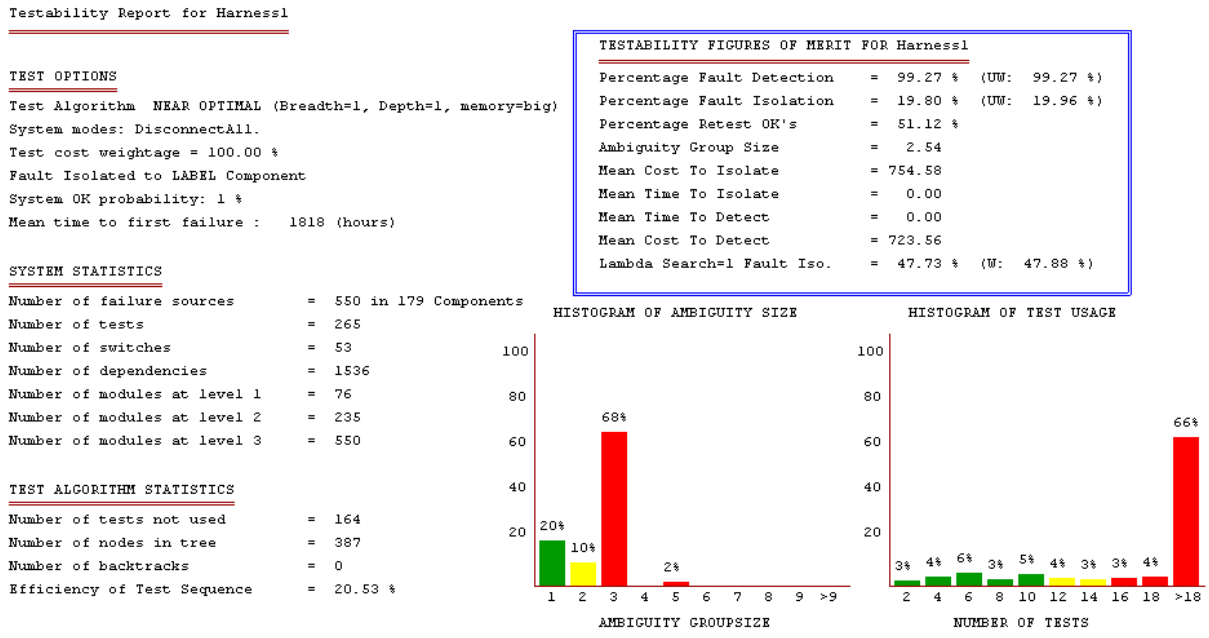

Figure 22. TFOM Summary for the MEC1 J3 Connector Wiring Model.

Under the topic Test Options , there is a list of the options set for the analysis which generated this report. Under System Statistics , a list of model details is provided. The Test Algorithm Statistics topic provides a list of information about the resulting test strategy. The most important bit of information provided by the TFOMS Report is the bar graph entitled Histogram of Ambiguity Size. If the design goal was to fault isolate to an ambiguity group size of two or less components, then it is quickly seen that additional tests still need to be devised that will break up the ambiguity groups of three or more components. The first step necessary to define additional tests is to determine what components comprise these ambiguity groups. This information can be found in the Ambiguity Groups (dynamic) test report. There is a large number of ambiguity groups comprised of three components. This is due to the fact that most wire paths in the sub harnesses are comprised of a wire with a pin at either end. If it was necessary to break this ambiguity further, more tests could be added.

For example, if a Reflectometer were used, isolation to the failure to a single component would be possible.

Figure 23 is an example of a section of an ambiguity group report for the MEC1 J3 connector wiring model. By reviewing the first ambiguity group in the report, which components comprise the ambiguity group of five can be determined. It is the two pins, two wires, and solder splice of a wire path in sub harness 50V77W34.

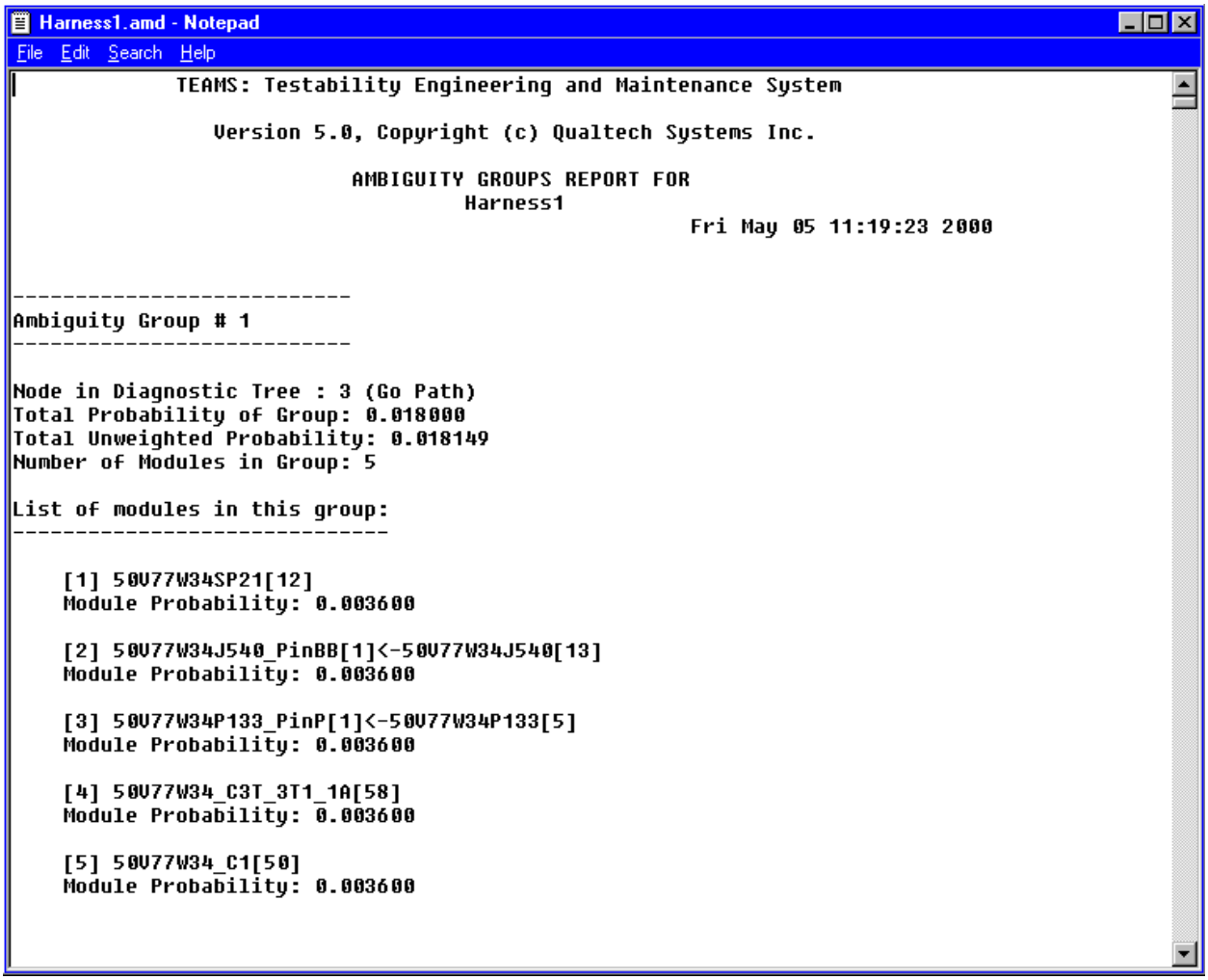

Figure 23 Ambiguity Groups Report for MEC1 J3 Connector Wiring Model.

The diagnostic tree can now be examined to determine if the resulting test strategy seems logical. Figure 24 illustrates a partial view of the diagnostic tree for the MEC1 J3 connector wiring model.

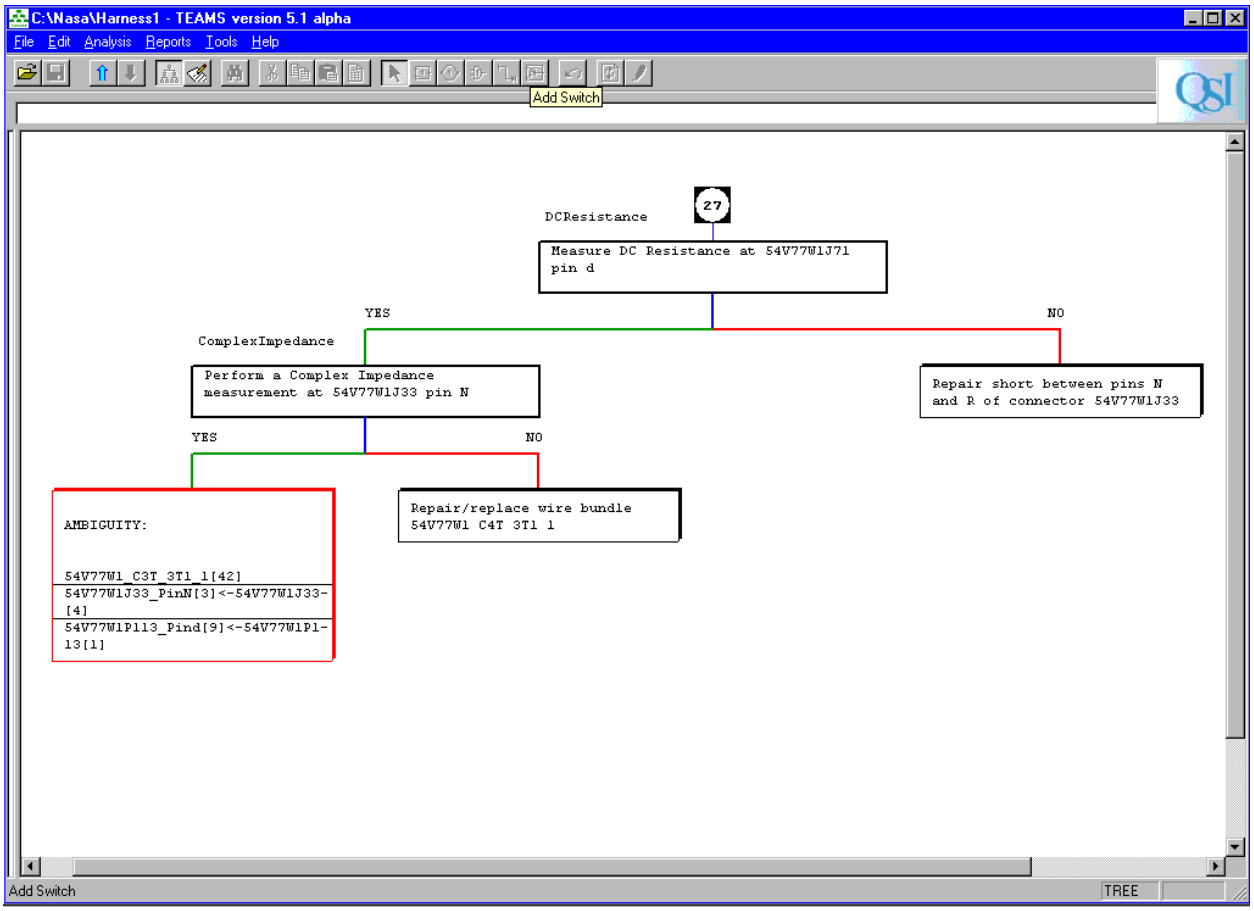

Figure 24. Partial view of Diagnostic Tree for MEC1 J3 Connector Wiring Model.

The diagnostic tree is verified that it correctly isolates failures. If problems are found with the diagnostic strategy, the model should be updated to rectify these problems and the analysis rerun until the analyst is satisfied that the model is producing a valid test strategy.

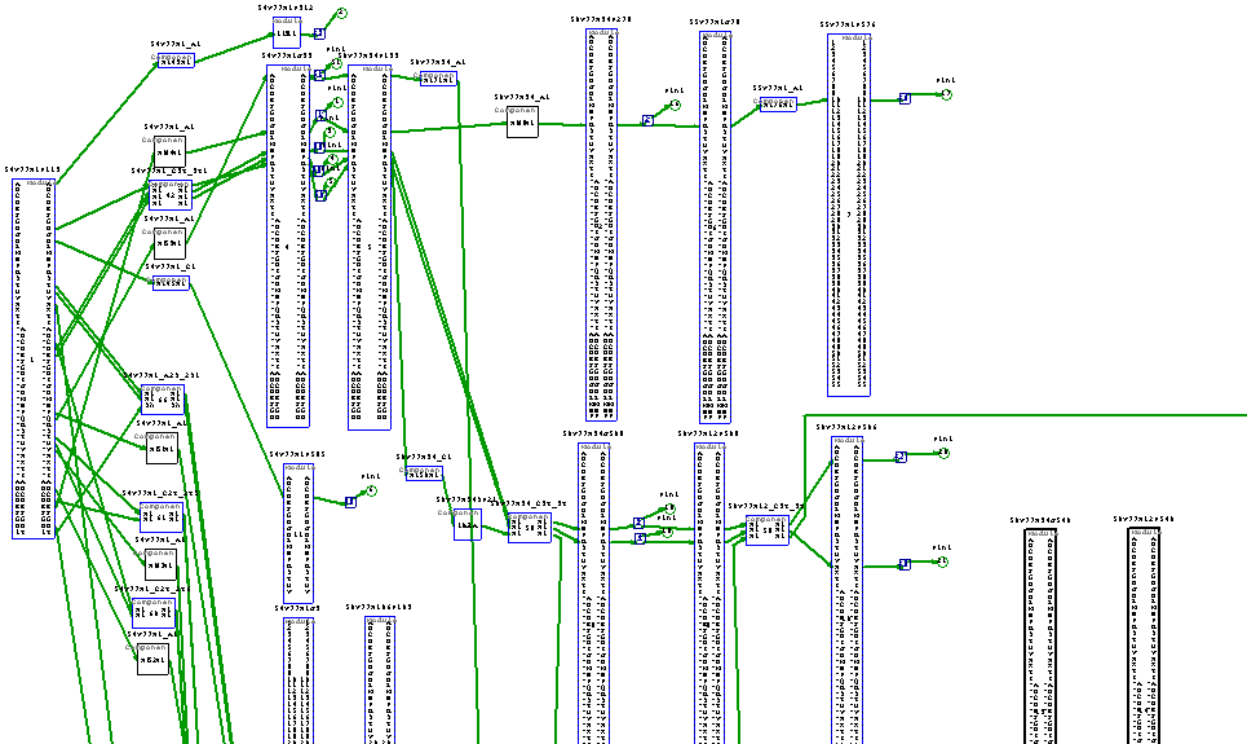

Figure 25. MEC1 J3 Connector Harness Block Diagram.

A partial block diagram of the MEC1 J3 connector harness, as modeled with TEAMS, is depicted in Figure 25. By making some basic assumptions on failure modes and test types, a model representative of a typical wiring circuit was manually created which supplied the necessary information for automatically creating the same model. The resulting model closely resembles the physical structure of the wiring circuit, thus allowing updates to be made quickly and easily. The TEAMS model of the entire MEC1 subsystem was then automatically created from existing data with little or no effort.

These models make a basic assumption that the wiring harnesses are de-mated from the subsystems they interconnect. A more effective way of troubleshooting wiring problems would be to model the subsystems and interconnect them with the wiring harness model. Then, by running tests on the various subsystems, the problem could be partially isolated and the amount of manual harness testing necessary to further isolate the fault would be reduced.

GRC MultiLinx

Using MultiLinx for Test Management

MultiLinx is a system integration and analysis suite of software tools available from GRC International (GRCI). It is currently being used extensively by NASA X-38 and International Space

Station system engineers as a design tool. Functional dependency models are created in MulitiLinx. The model is implemented in an underlying database application 4th Dimension, manufactured by ACI US, Inc. MultiLinx includes a set of static and active component templates, including wire harnesses, connectors, relays, diodes, circuit breakers, switches, and terminal junctions that are used to model electrical interconnectivity hardware architecture. MultiLinx can also self-learn a wire harness configuration, by using the DIT-MCO tester self-learn capability. The MultiLinx harness model can then be used to automatically generate test programs for DIT-MCO Automated Test Equipment (ATE).

The MultiLinx database can store any metrics associated with elements of the model. As an example, you could store capacitance values obtained from a DIT-MCO lumped capacitance measurement for every wire pair, or between a wire and ground. This data can be stored for trend analysis to detect changes that might indicate wire degradation.

MultiLinx s Automatic Test Generator (ATG) module permits the creation of test programs based on the system model. The interconnectivity information captured in the model allows for construction of end-connector wire lists for single harnesses or complicated multi-harness wire-runs. In addition, characteristics have been predefined within MultiLinx for a variety of static and active components such as relays, diodes, circuit breakers, switches, and terminal junctions. Any additional, special-case characteristics can be stored in the individual component descriptions. The ATG module can be set up with default test parameters to meet any NASA specifications for test conditions. Paths and components that are too sensitive to be included in automated testing may be blocked or set to allow isolation tests only. Text files of pre-approved test procedures can be stored in the database and recalled to aid engineers in creation of OMIs. The ATG module was demonstrated with DIT-MCO test equipment, but the development of simlar modules for other test equipment manufacturers is a possibility, if required.

Test results can be stored within the MultiLinx database and recalled for analysis by external tools. Trend analysis within MultiLinx is currently limited to linear-regression curve-fit of historical data. A threshold value may be assigned, and the intersection of the data curve and the threshold line will be noted as a predicted failure date. There are obvious limitations to the usefulness of this simple trend tool with regards to the linear-regression capability, as well and the analysis reliance on the use of the same test program and the same harness configuration. (GRCI does plan on enhancing this capability.)

By keeping track of the pass/fail status of each component/path (with some kind of expiration date), a rough percentage of test coverage can be determined.

Test Bed Evaluation of We asked GRCI to create a MultiLinx model of our Configuration Test Bed. The Configuration Test Bed is described in Appendix 5. The job required 24 hours to model approximately 100 wires, 8 connectors, 180 pins, 30 shields, 16 splices, 5 fuses, and 1 active SPDT relay. In addition, all Interface Test Adapter (ITA) cables, which connected the Test Bed Harness connectors to the DIT-MCO tester were modeled in the MultiLinx datafile. Afterwards, GRCI representatives came to Ames and showed us the model. They also provided training on the creation of the MultiLinx data model, including harness modelling rules, data population, diagram creation, automatic test generation, data archival, and analysis. Then, we had them auto-generate a DIT-MCO

test program from the MultiLinx tool for the Configuration Test Bed. They were able to program the DIT-MCO and to run a continuity and isolation test on the test bed. They also demonstrated the MultiLinx capability for self-learning , and were able to produce a simple wiring diagram based on the self-learned data. The ability to automatically compare and display any differences detected between the model and the self-learned harness-under-test was recommended for future inclusion in the MultiLinx tool.

Entering wire connectivity data manually was a time-consuming process for GRCI. An automated spredsheet input form was used, but no electronic data was made available, and thus had to be manually entered into the spreadsheet. We believe this could be automated so the data would import directly from the CDF&TDS and SCAN databases. GRCI was not asked to develop an import tool during this study.

It is capable of auto-generating wiring diagrams from the wire interconnectivity data; however, the diagrams are very simple and not of high technical quality. The diagram utility can then be used to manually clean up the drawings, and templates (bitmaps and text files) can be used to standardize borders and notes. All components are initially displayed as rectangular objects, and all paths are displayed as line segments. Bitmap objects, as well as graphical images, can be copied and pasted to represent components using standard schematic symbols, but they are not currently linked with their corresponding component (future enhancement). The layout of additional component data is highly configurable in terms of location, selection, and format, increasing the usefulness of the resulting diagram.

GRCI successfully demonstrated the use of MultiLinx for auto-generating a test program. A DIT-MCO Model 2115 tester was programmed to do continuity and isolation testing of the WIRe Configuration Test Bed. The Configuration Test Bed included a SPDT relay, and a set of fuses of different values. GRCI demonstrated a MultiLinx feature that successfully switched the relay, energizing it for testing both paths of the switched circuit. They also were able to add a feature to MultiLinx that lets the user specify a value for limiting the test currents, so the circuit paths with fuses could be tested without fusing.

GRCI was not asked to implement the MultiLinx FPA capability with the WIRe testbed model. During the initial software demonstration, preliminary documentation was presented that indicated the single-point failure analysis had been expanded to as many as three failure sources. The capabilities of the MultiLinx FPA application are still being refined and enhanced. Therefore following discussion of capabilities is based on the preliminary documentation and may differ from the released version.

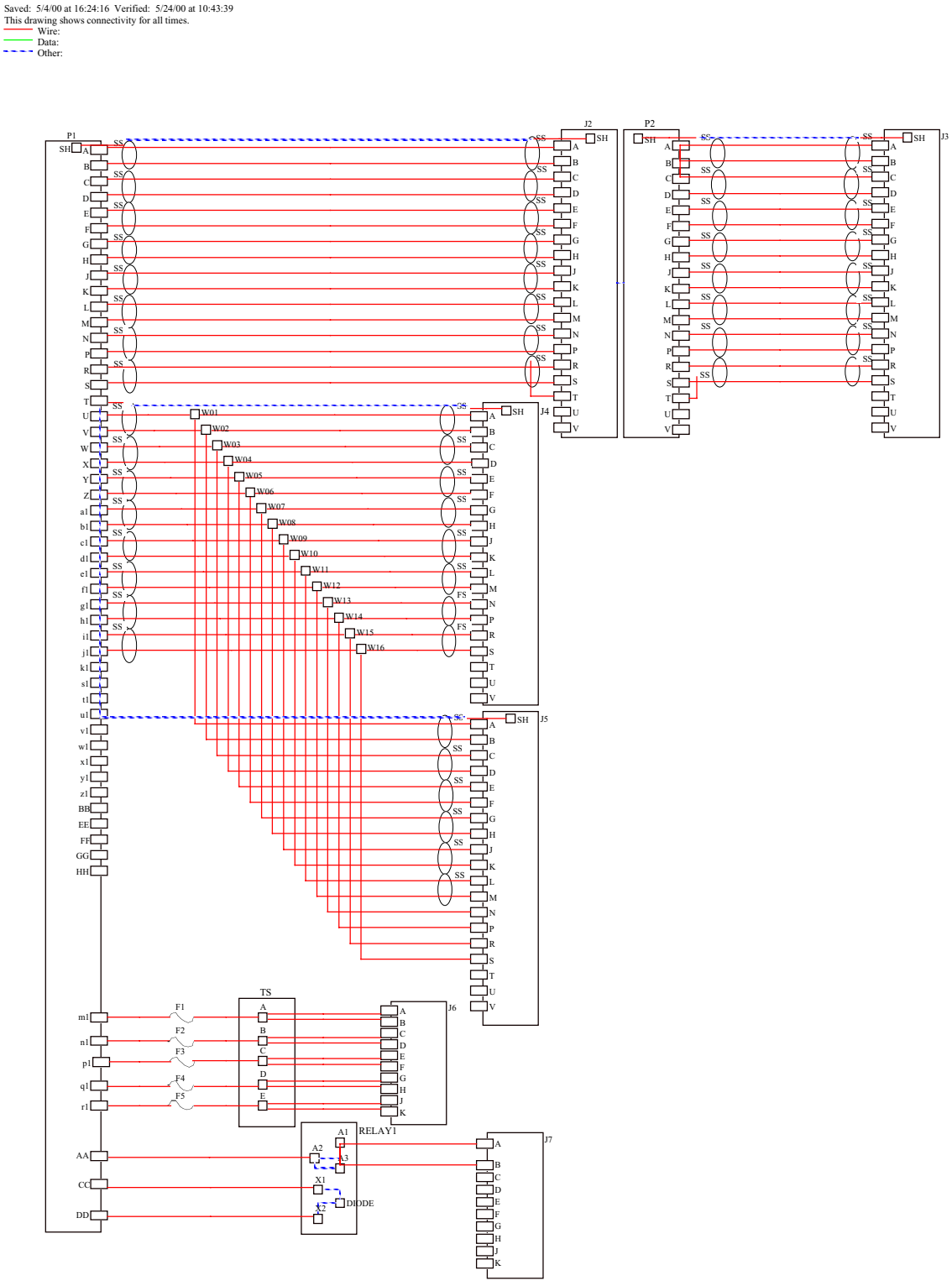

Figure 26. AV&V Test Bed Wiring Diagram Automatically Generated by MultiLinx.

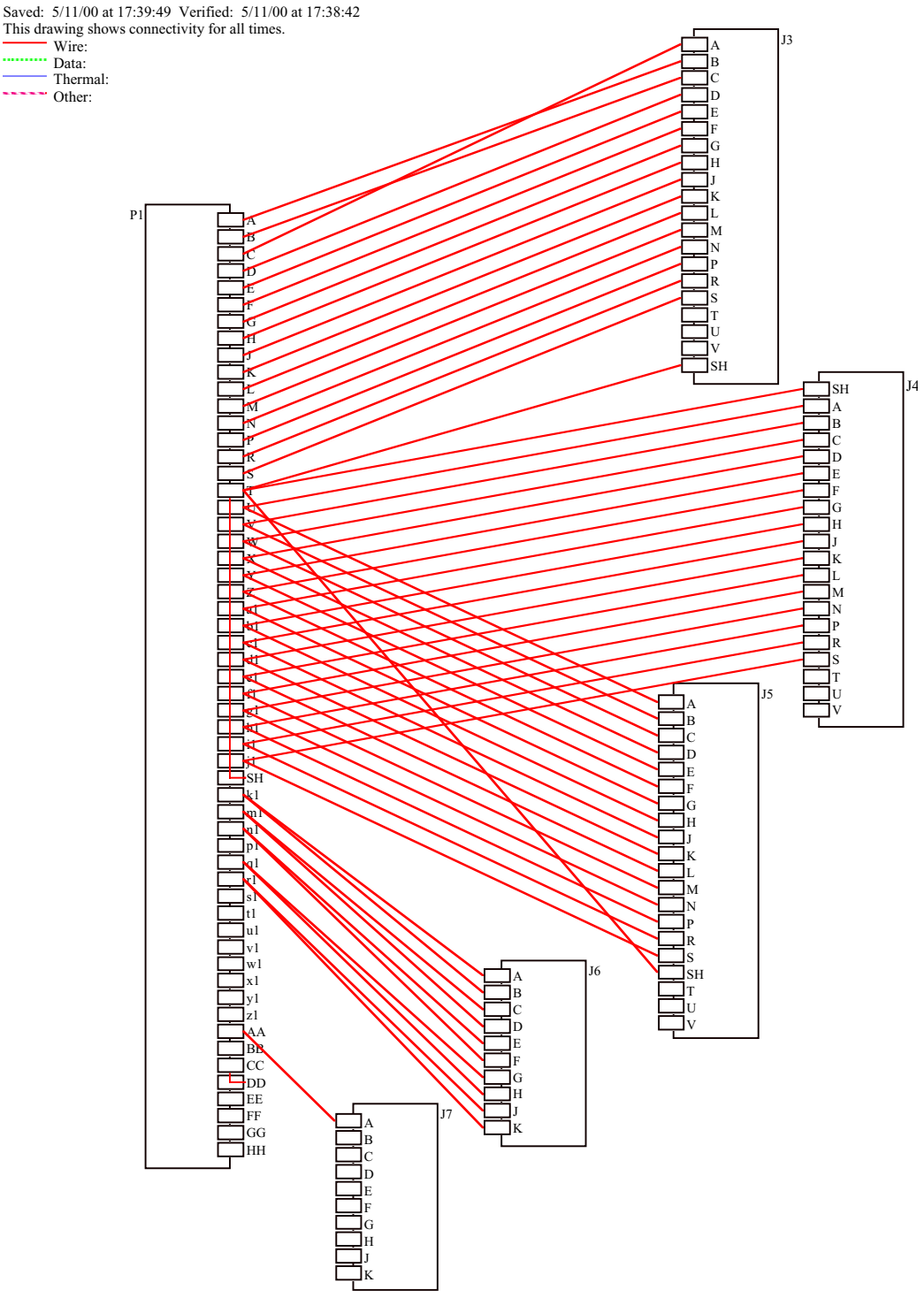

Figure 27. GRCI MultiLinx Model of the AV&V Wire Harness.

The MultiLinx Failure Propagation Assessment application uses Failure Modes, Failure Propagation rules, and Success Criteria to model failure effects on a system. The FPA documentation update suggests that single-point failure was the sole capability until recently. Up to 3 failure sources can now be chosen (Path or Component). The user defines propagation rules, success criteria, and failure modes. Failures are propagated through the system model, taking all interdependencies into account. Redundancy can be implemented and tested using Success Criteria and Success Criteria Alternatives. Success Criterion can be classified as Primary or Secondary. (Only Primary criteria are evaluated as part of the FPA Batch run / Reliability Analysis Report.)

Batch mode allows for input from ASCII file of Components or Paths to be used as single-point failures, or for generating all possible permutations of double and/or triple failures. This can take anywhere from several minutes to several days, depending on the complexity of the model. The documentation recommends that results not be saved when running double or triple permutations due to the extremely large failure sets. Even though the physical system is simple, the size of the model can become very large, very quickly. For reference, a single unshielded, twisted pair with a connector at each end requires the definition of a minimum of eight components and four paths. It should be noted that the documentation states that when batch mode is used, the user cannot predict which failure mode will be used for each connectivity type when multiple modes have been defined.

Batch mode can be used to assess reliability by defining a probability of failure as a Component Connectivity Type Metric with a Metric Name of Probability of Failure —Reliability or Probability of Failure —Availability and a value of 0-1.0 (% chance of failure occurring). The analysis can be run limiting the assessment to those failures with a probability of occurrence greater than some user-defined value. Batch results can be viewed using the FPA Results Report. This utility creates a set of text files containing details about the run that can be used to calculate a System Reliability Value. (The documentation referred to a FPA Batch Inputs/Outputs section, but that section was not included in the preliminary copy.)

The Diagram function can be used to visualize the failed components and paths in a highlighted schematic representation (some manual reorganization of the default diagram is required for readability). Source failures are highlighted with red filled circles. Secondary failures are highlighted with filled orange circles. Red rings denote components with failing Success Criteria and orange rings denote components where part of the Success Criteria is passing, but at least one of the Alternatives is failing. Green rings denote components with passing Success Criteria.

Modifications Needed for MultiLinx

Since some of the tools, especially the ATG capability, were undergoing modification, the User guide was not complete at the time of the demonstration, making it difficult to catalog all of the existing features.Either a GRCI expert can be used to maintain the system model (the X-38 program has a GRCI team managing their MultiLinx model for them), or program team members can be trained to maintain the system model independently (ISS program maintains their own model). The cost of maintaining the system model current with the actual Shuttle hardware configuration needs to be determined. The use of a cross-discipline system model requires a user who has cross-discipline expertise.

The ability of MultiLinx to handle the data with reasonable processing times with a large model needs to be proven. In abstract, the system model may be simple, but the details may prove to be overwhelming in their complexity and number. The MultiLinx underlying 4th Dimension database (ACI US, Inc.) may not be the optimal platform for a complete Shuttle wiring model. The MEC model used in this study is not large enough to stress the software or the hardware. It was noted that external tools are available to link 4th Dimension to other ODBC-compliant databases, such as Oracle and Microsoft Access, as well as the capability to interface with databases over the internet using web-browser technology.

A special function to import from CDF&TDS or SCAN should be added to the current import utility. If MultiLinx is used for Orbiter wiring, it will be in conjunction with existing databases. It will not supercede SCAN or CDF&TDS, so it must have the ability to repeatedly build a complete, current model from external input. This includes adding the ability to import special components (relays, diodes, etc.).

The configuration management issues must be solved. If MultiLinx has all of the specific information for every part, a new import should not overwrite the existing historical data. On the other hand, if a part is replaced, some means must be available to determine which test records belong to the new component and which belong to old components. Effectivity is not managed by MultiLinx. It may be more prudent to keep a separate database of test program files, results files, associated with specific part configurations.

The user interface is not intuitive enough to make up for the currently incomplete documentation. If systems engineers are to use MultiLinx interactively, the schematic diagram tool needs to have added visualization features, such as a component icon library, and filters to limit the number of components in any one diagram.

To be used in a diagnostic role, MultiLinx needs to have a failure analysis tool that can trace from symptom to root cause (FPA works in reverse). Perhaps a Fault-Tree analysis capability could be created from the FPA module. A fault-tree could be computed once for the current configuration from the FPA, and then tracing down the tree could be done in real-time.

WireWorks

Intergraph s WireWorks is software for design and documentation of electrical power and control systems. Tools are provided for quick schematic generation with symbol libraries, macros, and cut and paste editing. Many automatic functions, such as cross-referencing and wire numbering, are also provided. The built-in parts database is tied to the schematic, allowing automatic generation of bills of materials, panel layouts, wire lists, and terminal plans. The user can customize all drawing, symbol and listing formats.

Test Configuration/Test Data Usage

WireWorks is capable of producing ASCII wire list files for use in test program generation. Since it is intended for design purposes only, no test management tools are included.

Design Output: Lists, Reports, Drawings

WireWorks is fully capable of providing cable block diagrams, schematics, panel layouts, bills of materials, wire/cable schedules, and equipment lists. Also, WireWorks Data Distributor can provide ASCII files of all data necessary for wire lists or custom reports by populating a third-party application, such as Oracle or Microsoft Access.

Component Detailed Definition

Components in WireWorks are populated with all necessary data for WireWorks specific outputs. In addition, other tools, such as Intergraph s Instrument Data Manager, can share data such as tag numbers, locations, cable numbers, and miscellaneous electrical design requirements.

Accessible Database

WireWorks Data Collector utility extracts data from WireWorks projects to be stored in delimited ASCII files. The configuration of the extracted data is controlled by the user. WireWorks Data Distributor is used to transfer the ASCII files into any third party applications.

Wiring Design Automation Tools

WireWorks provides tools such as automatic cross-referencing; automated tagging of devices, wires, and cables; typical design templates; device and cable configuration management; and component placement by symbol, part, or data model.

Effectivity/Configuration Management

For managing Effectivity on the scale of the Orbiter, Intergraph recommends the use of an external document management system. Two products offered by Intergraph to work with WireWorks are Directa and Notia. The client/server nature of WireWorks allows for distributed processing, concurrent design, and project locking.

Contacts

Intergraph	(800) 260-0246

Logical Cable - WCAD

Boeing/Mentor Graphics W-CAD* has many desirable features, existing and in-development, for capturing design intent in its database. In order to capture the test configuration information, the underlying database should be further modified to contain the additional data. Also, a data input mechanism should be accessible to the designers. W-CAD currently has several ASCII format data import tools, but a user-friendly interface for mass data entry/modification would allow for entry of large amounts of data without using the schematic view to select each item individually for entry/modification. The designer could then accomplish much of the design in a rapid, generic schematic environment and then fill in the details for the component data in a table format if desired (or have another designer fill in the details).

*Wiring-CAD (W-CAD) is Boeing s modified version of Mentor Graphics Logical Cable (LCable). Boeing engineers and Mentor Graphics support have a continuing collaboration effort underway to develop W-CAD as a Shuttle-design-specific tool.

Pros:

- Shares data with CATIA (Shuttle 3D modeling CAD software package)
- Currently in use for Shuttle payloads wire design (investment already made)
- Highly system-intelligent and designer-friendly interface
- Customized for Shuttle-specific deliverable (schematics, wire-lists, etc.)
- Can import legacy data from CDF&TDS
- Ongoing customizations at Boeing s direction
- Drag and Drop schematic components from a library
- Component library is expandable (re-usable components jumpstart design)

Cons:

- Customizations owned by Boeing

LogicalCable (LCable)- ECAD Software Summary

Datasheet: http://www.mentorg.com/logical_cable/datasheet/index.html

Manufacturer

Mentor Graphics [www.mentorg.com]

Description

LCable is a CAD tool that can be integrated with CATIA (currently used for Shuttle 3-D modeling). It is in use now for electrical schematic development on Orbiter wiring (replacing obsolete TechniCAD) to a limited extent. An interface has been developed to download CDF&TDS data into LCable. The design can then be passed into a CATIA model for harness layout. Since most of the Shuttle is still paper design, the interface to CATIA is not always useful (yet). An entire 3-D model of the Shuttle may be required.

LCable runs on top of a proprietary database, which allows entry of product information related to the components. The data can then be listed in a report or used later in the design process without duplicating the data entry. Reports such as wire lists or bills of materials (BOMs) can be generated in real time in a user defined format (as an ASCII file if needed). The user interface is a graphical/data-entry interface. The design that can start with a high-level block diagram and progress on to greater levels of detail until the harness design is complete. Actually, the software deals with abstract representations of components easily, so the detail level of the design at any point is up to the designer.

LCable supports rules-based checking of the design (EMC checks, routing violations, connector-mate checks, etc.). CDF&TDS has a large rule-set used for checking designs that could be duplicated in LCable.

Features & Limitations

Integrates with CATIA (Dassault Systemes, IBM), Pro/Cabling (Parametric Technologies), SDRC Harness Design, UG Harness (EDS/UniGraphics), CDF&TDS

There are currently no Fault Propagation Analysis or Risk & Reliability Analysis tools.

A Diagram Constructor feature can take an ASCII wire list and (semi-) automatically create a schematic. If the wire list contains reference designators that mean something to the LCable Cable Library System (CLS) database, then the component data will also be included. The output file from Automated Test Equipment could feed into the Diagram Constructor for instant smart-file creation.

A wholesale conversion/replacement from CDF&TDS requires some manipulation of the data as it is imported, and the reports generated by CDF&TDS have to be duplicated in LCable. The link between SCAN and LCable also has to be created.

Software customization services are available from Mentor Graphics. The customer can also make customizations.

When maintaining records of the configuration over time for each Shuttle, one suggestion is the use of a PDM system to manage Effectivity. ENOVIA is an IBM PDM system used with CATIA that could do so.

Contacts

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Boeing, Huntington Beach	D. Buendia		david.buendia@west.boeing.com

ECT Promis•E

ECT s Promis•E is software for design and documentation of electrical control systems. Tools are provided for quick schematic generation with symbol libraries, macros, and cut and paste editing. Many automatic functions, such as cross-referencing and wire numbering, are also provided. The built-in parts database is tied to the schematic, allowing automatic generation of bills of materials, panel layouts, wire lists, and terminal plans. The user can customize all drawing, symbol, and listing formats. Symbol libraries are available for IEC, JIC, process control, hydraulic, and pneumatic applications.

Promis¥E runs on top of AutoCAD Release 14/2000(Autodesk). A stand-alone version is available that incorporates a run-time version of AutoCAD. The database is accessible through MS Access, making customization possible by either ECT International or the end customer. Part libraries are extensive and expandable.

- Database is not sophisticated enough to handle all of the various wire data elements with any intelligence
- Not capable of importing NASA legacy design data

Test Configuration/Test Data Usage

Promis•E is capable of producing ASCII wire list files for use in test program generation. Since it is intended for design purposes only, no test management tools are included.

Design Output: Lists, Reports, Drawings

Promis•E is fully capable of providing cable block diagrams, schematics, panel layouts, bills of materials, wire/cable schedules, and equipment lists. Also, Promis•E can populate a Microsoft Access database.

Component Detailed Definition

Components in Promis•E are populated with all necessary data for specific outputs. In addition, other data fields can be added to handle custom data requirements.

Accessible Database

Promis•E data is available to third-party database applications through ODBC. Microsoft Access is typically used to extract or manipulate the data.

Wiring Design Automation Tools

Promis•E provides tools such as automatic cross-referencing; automated tagging of devices, wires, and cables; typical design templates; and component placement by symbol using standard libraries (JIC, IEC).

Effectivity/Configuration Management

Promis•E organizes designs into Projects . The Shuttle wiring is most likely to complicated to be adequately managed in this manner. A third-party CM tool would be required.

Contacts

ECT International Promis•E Support (414) 781-1511

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Appendix 8 – CM Technologies Demonstration Report

This appendix includes a report submitted to the WIRe team from CM Technologies.

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Report on Wire Harness Testing at the Boeing's Huntington Beach Facility

Prepared for:

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June 2000

NOTICE

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1. Introduction

From May 2 to May 4, 2000, CM Technologies performed ECAD testing on two wire integrity test beds prepared by NASA Ames Research Center. The purpose of the testing was to determine the effectiveness of several standard electrical test methods in detecting and locating various types of wiring defects. The focus of the defects was nicked, chafed, or otherwise damaged insulation.

Measurements such as insulation resistance (IR), dielectric absorption ratio (DAR), capacitance, dissipation factor, AC and DC resistance, impedance, and time domain reflectometry (TDR) were all used in the assessment.

This report contains the results of a detailed analysis of the data, as well as conclusions and recommendations based on this analysis. For those unfamiliar with ECAD technology, Appendix A provides a description of the ECAD testing method.

A digital copy of the database files is located in Appendix B. The enclosed diskette contains the ECAD database files, INT12CDD.DAT and INT12MEA.DAT, GND12CDD.DAT and GND12MEA.DAT, and 22TPSCDD.DAT and 22TPSMEA.DAT, and ASCII text files (INT12.TXT, GND12.TXT, 22TPS.TXT) with all of the ECAD System 1100 measurement data.

2. Test Approach

The ECAD System 1100, shown in Figure 1, was used to perform all of the testing (again, see Appendix A for details on the ECAD methodology.) Since the goal of NASA s evaluation was to assess the off-the-shelf sensitivity of the ECAD test method, no special preparations were performed. As a result of this testing, however, a number of recommendations for optimizing the test equipment and analysis method became clear. These are discussed in the recommendation section of this report.

Figure 1. The ECAD System 1100.

2.1. Test Bed Description

The 12 AWG harness, shown in Figure 2, consisted of 19 unshielded, single conductor wires. The wires were formed into a harness and secured to the aluminum tray with several insulated clamps. The Amphenol connector J1 served as the test point for the ECAD equipment. The test equipment connection to the circuit under test was made by attaching alligator test clips to dummy pins inserted into the J1 connector.

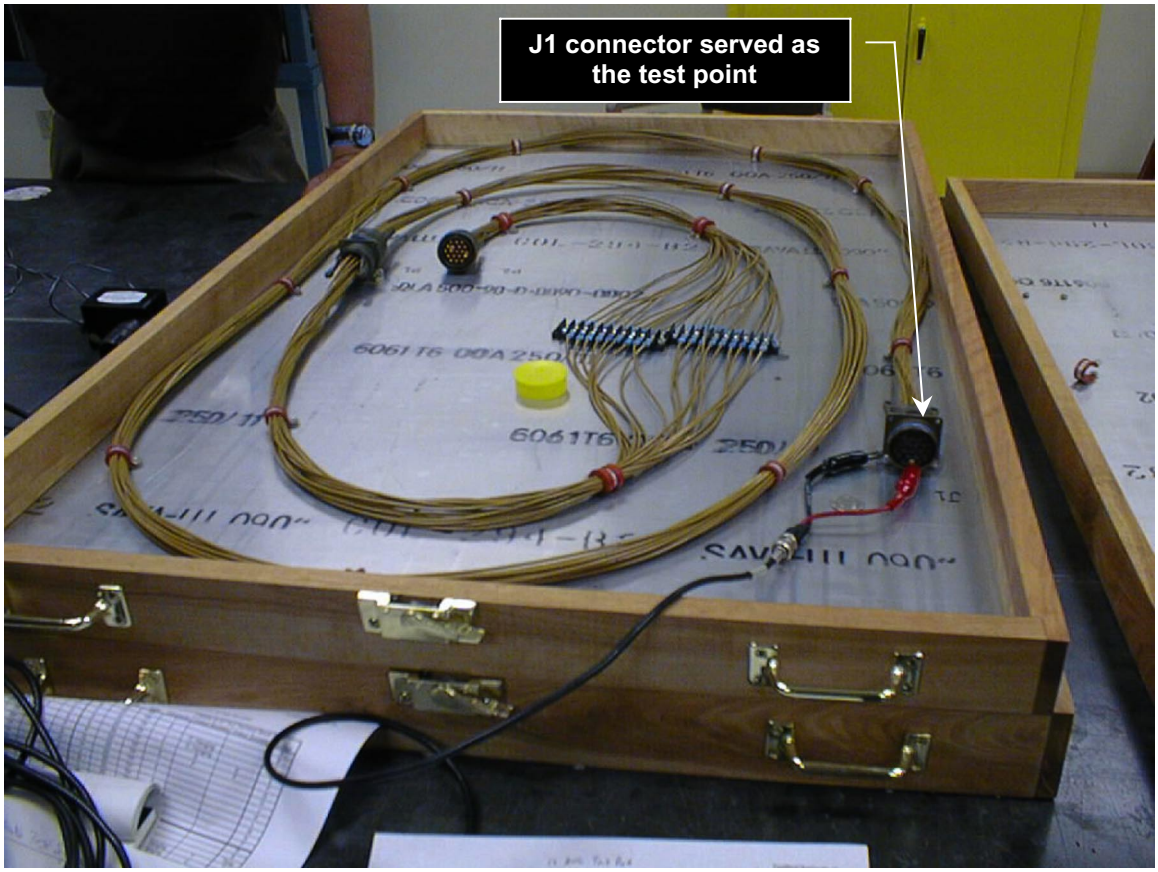

Figure 2. 12 AWG Integrity Test Bed.

The 22 AWG harness, shown in Figure 3, consisted of several different wire types. The 22 AWG contained 14 unshielded single conductor wires, 6 shielded twisted pair, and 14 controlled impedance wires. Dummy pins were used for the test equipment connection at the J1 connector.

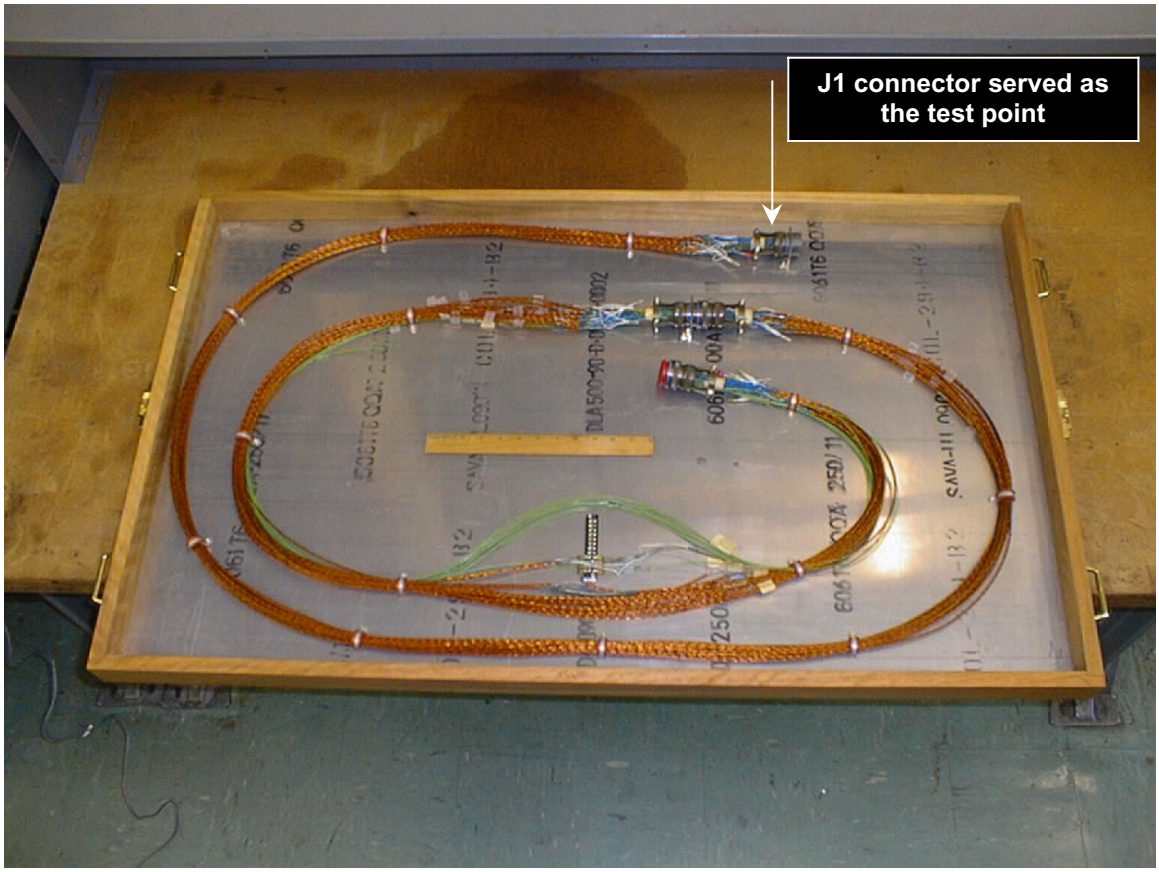

Figure 3. 22 AWG Test Bed

The wire insulation material for the 12 AWG and 22 AWG harnesses was Kapton.

2.2. Device Codes and Testing Configurations

Explanations of the device codes used for the testing are shown in Table 1.

Table 1. Device Codes Used for Testing.

Device Code	Description
12_AWG_INTEGRITY	Single Unshielded Wires in the 12 AWG Harness
12_AWG_INTEGRITY_GND	Single Unshielded Wires in the 12 AWG Harness (with all of the unused wires grounded)
22_AWG_SC	Single Unshielded Wires in the 22 AWG Harness
22_AWG_TP-S	Shielded Twisted Pair Wires in the 22 AWG Harness
22_AWG_CZ	Controlled Impedance Wires in the 22 AWG Harness
22_AWG_CZ-1	Controlled Impedance Wires in the 22 AWG Harness

The testing configurations were pre-selected by NASA Ames based on the faults and defects that had been inserted into the wire harnesses. If these harnesses were actually installed on the shuttle, however, the end device type would determine the ECAD testing configurations.

The testing configurations for the 12 AWG wire harness are shown in Table 2. These configurations were used for device codes 12_AWG_INTEGRITY and 12_AWG_INTEGRITY_GND.

Table 2. Testing Configurations for the 12 AWG Test Bed

Configuration	Description
A	J1 — Pin A to J1 - Pin N
B	J1 — Pin A to Ground
C	J1 — Pin B to J1 - Pin C
D	J1 — Pin B to Ground
E	J1 — Pin V to J1 - Pin N
F	J1 — Pin V to Ground
G	J1 — Pin H to J1 - Pin J
H	J1 — Pin H to Ground
I	J1 — Pin F to J1 - Pin G
J	J1 — Pin F to Ground
K	J1 — Pin K to J1 - Pin L
L	J1 — Pin K to Ground
M	J1 — Pin M to J1 - Pin N
N	J1 — Pin M to Ground
O	J1 — Pin S to J1 - Pin T
P	J1 — Pin S to Ground
Q	J1 — Pin P to J1 - Pin N
R	J1 — Pin P to Ground
S	J1 - Pin R to Ground
T	J1 - Pin U to Ground

The testing configurations for the single unshielded wires (device code 22_AWG_SC) in the 22 AWG wire harness are shown in Table 3.

Table 3. Testing Configurations for the Single Unshielded Wires in the 22 AWG Test Bed

Configuration	Description
A	J1 — Pin A to J1 - Pin B
B	J1 — Pin A to Ground
C	J1 — Pin B to J1 - Pin C
D	J1 — Pin B to Ground
E	J1 — Pin C to J1 - Pin D
F	J1 — Pin C to Ground
G	J1 — Pin E to J1 - Pin F
H	J1 — Pin E to Ground
I	J1 — Pin G to J1 - Pin H
J	J1 — Pin G to Ground
K	J1 — Pin J to J1 - Pin K
L	J1 — Pin J to Ground
M	J1 — Pin L to J1 - Pin M
N	J1 — Pin L to Ground
O	J1 — Pin N to J1 - Pin P
P	J1 — Pin N to Ground

The testing configurations for the shielded twisted pair wires (device code 22_AWG_TP-S) in the 22 AWG wire harness are shown in Table 4.

Table 4. Testing Configurations for the Shielded Twisted Pair Wires in the 22 AWG Test Bed

Configuration	Description
A	J1 — Pin R to J1 - Pin S
B	J1 — Pin R to Ground
C	J1 — Pin T to J1 - Pin U
D	J1 — Pin T to Ground
E	J1 — Pin V to J1 - Pin W
F	J1 — Pin V to Ground
G	J1 — Pin X to J1 - Pin Y
H	J1 — Pin X to Ground
I	J1 — Pin Z to J1 - Pin a
J	J1 — Pin Z to Ground
K	J1 — Pin b to J1 - Pin c
L	J1 — Pin b to Ground

The testing configurations for the controlled impedance wires (device codes 22_AWG_CZ and 22_AWG_CZ-1) in the 22 AWG wire harness are shown in Tables 5 and 6.

Table 5. Testing Configurations for the Controlled Impedance Wires (22_AWG_CZ) in the 22 AWG Test Bed

Configuration	Description
A	J1 — Pin d to J1 - Pin e
B	J1 — Pin d to Ground
C	J1 — Pin f to J1 - Pin g
D	J1 — Pin f to Ground
E	J1 — Pin h to J1 - Pin l
F	J1 — Pin h to Ground
G	J1 — Pin j to J1 - Pin k
H	J1 — Pin j to Ground
I	J1 — Pin r to J1 - Pin s
J	J1 — Pin r to Ground
K	J1 — Pin m to J1 - Pin n
L	J1 — Pin m to Ground
M	J1 — Pin p to J1 - Pin q
N	J1 — Pin p to Ground
O	J1 — Pin t to J1 - Pin u
P	J1 — Pin t to Ground
Q	J1 — Pin u to Ground
R	J1 — Pin v to J1 - Pin w
S	J1 — Pin v to Ground
T	J1 — Pin u to Ground
U	J1 — Pin x to J1 - Pin y
V	J1 — Pin x to Ground
W	J1 — Pin z to J1 - Pin AA
X	J1 — Pin z to Ground
Y	J1 — Pin BB to J1 - Pin CC
Z	J1 — Pin BB to Ground

Table 6. Testing Configurations for the Controlled Impedance Wires (22_AWG_CZ-1) in the 22 AWG Test Bed

Configuration	Description
A	J1 — Pin DD to J1 - Pin EE
B	J1 — Pin DD to Ground
C	J1 — Pin FF to J1 - Pin GG
D	J1 — Pin FF to Ground

A total of 118 ECAD tests were performed on the two test beds. In addition, 102 high-resolution TDR signatures were also acquired using the PCI-3100 in the standalone mode.

3. Detailed Data Analysis

3.1. 12 AWG Test Bed

Two sets of tests were performed on the 12 AWG wire harness. The first set, those tests with the 12_AWG_INTEGRITY device code, was performed with no modifications to the wire harness. The 1 kHz capacitance, inductance, dissipation factor and quality factor data are shown in Table 7.

Table 7. Selected Impedance Data from the 12 AWG Test Bed (Unused Wires Ungrounded).

Device Code	Cfg	L/C (1 kHz)	QF/DF (1 kHz)
12_AWG_INTEGRITY	A	0.36 nF	30.78 mD
12_AWG_INTEGRITY	B	0.50 nF	22.62 mD
12_AWG_INTEGRITY	C	0.38 nF	27.88 mD
12_AWG_INTEGRITY	D	0.49 nF	24.07 mD
12_AWG_INTEGRITY	E	0.37 nF	30.68 mD
12_AWG_INTEGRITY	F	0.49 nF	24.06 mD
12_AWG_INTEGRITY	G	0.43 nF	30.57 mD
12_AWG_INTEGRITY	H	0.51 nF	23.30 mD
12_AWG_INTEGRITY	I	0.36 nF	29.02 mD
12_AWG_INTEGRITY	J	0.44 nF	24.23 mD
12_AWG_INTEGRITY	K	0.43 nF	28.18 mD
12_AWG_INTEGRITY	L	0.50 nF	34.52 mD
12_AWG_INTEGRITY	M	0.37 nF	32.32 mD
12_AWG_INTEGRITY	N	0.50 nF	24.02 mD
12_AWG_INTEGRITY	O	0.44 nF	28.88 mD
12_AWG_INTEGRITY	P	0.49 nF	24.06 mD
12_AWG_INTEGRITY	Q	0.62 nF	16.16 mD
12_AWG_INTEGRITY	R	0.49 nF	24.06 mD
12_AWG_INTEGRITY	S	4.22 uH	728.92 mQ
12_AWG_INTEGRITY	T	0.52 nF	23.97 mD

The first outlier seen in the impedance data is configuration S, J1 pin R to ground. The impedance data for all of the test configurations should have been capacitive. The results from test configuration S are inductive and indicate a short circuit. The TDR signatures, shown in Figure 4, indicate a short circuit between pin R and ground is present.

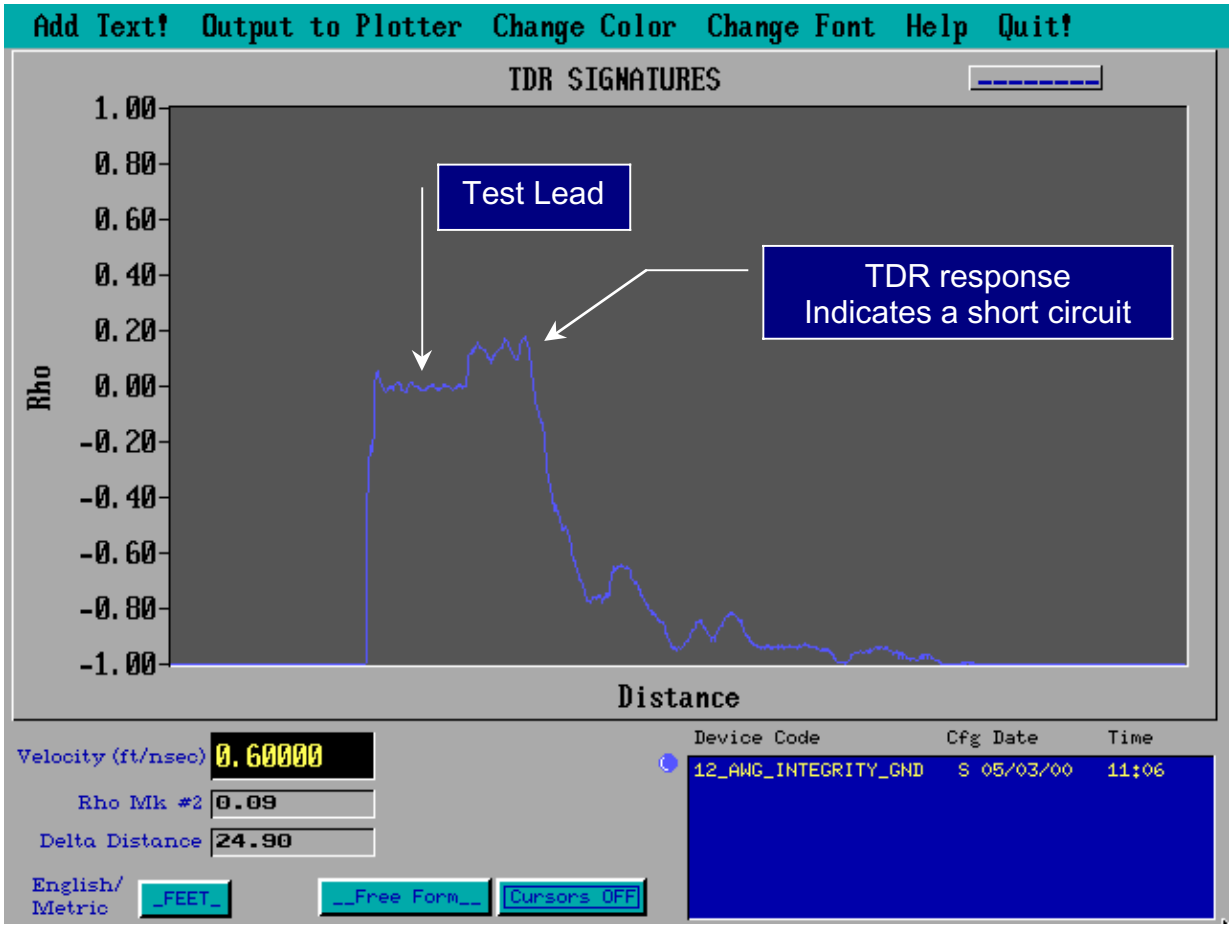

Figure 4. TDR Signatures Locate a Short Circuit for Cfg S.

Figure 5 shows the test configuration S signature at 2x magnification. From this data, we are able to determine that the short circuit is located in wire section between the terminal block and the end connector.

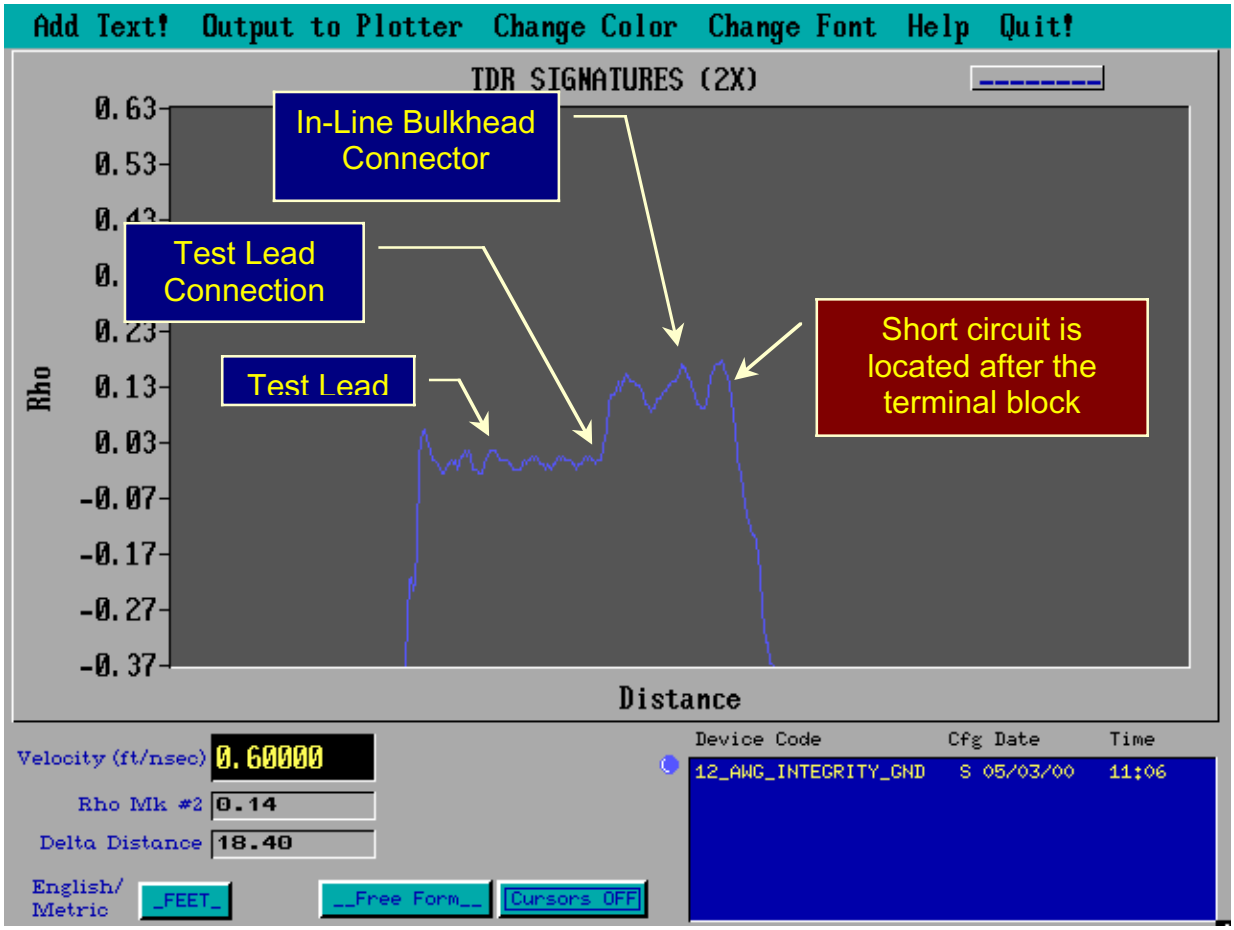

Figure 5. TDR Signatures Locate a Short Circuit for Cfg S (2x Zoom).

When the other configurations were compared in the lab, a significant variance in capacitance and dissipation factor values was observed. The reason for the difference is related to the wire type and geometry of the harness. CM Technologies has learned from our past experiences when testing unshielded, single conductor wiring that the geometry effects on the data can be reduced by grounding the unused conductors in the harness. As a result, a second set of tests was performed with the unused wires grounded (12_AWG_INTEGRITY_GND).

The first test on the 12 AWG wire harness also included insulation resistance (IR) tests. The IR tests were performed for 60 seconds with a test voltage of 1000 VDC. The first IR value at 5 seconds, the final IR value at 60 seconds, and the polarization ratio (PR) are shown in Table 8.

Table 8. Selected Insulation Resistance Data for the 12 AWG Harness.

Device Code	Cfg	First IR	Last IR	PR
12_AWG_INTEGRITY	A	1.37 G_	1.45 G_	1.02
12_AWG_INTEGRITY	B	97.95 G_	352.07 G_	1.35
12_AWG_INTEGRITY	C	1.84 G_	1.91 G_	1.01
12_AWG_INTEGRITY	D	109.71 G_	382.15 G_	1.34
12_AWG_INTEGRITY	E	958.05 M_	976.61 M_	1.01
12_AWG_INTEGRITY	F	107.11 G_	379.79 G_	1.33
12_AWG_INTEGRITY	G	2.95 G_	3.01 G_	921.36 m
12_AWG_INTEGRITY	H	104.22 G_	403.75 G_	1.39
12_AWG_INTEGRITY	I	1.81 G_	1.67 G_	974.47 m
12_AWG_INTEGRITY	J	104.43 G_	435.77 G_	1.42
12_AWG_INTEGRITY	K	2.29 G_	2.44 G_	1.03
12_AWG_INTEGRITY	L	105.31 G_	434.76 G_	1.46
12_AWG_INTEGRITY	M	1.99 G_	2.08 G_	1.02
12_AWG_INTEGRITY	N	90.82 G_	374.67 G_	1.38
12_AWG_INTEGRITY	O	2.03 G_	2.20 G_	1.03
12_AWG_INTEGRITY	P	100.67 G_	310.31 G_	1.12
12_AWG_INTEGRITY	Q	4.07 G_	3.96 G_	1.04
12_AWG_INTEGRITY	R	92.11 G_	325.91 G_	1.33
12_AWG_INTEGRITY	S	N/A	N/A	N/A
12_AWG_INTEGRITY	T	79.74 G_	291.02 G_	1.43

As expected, the insulation resistance data was not sensitive to the presence of any chaffed or damaged wiring. The reason is that the defects (i.e., cuts and abrasions) introduced into the wiring harness were clean and the test environment was clean. In order to be detectable, a semi-conductive material must be present in the damaged insulation. Some examples of these materials include hydraulic fluid, oil, water, carbon, and dust/dirt.

Table 9 contains the 1 kHz capacitance and dissipation factor data for 12 AWG tests with the unused conductors grounded. If these data are compared to the results shown in Table 7, it is clear that the variance between test configurations has been significantly reduced.

Another outlier in the data shown in Table 9 is the dissipation factor of test configuration E. Figure 6 is a comparison of the dissipation factor values from test configurations E, A, M and Q.

Table 9. Selected Impedance Data from the 12 AWG Test Bed (Unused Wires Grounded).

Device Code	Cfg	L/C (1 kHz)	QF/DF (1 kHz)
12_AWG_INTEGRITY_GND	A	0.62 nF	32.23 mD
12_AWG_INTEGRITY_GND	B	0.62 nF	32.28 mD
12_AWG_INTEGRITY_GND	C	0.55 nF	16.20 mD
12_AWG_INTEGRITY_GND	D	0.61 nF	33.17 mD
12_AWG_INTEGRITY_GND	E	0.53 nF	77.26 mD
12_AWG_INTEGRITY_GND	F	0.59 nF	35.18 mD
12_AWG_INTEGRITY_GND	G	0.54 nF	17.44 mD
12_AWG_INTEGRITY_GND	H	0.65 nF	31.46 mD
12_AWG_INTEGRITY_GND	I	0.60 nF	32.98 mD
12_AWG_INTEGRITY_GND	J	0.60 nF	33.38 mD
12_AWG_INTEGRITY_GND	K	0.62 nF	32.28 mD
12_AWG_INTEGRITY_GND	L	0.61 nF	33.91 mD
12_AWG_INTEGRITY_GND	M	0.68 nF	29.66 mD
12_AWG_INTEGRITY_GND	N	0.67 nF	30.64 mD
12_AWG_INTEGRITY_GND	O	0.67 nF	30.10 mD
12_AWG_INTEGRITY_GND	P	0.75 nF	25.52 mD
12_AWG_INTEGRITY_GND	Q	0.72 nF	27.78 mD
12_AWG_INTEGRITY_GND	R	0.72 nF	27.83 mD
12_AWG_INTEGRITY_GND	S	28.08 uH	221.16 mQ
12_AWG_INTEGRITY_GND	T	0.70 nF	27.92 mD
12_AWG_INTEGRITY_GND	T	0.72 nF	26.73 mD
12_AWG_INTEGRITY_GND	T	0.71 nF	27.44 mD

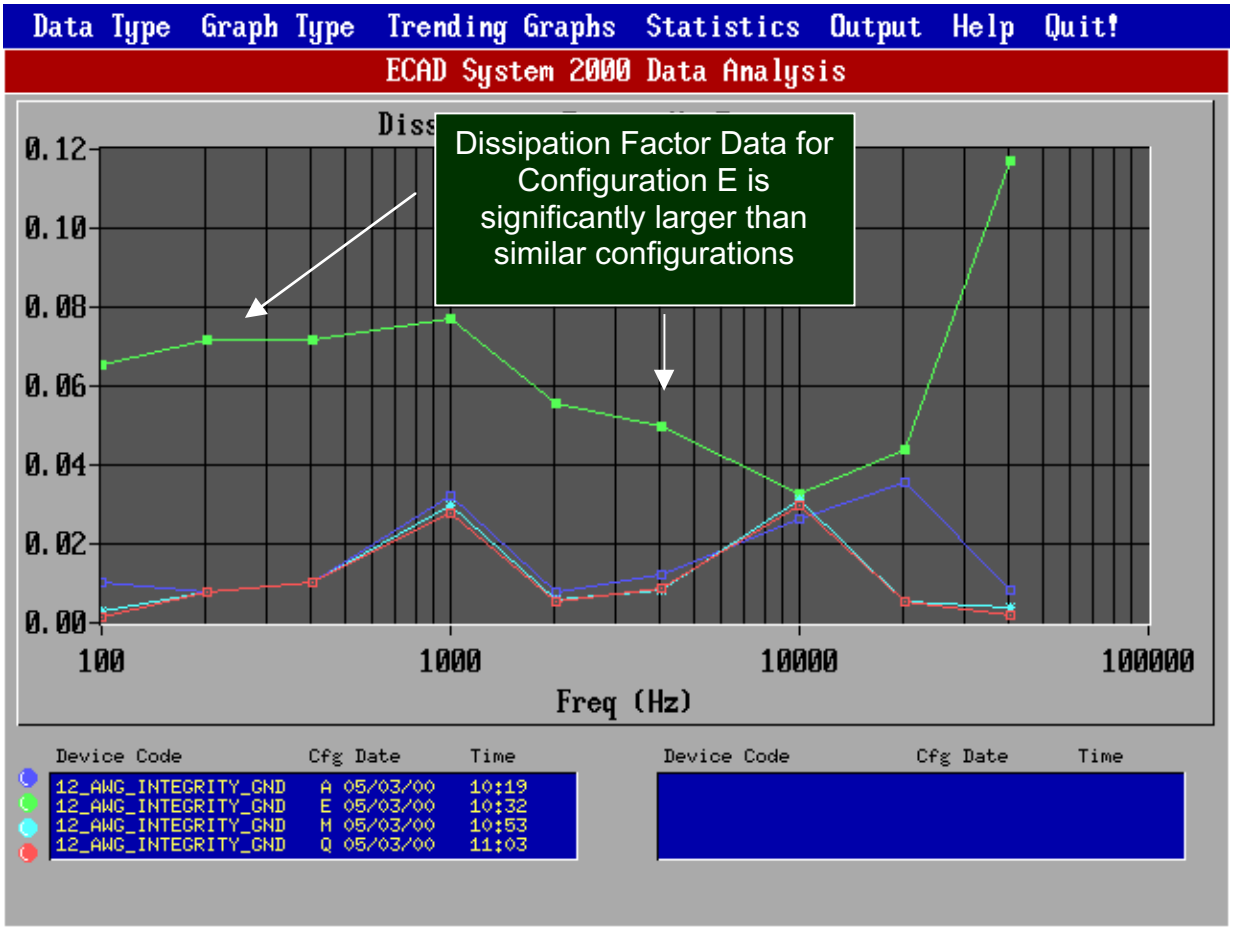

Figure 6. Dissipation Factor Data from Test Configuration E.

A comparison of the TDR signatures for test configurations A, E, M and Q are shown in Figure 7. The TDR signatures from test configuration E (J1 — Pin C to J1 - Pin D) indicate an area of increased resistance near the terminal block.

In addition, the TDR signature from configuration M (J1 — Pin L to J1 - Pin M) indicates an anomalous area near the end of the wiring harness.

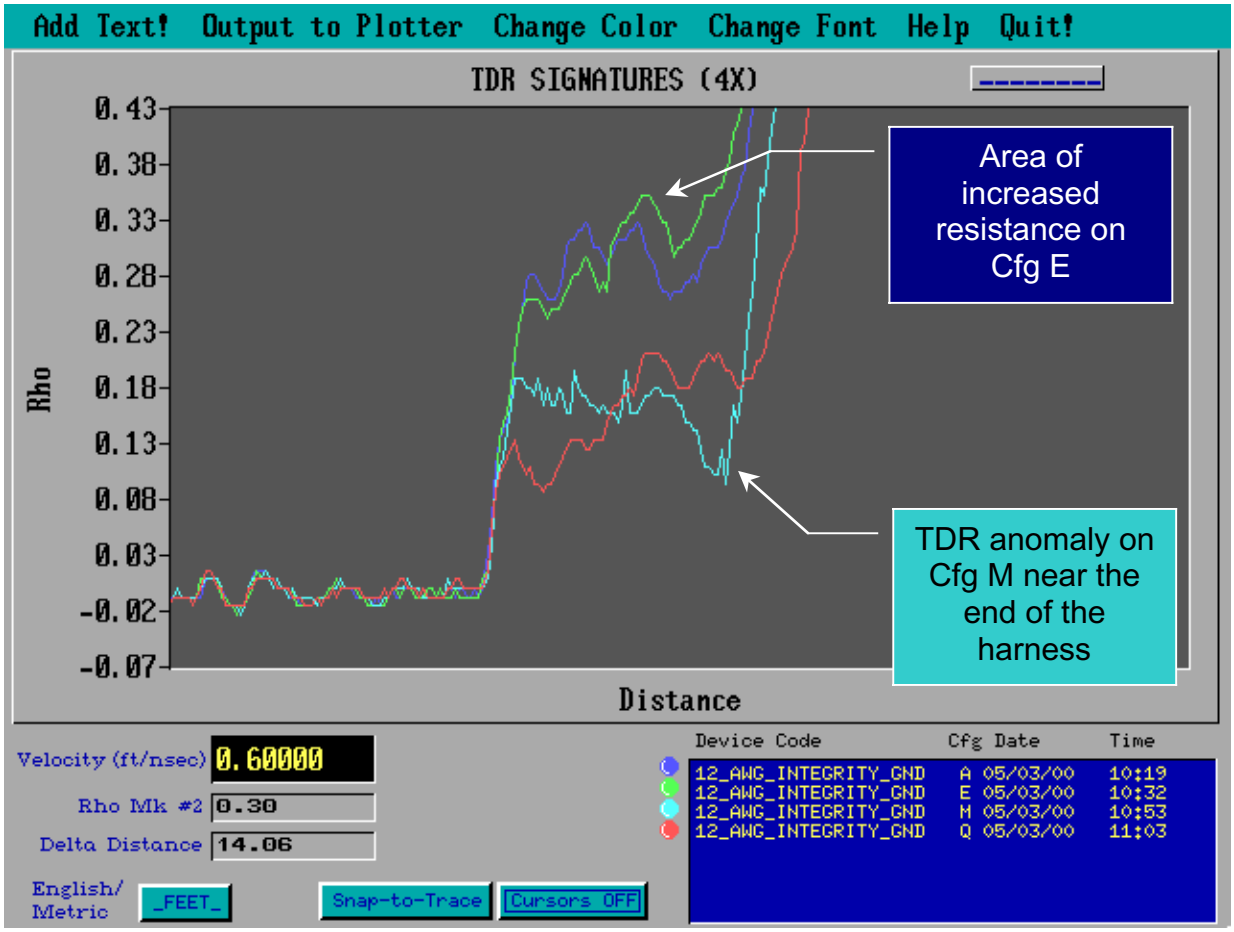

Figure 7. TDR Signatures from Configuration A, E, M, and Q.

Table 10 summarizes the results from 12 AWG wire harness testing. The summary is expressed in terms of the lumped electrical and the TDR signatures. A YES indicates that the configuration appeared as outlier when compared to the others or to configurations A and B (assumed good).

Table 10. Summary of Results for the 12 AWG Test Bed

Cfg	Lumped Data	TDR Signatures
A	Assumed Good	Assumed Good
B	Assumed Good	Assumed Good
C	Yes	Yes
D	No	Yes
E	Yes	Yes
F	No	Yes
G	Yes	Yes
H	No	No
I	No	No
J	No	No
K	No	No
L	No	No
M	No	Yes
N	No	No
O	No	No
P	Yes	No
Q	Yes	Yes
R	Yes	Yes
S	Yes	Yes
T	Yes	Yes

3.2. 22 AWG Test Bed

3.2.1. 22 AWG Single Conductor

Table 11 contains the 1 kHz capacitance and dissipation factor data for single conductor 22 AWG wire. Again, assuming that configurations A and B are good, three outliers are evident in the data — configurations F, O and P.

Table 11. 1 kHz Capacitance and Dissipation Factor Data for the 22 AWG Single Conductor Tests.

Device Code	Cfg	C (1 kHz)	DF (1 kHz)
22_AWG_SC	A	0.23 nF	49.45 mD
22_AWG_SC	B	0.29 nF	32.35 mD
22_AWG_SC	C	0.27 nF	45.50 mD
22_AWG_SC	D	**	**
22_AWG_SC	E	0.28 nF	46.91 mD
22_AWG_SC	F	0.34 nF	30.05 mD
22_AWG_SC	G	0.28 nF	46.93 mD
22_AWG_SC	H	0.28 nF	31.41 mD
22_AWG_SC	I	0.27 nF	47.19 mD
22_AWG_SC	J	0.28 nF	31.41 mD
22_AWG_SC	K	0.28 nF	44.73 mD
22_AWG_SC	L	0.28 nF	31.41 mD
22_AWG_SC	M	0.28 nF	45.37 mD
22_AWG_SC	N	0.29 nF	31.30 mD
22_AWG_SC	O	0.27 nF	50.92 mD
22_AWG_SC	P	0.33 nF	33.99 mD

** Configuration D was overlooked

The TDR signatures from configuration P appeared very similar to configuration B suggesting that the higher capacitance measured at 1 kHz may be related to geometry rather than a defect.

The TDR signatures from configurations F and B (see Figure 8), however, do indicate an area of increased capacitance near the terminal block area.

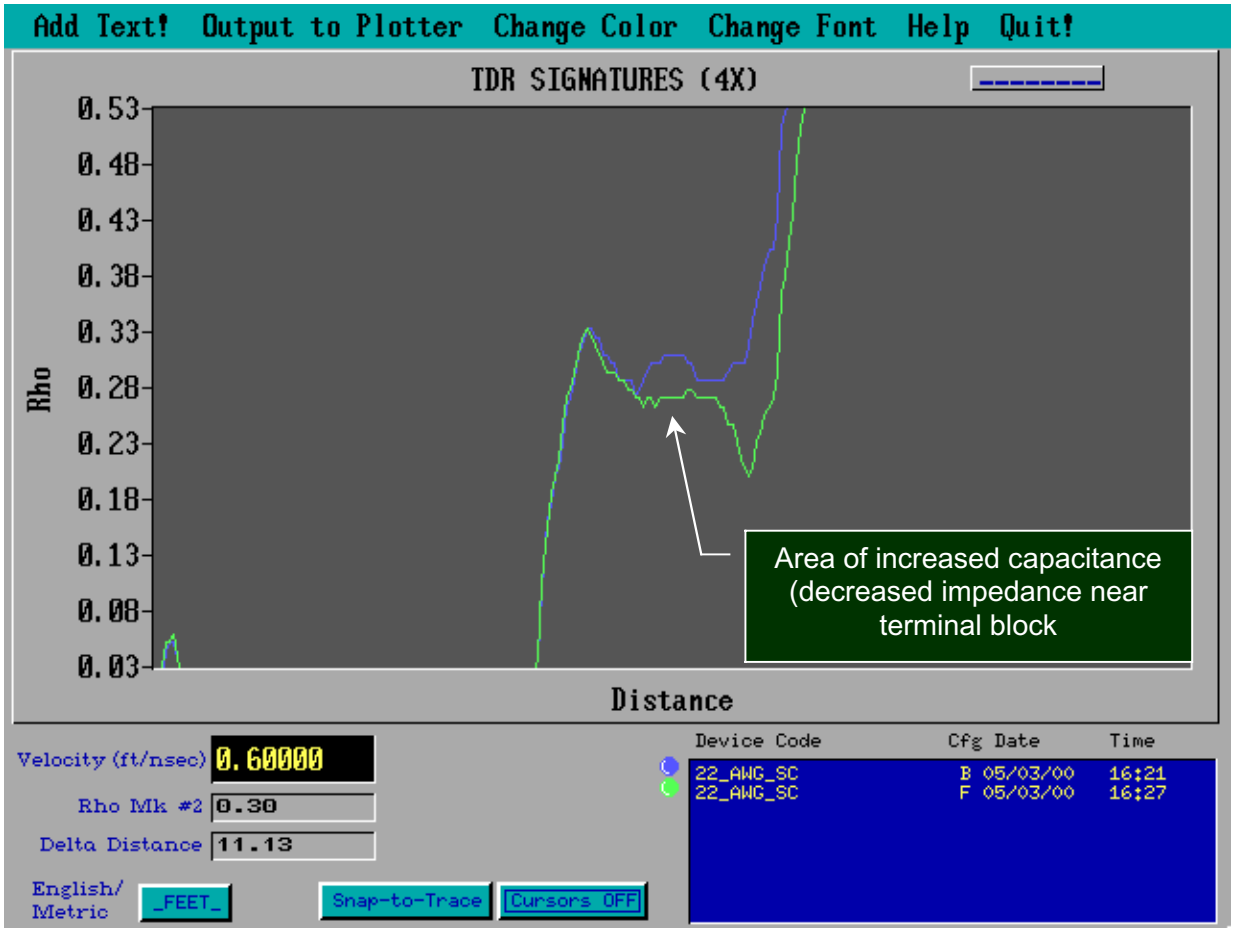

Figure 8. TDR Signatures from 22_AWG_SC Configuration B and F.

The data in Table 11 also show configuration O as an outlier (high dissipation factor) when compared with the other configurations. The TDR signatures for configurations A and O are shown in Figure 9 and locate an anomalous area near the end of the harness.

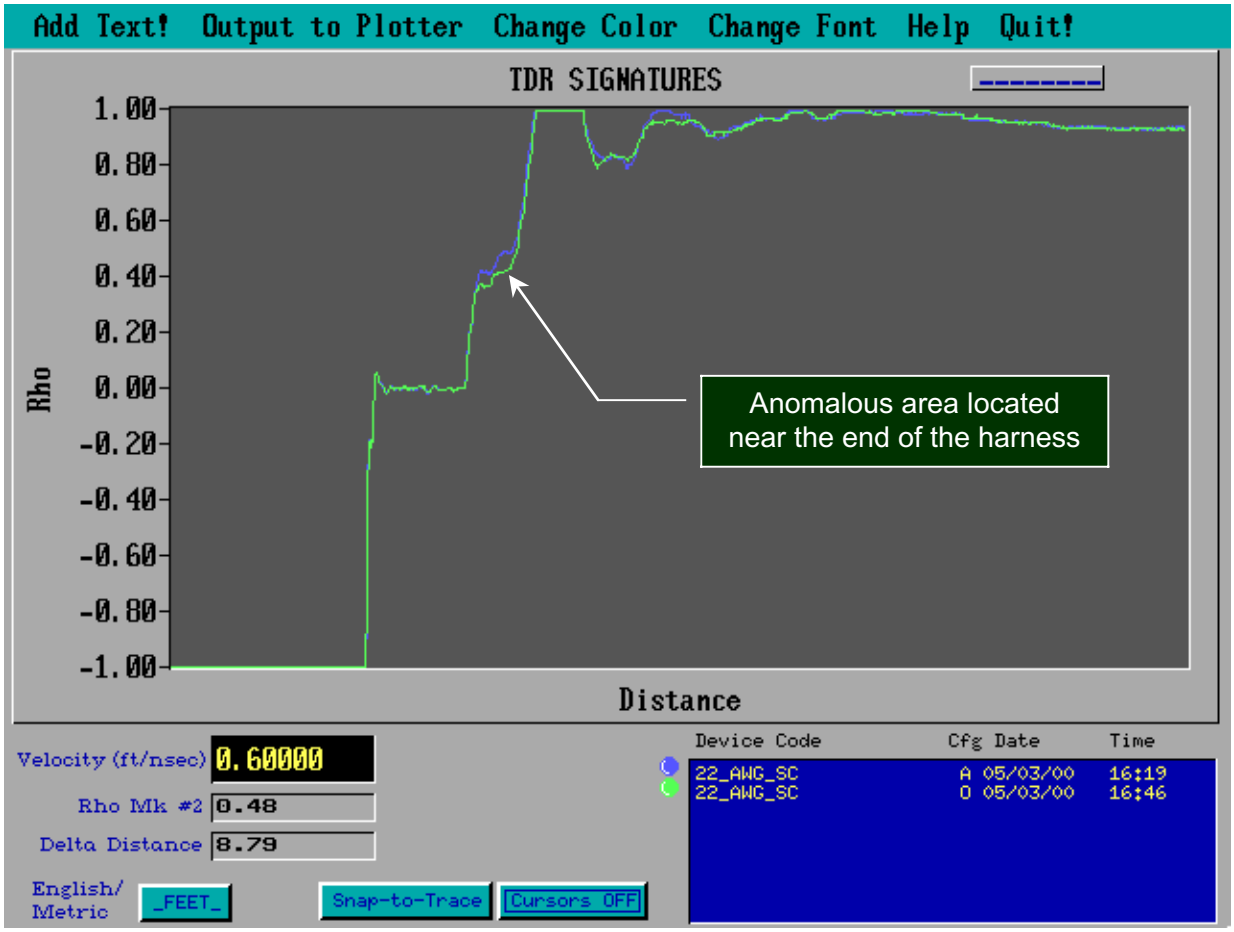

Figure 9. TDR Signatures from 22_AWG_SC Configuration A and O.

Table 12 summarizes the results from the single conductor tests on 22 AWG wire harness. Again, this summary is expressed in terms of the lumped electrical and the TDR signatures. A YES indicates that the configuration appeared as outlier when compared to the others or to configurations A and B (assumed good).

Table 12. Summary of Results for the 22 AWG Single Conductor Tests

Cfg	Lumped Data	TDR Signatures
A	Assumed Good	Assumed Good
B	Assumed Good	Assumed Good
C	No	No
D	No	No
E	No	Yes
F	Yes	Yes
G	No	No
H	No	No
I	No	Yes
J	No	No
K	No	Yes
L	No	No
M	No	No
N	No	No
O	Yes	Yes
P	Yes	No

3.2.2. 22 AWG Shielded Twisted Pair

Table 13 contains the 1 kHz capacitance and dissipation factor data for shielded twisted pair 22 AWG wire. Again, assuming that configurations A and B are good, several outliers are evident in the data — configurations C, D, L, H, and F.

Table 13. 1 kHz Capacitance and Dissipation Factor Data for the 22 AWG Twisted Shielded Pair Tests.

Device Code	Cfg	C (1 kHz)	DF (1 kHz)
22_AWG_TP-S	A	0.82 nF	0.17 mD
22_AWG_TP-S	B	1.03 nF	17.39 mD
22_AWG_TP-S	C	0.96 nF	3.53 mD
22_AWG_TP-S	D	1.21 nF	13.95 mD
22_AWG_TP-S	E	0.80 nF	6.13 mD
22_AWG_TP-S	F	1.18 nF	14.31 mD
22_AWG_TP-S	G	0.82 nF	0.72 mD
22_AWG_TP-S	H	1.11 nF	15.87 mD
22_AWG_TP-S	I	0.83 nF	0.84 mD
22_AWG_TP-S	J	1.03 nF	17.87 mD
22_AWG_TP-S	K	0.82 nF	0.70 mD
22_AWG_TP-S	L	1.11 nF	15.88 mD

Figure 10 shows a comparison of the TDR signatures from test configurations A and C. In area of increased capacitance is clearly evident near the end of the harness.

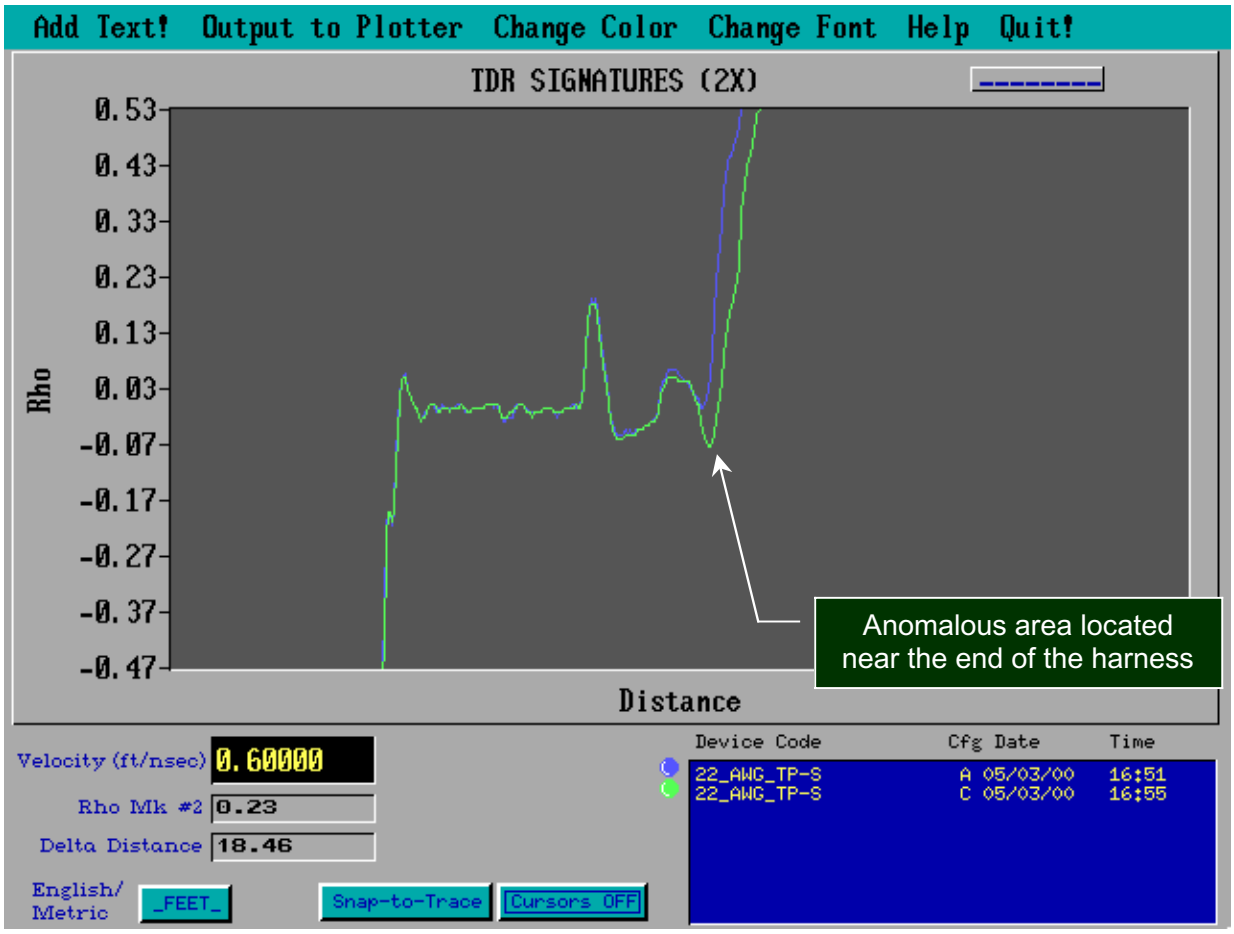

Figure 10. TDR Signatures from 22_AWG_TP-S

Table 14 summarizes the results from the shielded twisted pair tests on 22 AWG wire harness.

Table 14. Summary of Results for the 22 AWG Twisted Shielded Pair Tests.

Cfg	Lumped Data	TDR Signatures
A	Assumed Good	Assumed Good
B	Assumed Good	Assumed Good
C	Yes	Yes
D	Yes	Yes
E	No	No
F	Yes	Yes
G	No	No
H	Yes	Yes
I	No	No
J	No	No
K	No	No
L	Yes	Yes

3.2.3. 22 AWG Controlled Impedance

Table 15 contains the 1 kHz capacitance and dissipation factor data for the controlled impedance 22 AWG wire. Again, assuming that configurations A and B are good, three outliers are evident in the data — configurations E, F, G, and H.

Table 15. 1 kHz Capacitance and Dissipation Factor Data for the 22 AWG Controlled Impedance Tests.

Device Code	Cfg	C (1 kHz)	DF (1 kHz)
22_AWG_TSP-CZ	A	0.44 nF	43.19 mD
22_AWG_TSP-CZ	B	0.52 nF	40.81 mD
22_AWG_TSP-CZ	C	0.46 nF	42.79 mD
22_AWG_TSP-CZ	D	0.52 nF	40.71 mD
22_AWG_TSP-CZ	E	0.27 nF	47.23 mD
22_AWG_TSP-CZ	F	0.29 nF	32.16 mD
22_AWG_TSP-CZ	G	0.28 nF	48.02 mD
22_AWG_TSP-CZ	H	0.27 nF	49.75 mD
22_AWG_TSP-CZ	I	0.46 nF	42.73 mD
22_AWG_TSP-CZ	J	0.52 nF	41.07 mD
22_AWG_TSP-CZ	K	0.42 nF	44.06 mD
22_AWG_TSP-CZ	L	0.52 nF	40.86 mD
22_AWG_TSP-CZ	M	0.46 nF	42.79 mD
22_AWG_TSP-CZ	N	0.52 nF	39.99 mD
22_AWG_TSP-CZ	O	0.46 nF	43.99 mD
22_AWG_TSP-CZ	P	0.52 nF	40.39 mD
22_AWG_TSP-CZ	Q	0.52 nF	41.72 mD
22_AWG_TSP-CZ	R	0.46 nF	43.49 mD
22_AWG_TSP-CZ	S	0.52 nF	40.71 mD
22_AWG_TSP-CZ	T	**	**
22_AWG_TSP-CZ	U	0.46 nF	42.79 mD
22_AWG_TSP-CZ	V	0.52 nF	40.02 mD
22_AWG_TSP-CZ	W	0.46 nF	43.54 mD
22_AWG_TSP-CZ	X	0.52 nF	40.02 mD
22_AWG_TSP-CZ	Y	0.46 nF	44.19 mD
22_AWG_TSP-CZ	Z	0.52 nF	40.50 mD
22_AWG_TSP-CZ-1	A	0.46 nF	42.63 mD
22_AWG_TSP-CZ-1	B	0.52 nF	40.36 mD
22_AWG_TSP-CZ-1	C	0.46 nF	42.79 mD
22_AWG_TSP-CZ-1	D	0.52 nF	40.02 mD

** Repeated configuration

The TDR signatures from configurations F, H, X, Z, B, and are

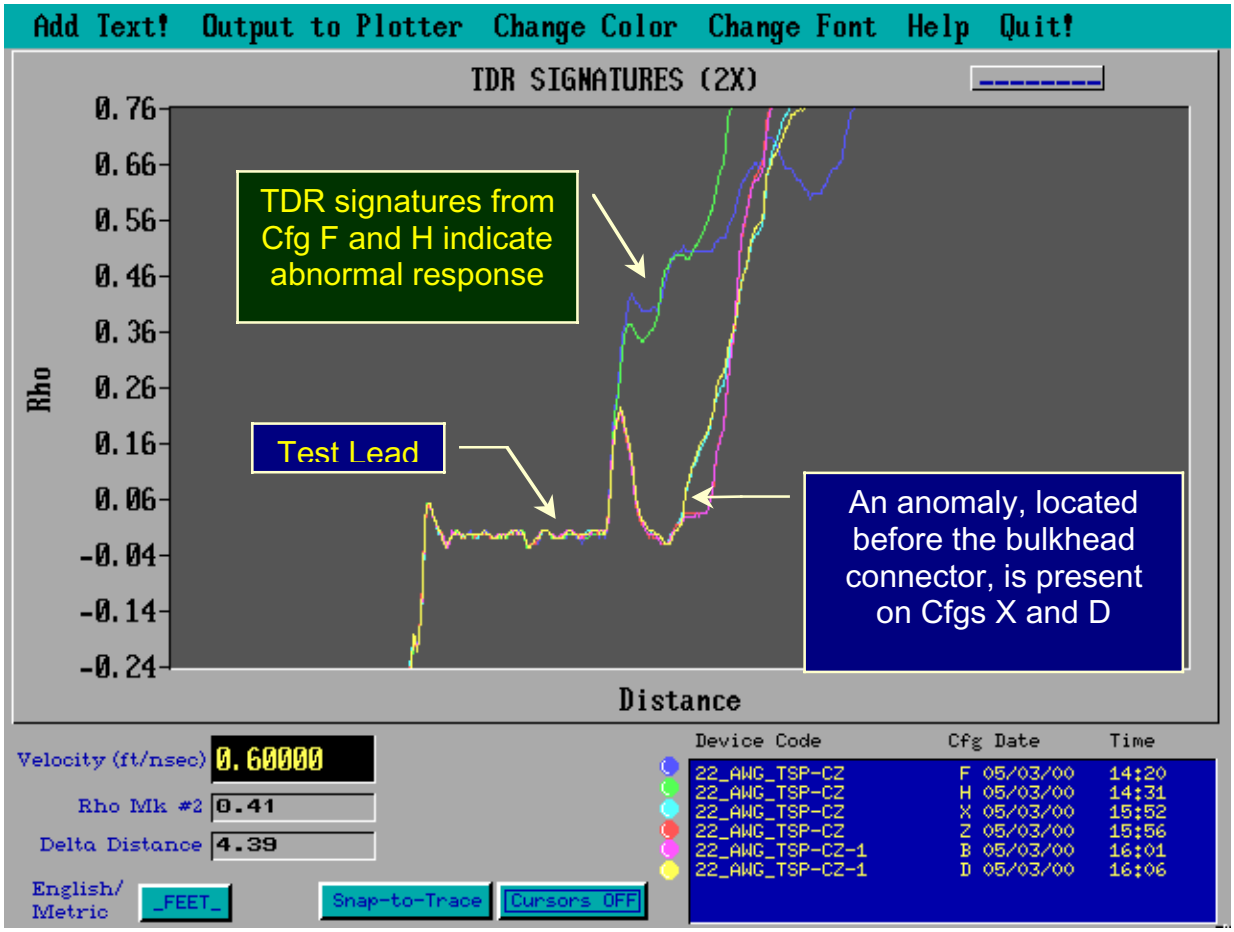

Figure 11. TDR Signatures from Controlled Impedance Wire.

Table 16 summarizes the results from the controlled impedance tests on 22 AWG wire harness.

Table 16. Summary of Results for the 22 AWG Controlled Impedance

Cfg	Lumped Data	TDR Signatures
A	Assumed Good	Assumed Good
B	Assumed Good	Assumed Good
C	No	No
D	No	No
E	Yes	Yes
F	Yes	Yes
G	Yes	Yes
H	Yes	Yes
I	No	No
J	No	No
K	No	No
L	No	No
M	No	No
N	No	No
O	No	No
P	No	No
Q	No	No
R	No	No
S	No	No
T	No	No
U	No	No
V	No	No
W	No	No
X	No	Yes
Y	No	No
Z	No	Yes
CZ-A	No	No
CZ-B	No	Yes
CZ-C	No	No
CZ-D	No	Yes

4. Conclusions

Off the Shelf Performance

In general, the ECAD test method was applicable to both wire harnesses. The single-ended test method had sufficient range and resolution to detect and locate several of the defects and faults.

Performance Categories

Based on the results from this test and by applying our standard analysis methods, there appeared to be three performance categories for ECAD test method.

1. Certain defects and faults affected both the lumped properties (impedance, capacitance) and the distributed properties (TDR). This represents our standard analysis method.

2. Certain defects and faults did not produce a significant change in the lumped electrical properties, but the TDR detected them as an anomaly. We were able to detect these defects based upon our experience with interpreting TDR signatures. In some cases, we recognized the TDR response and were able to correlate it to a defect. In other instances, we observed an abnormal response, but were unable to correlate it to a defect type.

3. Certain defects and faults did not produce a significant change in either the lumped properties or the TDR signature. This was expected as not all defects result in a change in a wire s electrical characteristics.

5. Recommendations

Based on the results of this testing, CM would like to offer the following general recommendations.

Test Instrumentation Optimization

It is clear that the ECAD test instrumentation could be optimized for this application. Some of areas to consider, include:

- switching hardware to more easily interface the test equipment and the wire under test,
- increase the test frequencies used to make impedance measurements,
- and experiment with the TDR properties to determine an optimum configuration given the lengths, geometries and materials used on the shuttle.

Modeling Wiring Defects

NASA should consider developing a mathematical model(s) of various wiring harnesses. This model could be used to establish acceptance criteria in terms of the harness s electrical properties. A model would also be useful in assessing the sensitivity (tolerance) to certain defects.

Appendix A

ECAD Testing Methodology

Testing Methodology

Each of the selected circuits is tested according to a logical set of predefined configurations. The configurations provide a standard method of testing a particular device type. For example, a three phase motor circuit is tested using six test configurations, A through F. Configurations A, B, and C are the phase to phase tests; configurations D, E, and F are the phase to ground tests. Circuits tested in this manner are easily compared to like devices tested in other locations. These test configurations, along with other information about the circuit under test are stored in a circuit descriptive database.

Prior to testing, the circuit is de-energized and de-terminated. Test equipment setup and data acquisitions are performed automatically, and the measured values are stored in a measurement database. A typical circuit is completely tested in approximately ten minutes.

The measurements acquired by the system can be separated into two groups, lumped data and the distributed measurement. The lumped measurements treat the entire circuit (cable, connections and end device) as a network of simple resistors, capacitors, and inductors. The lumped measurements are as follows:

- AC and DC Voltage
- DC Resistance
- Impedance and Phase Angle
- Insulation Resistance

Voltage measurements are made to determine the amount of induced voltage, if any, on the circuit. The measurements also provide protection of the test equipment. The DC resistance represents the total resistance of the circuit. Impedance and phase angle measurements are made at nine discrete frequencies from 100 Hz to 40 kHz. From this data, critical parameters such as inductance, quality factor, capacitance, and dissipation factor are calculated.

An optional insulation resistance (IR) test can be performed if the DC resistance values are greater than 500 kΩ. For this test, a user specified voltage from 1 to 1,100 volts DC is applied for one of the following durations: 1 minute, 3 minutes, or 10 minutes. Twelve readings are taken during each test duration. For example, readings are taken every 15 seconds during the 3 minute test. In addition, for each test duration, the following ratios are calculated:

Dielectric Absorption Ratio (DAR) = 60 sec. IR/30 sec. IR (1 minute test)
Polarization Ratio (PR) = 180 sec. IR/15 sec. IR (3 minute test)
Polarization Index (PI) = 600 sec. IR/60 sec. IR (10 minute test)

The lumped data are normally the first and best indicators of circuit anomalies. DC resistance and inductance are loop values related to the circuit s conductive path. Quality factor is the ratio of reactance to the AC resistance and is a measure of the purity of an inductive circuit. In other words, the higher the resistive losses in an inductive circuit, the lower the quality. These parameters are used to identify problems such as opens, shorts, poor or degraded connections, and failed end devices.

IR, PR, capacitance, and dissipation factor are used to determine the insulation quality of a circuit. These values are used to identify insulation degradation, moisture intrusion, and failed end devices. IR is a measure of the DC losses through the dielectric or insulating material. PR is independent of temperature and is based on the absorption effect of the insulation; good insulation shows a steady increase in IR over several minutes resulting in PRs of the greater than 1. Dissipation factor, the ratio of AC resistance to reactance, is a measure of the AC losses through the insulation. The capacitance of the circuit is dependent on both the physical characteristics of the circuit and dielectric material.

Once problems are identified with the lumped measurements, they can be located using the distributed circuit measurement, the time domain reflectometry (TDR) signature. TDR is a technique analogous to radar where a pulse with a fast risetime is propagated along the circuit. The circuit acts as a radio frequency transmission line with the pulse traveling along the line at a velocity fixed by the line s characteristics. Any impedance discontinuities cause a reflected wave to travel back towards the generator where it is captured. This reflection indicates the type and location of a discontinuity.

Appendix B

Data Charts and Data Diskette

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Appendix 9 – Qualtech TEAMS Model for Test Management

This appendix includes a report submitted to the WIRe team from Qualtech.

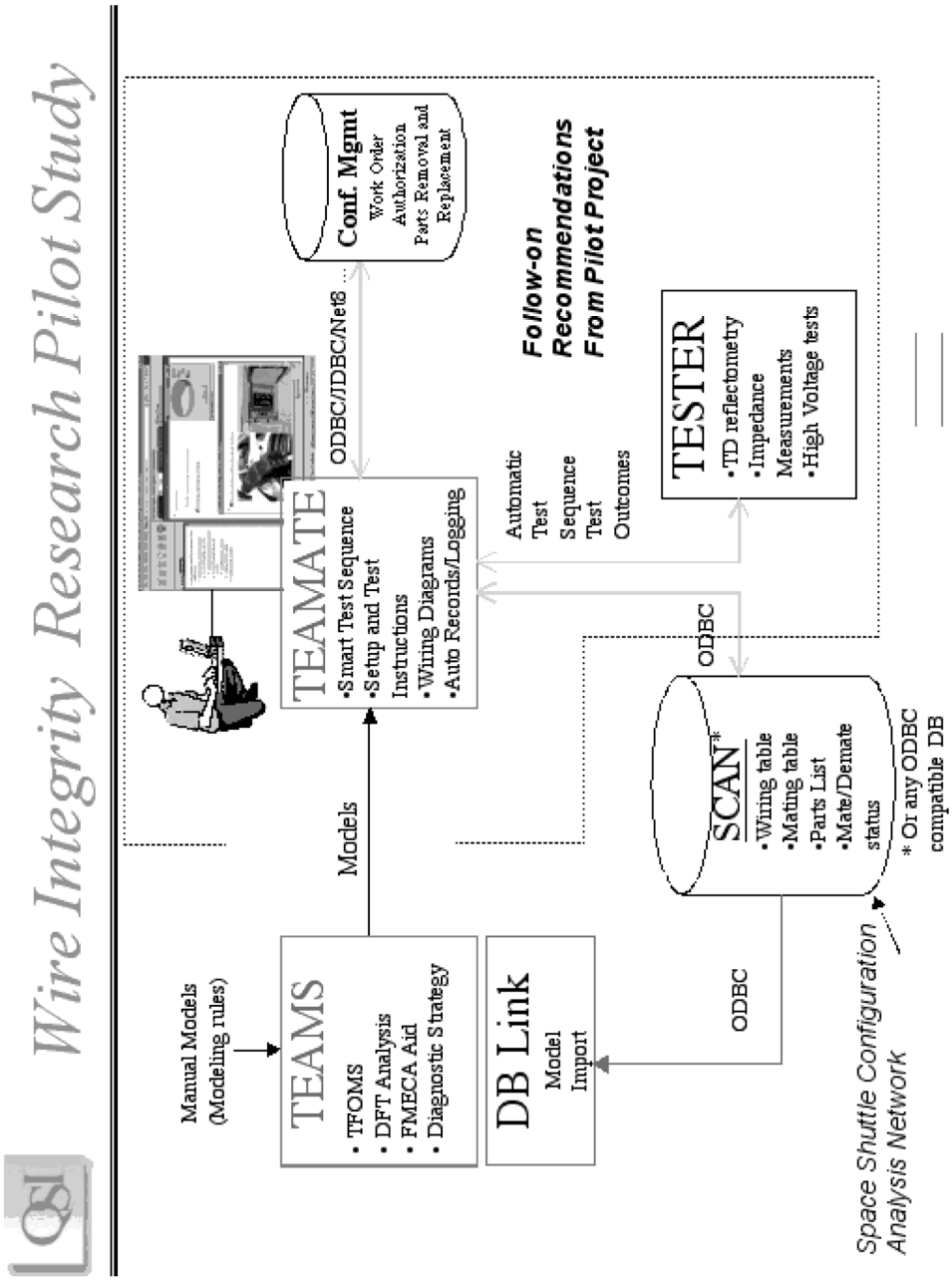

Figure 28. Using Teams for Orbiter Test Management .

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Final Report for the Manually and Automatically Generated Shuttle Wiring Model using TEAMS 5.1

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Table of Contents

1. Introduction

The intent of this pilot study was to investigate the feasibility of automatically creating a TEAMS model for a subset of the space-shuttle wiring. The model could be used by the TEAMS toolset to guide the technician in the wiring diagnosis and quality assurance process while helping NASA engineers monitor the extent of wiring failure modes covered by the testing process. The TEAMS toolset could also provide the technician with the necessary tools to electronically log all maintenance activities, and help automate the maintenance process, while preserving all the existing checks and balances. A short description of the TEAMS toolset is presented in Appendix A.

All of the wiring information required for creating the TEAMS model was supplied via a Shuttle Connector Analysis Network (SCAN) Electronic wirelist. This partial wirelist contained all the wiring information relative to the MEC1 assembly. Using this NASA supplied SCAN wirelist, QSI concurrently created manual and automatically generated TEAMS wiring models for all wire paths associated with connector J3 on the MEC1 assembly. The manually generated model helped establish the rules of modeling. The automated model was compared against the manual model to verify that the automatically generated model accurately portrayed the actual shuttle wiring. Once it was ascertained that the automatically generated model was identical to the one created manually, the complete MEC1 model was generated, thus saving significant modeling cost.

2. Deliverables

The enclosed CDROM includes the software and model deliverables for the project in a single self-extracting file, `teams51_alpha_setup.exe`. Insert the CDROM in a Windows 9X/NT machine and execute this file to setup Alpha version of TEAMS-5.1 software, which has been customized for the automated wiring model generation. The deliverables for this pilot study were the following:

- Manually generated model of the J3 connector wiring for MEC1. Assuming TEAMS is installed in `C:\teams51`, the model can be loaded into TEAMS by double clicking on the file `C:\teams51\Complib\Mec1_j3\Harness1.tms`.
- Automatically generated model for all connectors of the MEC1. This model can be loaded by double clicking on the file `C:\teams51\Complib\NasaAuto\mec1.tms`
- Software for auto-generation and analysis of wiring models —namely TEAMS 5.1 Alpha, with several enhancements for interfacing to SCAN tables and auto-generation of wiring models.
- Analysis documentation (contained herein)
- Tutorial or briefing presented at NASA-ARC on May 8, 2000 and at the Aging Aircraft conference in St. Louis on May 16, 2000.

3. Modeling Methodology

TEAMS multisignal modeling is a hierarchical modeling methodology. Models can be built top-down or bottom-up. In the present effort we pursued a bottom up approach, where we first created a library of connector and wire types and then interconnect them as per the SCAN wirelist to generate the complete model. To automatically generate the TEAMS model, the raw data from the SCAN wirelist was converted into a format more compatible with TEAMS. The details of the table formats are presented in Appendix F. A filter was written to reformat this into TEAMS model. The details of this conversion process can be found in Appendix G. An import function was added to TEAMS to read the TEAMS-SCAN model over ODBC and automatically generate the model.

In making the models of the components, we made some basic assumptions regarding to failure modes of components, level of repair, testing methods, etc. These are documented in the following subsections.

3.1 Modeling of connectors

For connectors, it was assumed that only the pins of the connector can fail, and that the possible failure modes of the pins are:

1. *PushedPin* or open circuit caused by pushed pins
2. *PinCorrosion* or resistive contact, possibly caused by corroded pins or poor contact with mating pin
3. *BentPin* or shorts possibly caused by a bent pin shorting to an adjacent pin, or a piece of metal shorting two or more pins

It was confirmed in a telephone conference with NASA-Kennedy Space that NASA procedures require that the pins in connectors be repaired or replaced, rather than replacing the entire connector. Therefore, the connectors were labeled as modules, and the pins as (replaceable) components with the three failure modes as discussed previously (see Fig. 1). The connector was modeled as a collection of pins with the appropriate pin labels (see Fig. 2). To avoid unnecessary undetected failures, only the wired pins were represented in the TEAMS model.

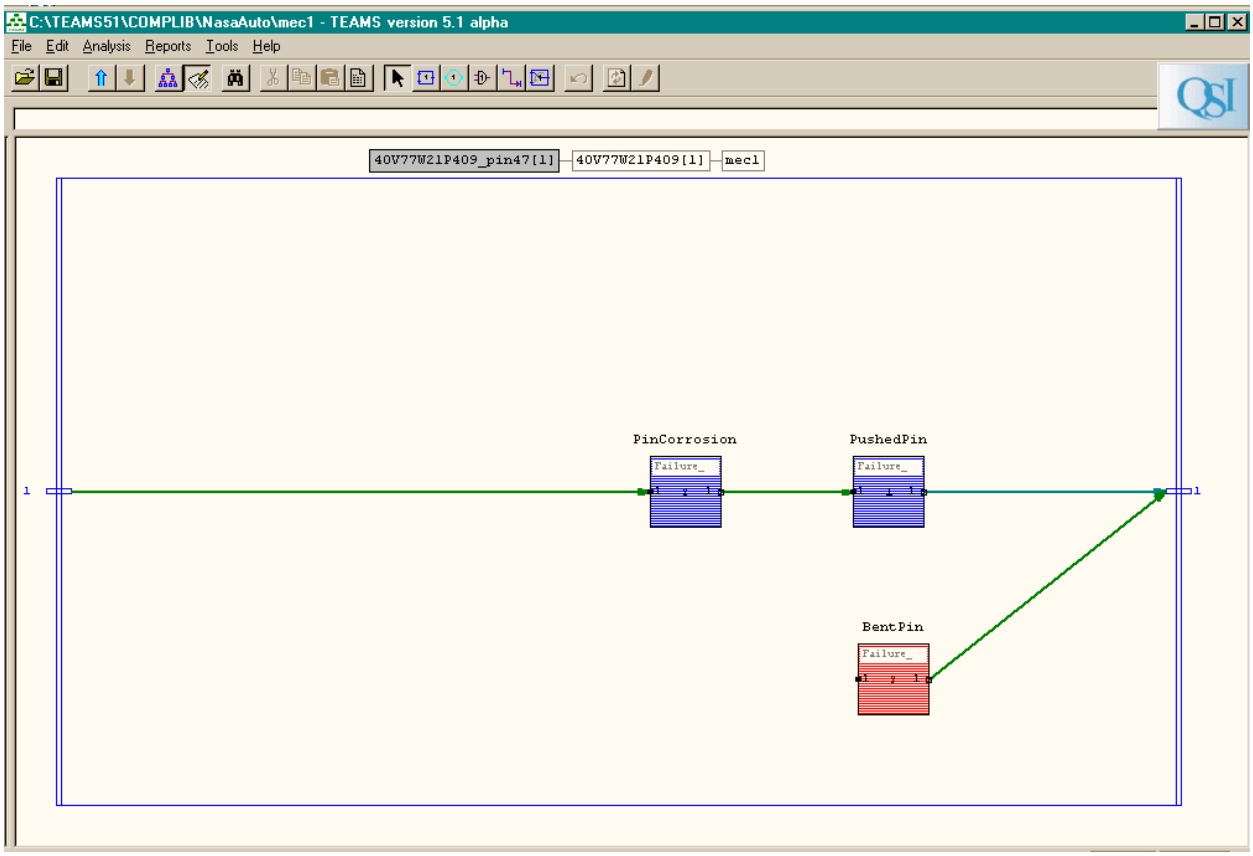

Figure 1: Connector Pin Module

3.2 Modeling of wires

Wire failure modes were generated as follows:

1. *Open*, e.g., due to a broken conductor

2. *DeltaResistance*, e.g., oxidized or frayed conductor making partial connections
3. *HardShort* , e.g., a short circuit to ground or adjacent conductors due to damaged insulation
4. *BadDielectric*, e.g., worn or degraded insulation allowing arcing when a high voltage is applied, possibly causing intermittent, and potentially hazardous, electrical discharges under normal operation

The wires were modeled based on their type (conductor, twisted pair, twisted pair shielded, etc.). A library of wire components was created based on the wire types listed in the SCAN wirelist. Consistent with NASA repair procedures, a twisted wire was modeled as a single wire component since it would be replaced as a single unit. The Wire Type and Cable Descriptor fields of the SCAN database uniquely define bundles. For each wire (or conductor) in the wire type, we inserted a sub-component with the appropriate failure modes. The shield, however, has only one failure mode, representing a broken shield or ground path. Fig. 3 presents an example model of a wire showing the failure modes. Fig. 4 presents the model of 2 conductor shielded wire of gauge F wires (F2S).

The model can easily be updated to represent actual wiring repair practices used by NASA, should the current assumptions prove incorrect. If, for example, it is determined that a particular harness cannot be repaired and must be replaced as an entire assembly, then the repair label of that particular harness would be revised, leaving the previously defined repair labels for the other harnesses intact.

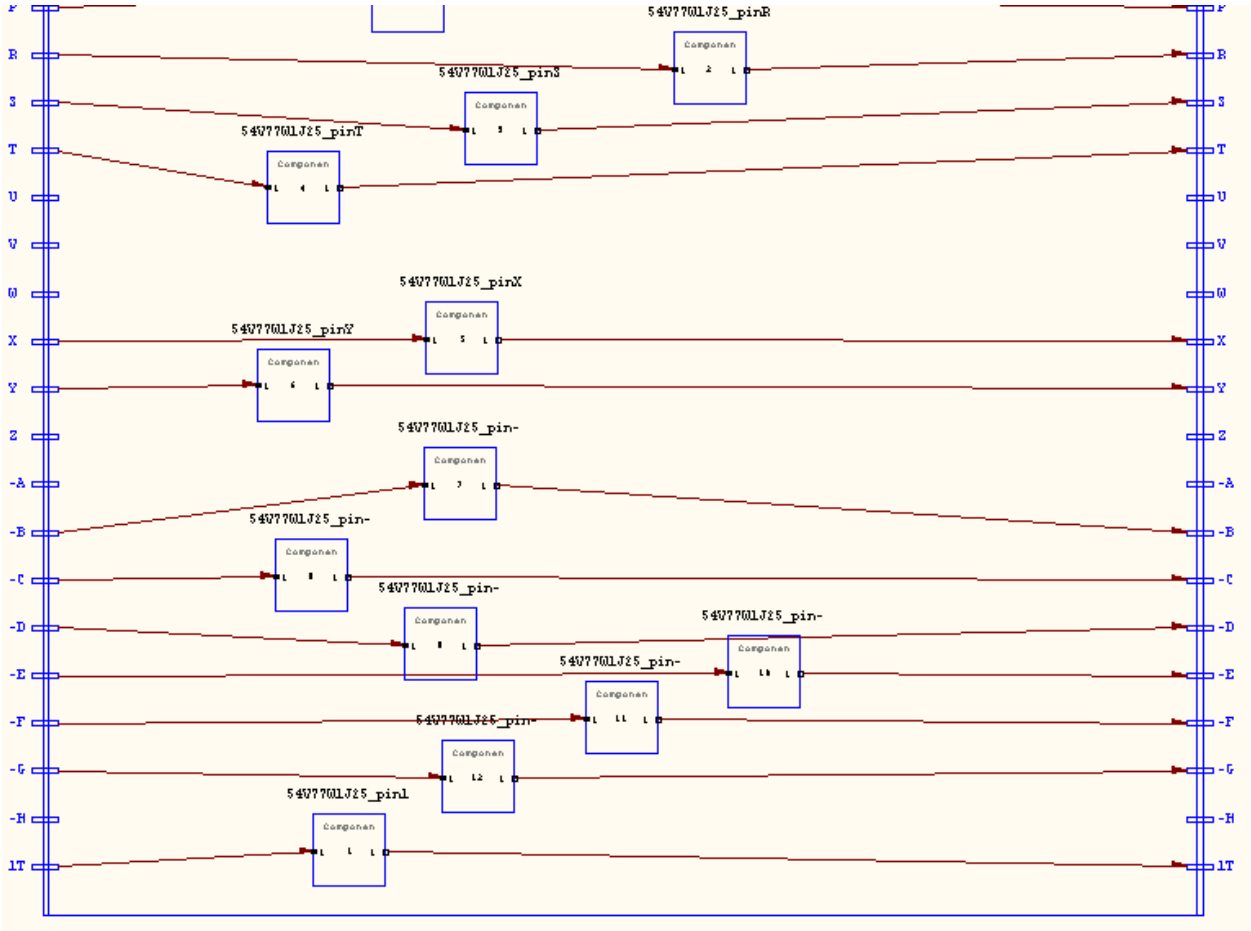

Figure 2: Bottom part of a connector module showing the (wired) pin components.

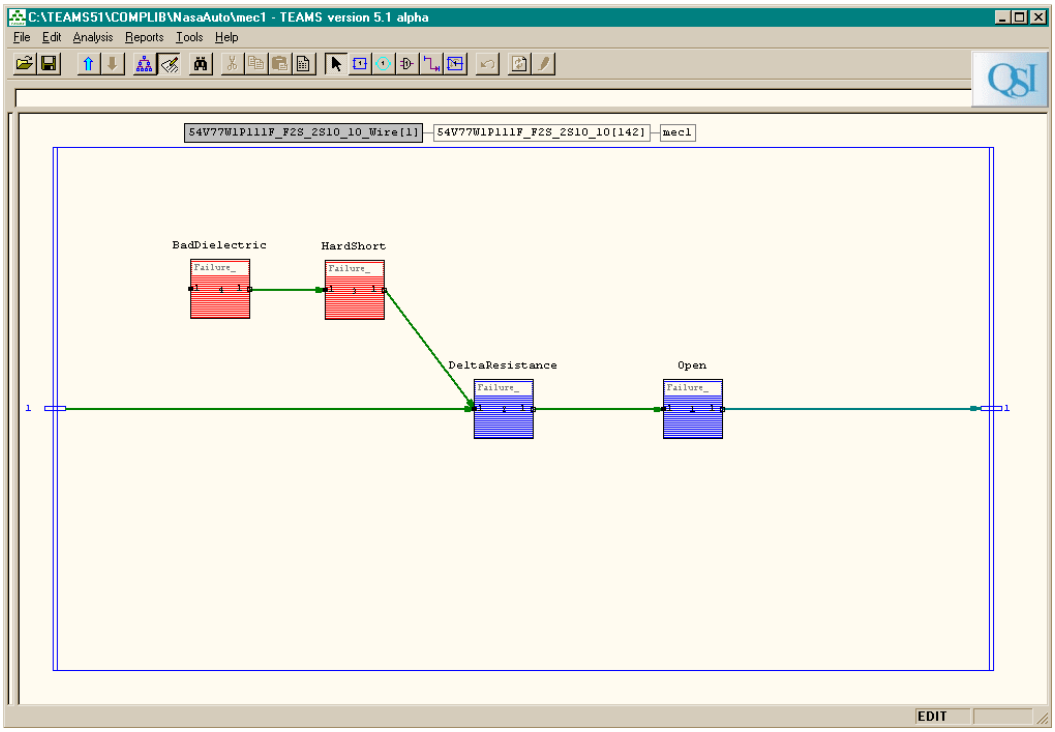

Figure 3: Failure modes of a wire.

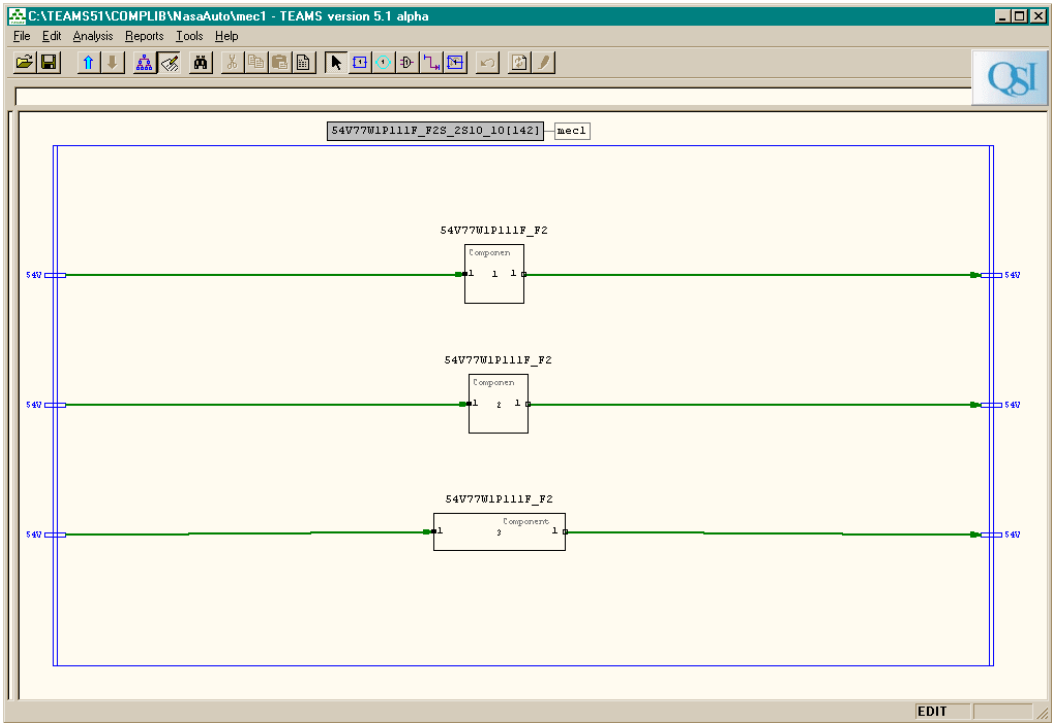

Figure 4: TEAMS model of a two conductor shielded wire.

3.3 Modeling of Mate/Demate status of connectors

The mate/demate status of each connector was modeled using *switches* (see Fig. 5). These *switches* can be opened and closed in TEAMS and TEAMATE/TEAMS-RT to simulate the mated and demated states of the connectors. When connectors are demated, they provide access to the pins and various tests can be performed to assess fault coverage and isolation. We have created System modes, which should be used when running the analysis. The first one is labeled CompleteHarness . Selecting this mode will simulate all connectors being mated to their mating connector with the exception of the last connector in each wire path. Running the analysis in this mode will generally result in large ambiguity groups caused by the inability to fault isolate paths containing multiple wire segments and connectors. The second system mode we have created is called DisconnectAll . Selecting this mode will simulate all connectors being demated, thus allowing testing on the pins of all connectors. Running the analysis in this mode will result in much smaller ambiguity groups. Additional system modes can be defined or changed as needed. If it is known that some connectors in the wiring harness cannot be accessed, then system modes can be defined to allow demating of all but these connectors. In the actual application, the mate/demate status of the connector would be read from SCAN and automatically represented with the proper status in the TEAMS model.

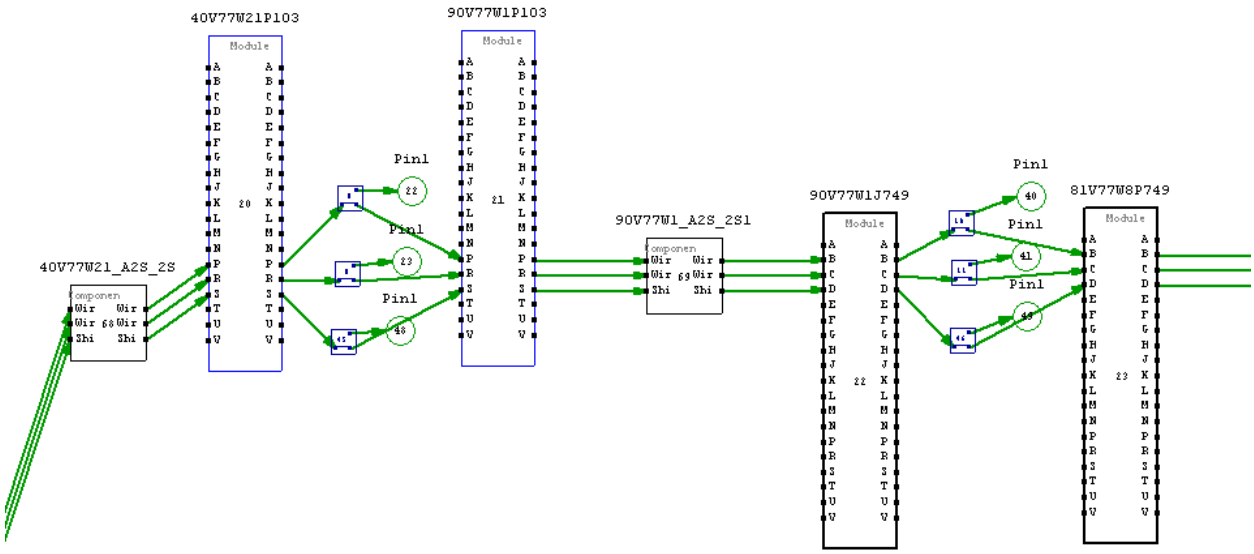

Figure 5: Partial Wiring Harness Model showing switches to model mate/demate status of each connector.

3.4 Modeling of tests

The final step was to add tests to address the failure modes. The tests defined for the wiring model are as follows:

- Continuity – To detect open wires and pushed pins
- Isolation – Involves shorting all other pins to ground and then measuring resistance between the pin being tested and ground to assure pin is isolated from all other pins and ground.

- Delta Resistance – Involves measuring DC resistance through a wire path and comparing it to a predetermined limit. It will detect open wires, pushed pins, and high resistance paths caused by corroded pins, poor contact with mating pins, and broken or frayed wires making partial contact. It will also detect wires shorted to ground. However, based on the feedback at our review meeting, we disabled these tests, as they are currently not part of the standard test procedures.
- Complex Impedance – This test will detect changes in resistance (wire shorts, opens and degradations) and reactance (degradation in insulation leading to capacitive coupling).
- DWV (Dielectric Withstanding Voltage) – Similar to Isolation test except a voltage signal is applied and gradually increased to detect wire or pin breakdown.

4. Testability Analysis Results

Testability analysis was performed using TEAMS to produce reports that provide failure mode coverage metrics and generate optimized test strategy. The results of the analysis are presented in a number of formats. The primary testability report is the Testability Figures Of Merit Summary (TFOMS) Report. The TFOMS Report for the MEC1 wiring model is illustrated in Fig. 6.

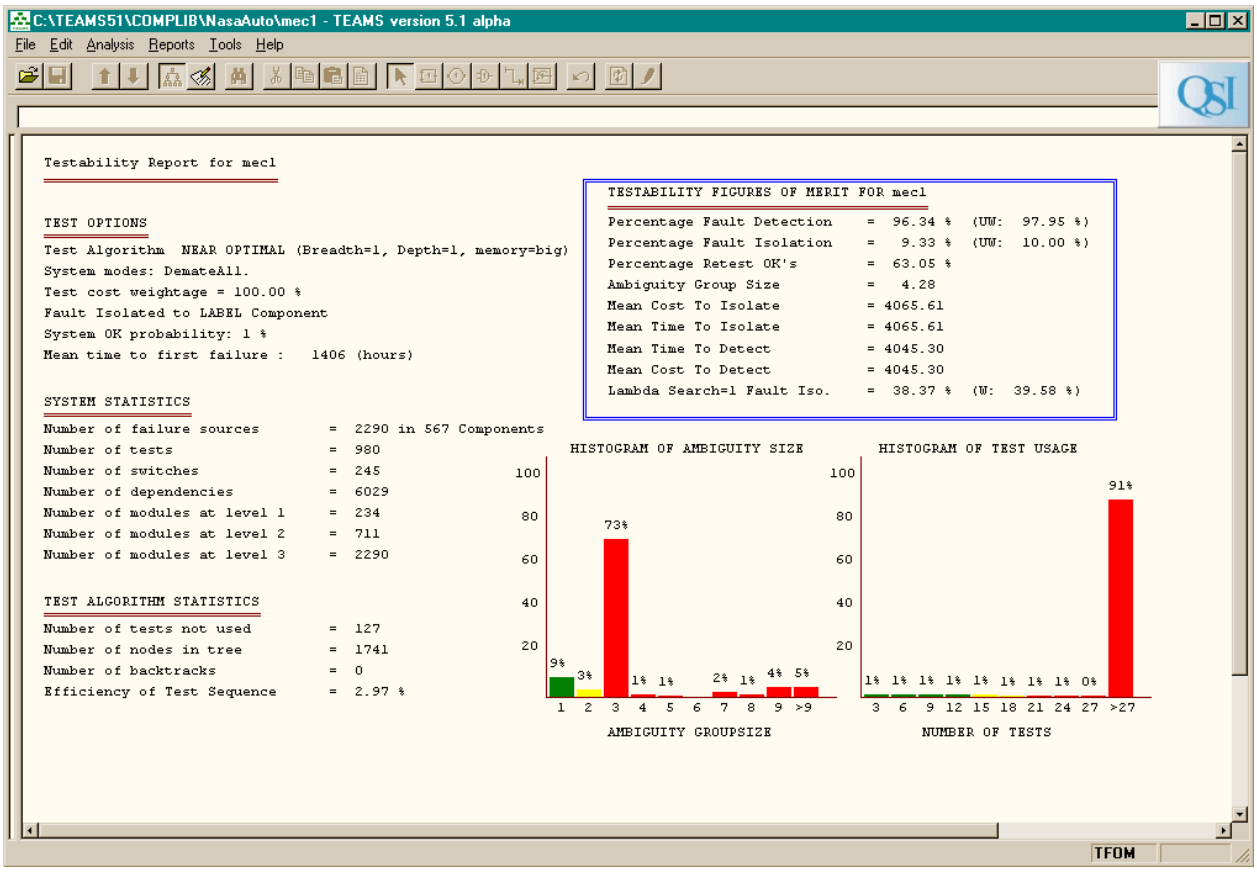

Figure 6: TFOM Summary for the MEC1 wiring model

The failure rates of the individual wires and connectors were set to 1 per million hours. However, with the sheer number of wires and pins, the mean time to first failure is 1406 hours. Such parameters, along with estimates of time and cost associated with tests can be adjusted based on field MTTF and experience and then used to optimize the troubleshooting strategies of TEAMS.

The Test Options section of the TFOMs report lists the options we for the analysis. System Statistics provides the model details. The Test Algorithm Statistics provides a list of information about the resulting test strategy. The TFOMs box present the Percentage Fault Detection or Fault Coverage (see Appendix B for a partial listing of uncovered faults) and Percentage Fault Isolation metrics. The most important information provided by the TFOMS Report is the bar graph entitled Histogram of Ambiguity Size . The histogram provides a graph of the relative number of ambiguity group sizes. The list of specific components comprising the individual ambiguity groups is provided in the Ambiguity Groups (dynamic) test report (see Fig. 7 and Appendix C). The analysis indicates a large number of ambiguity groups comprised of three components. This is due to the fact that most wire paths in the sub harnesses are comprised of a wire with a pin at either end. If it was necessary to break this ambiguity further, Time Domain Reflectometer (TDR) tests could be used to isolate the failure to a single component. Such tests can be modeled easily in TEAMS, but were left out of the model to reflect current test procedures practiced by NASA.

TEAMS also generates an optimized test strategy represented in a diagnostic tree. Figure 8 illustrates a partial view of the diagnostic tree for the MEC1 wiring model. The optimized strategy generated by TEAMS involves over 1000 steps and would be an enormous task if it were to be generated manually. A small segment of the tree is presented in Appendix D.

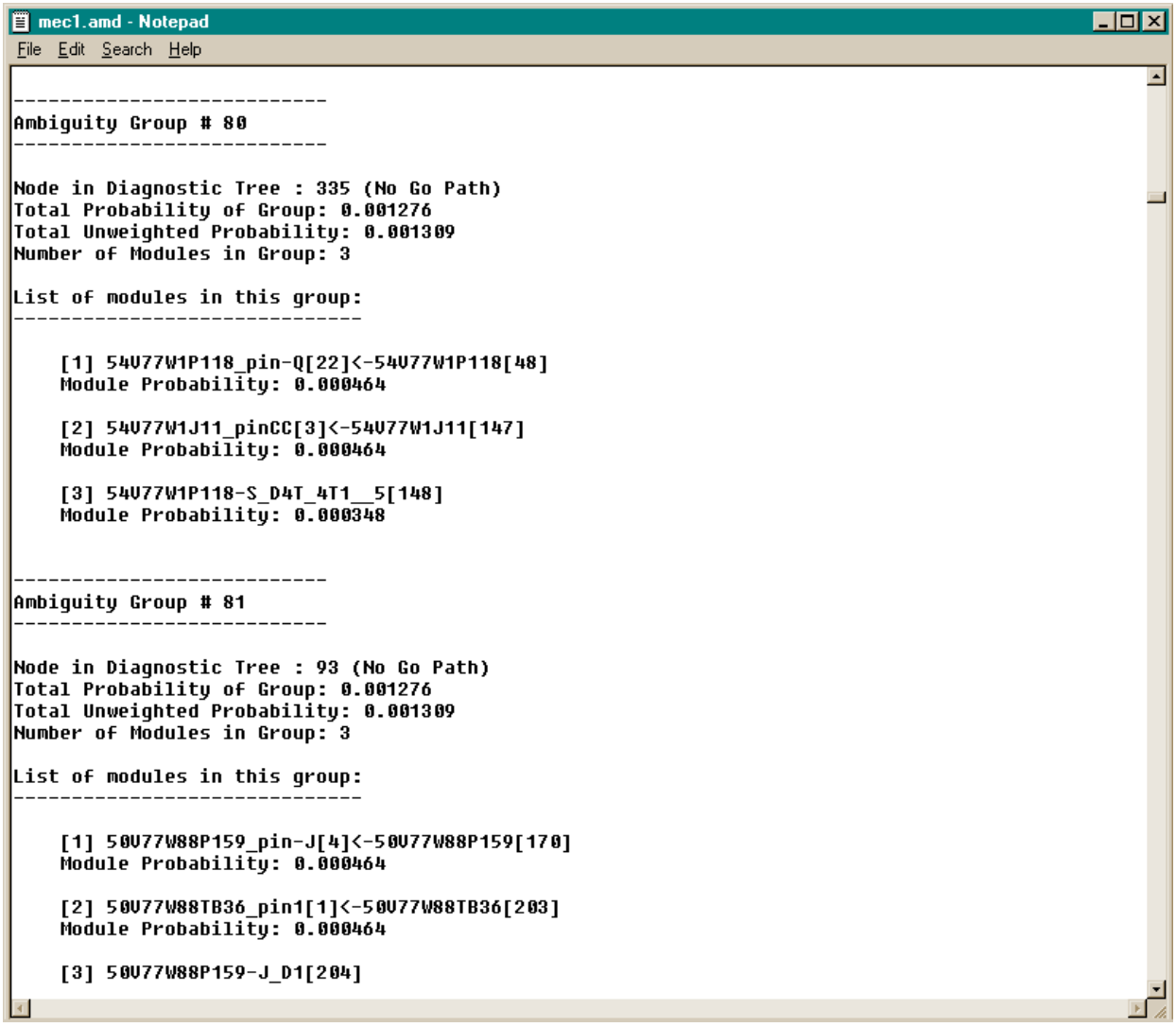

Figure 7: Ambiguity Groups Report for MEC1 J3 connector wiring model

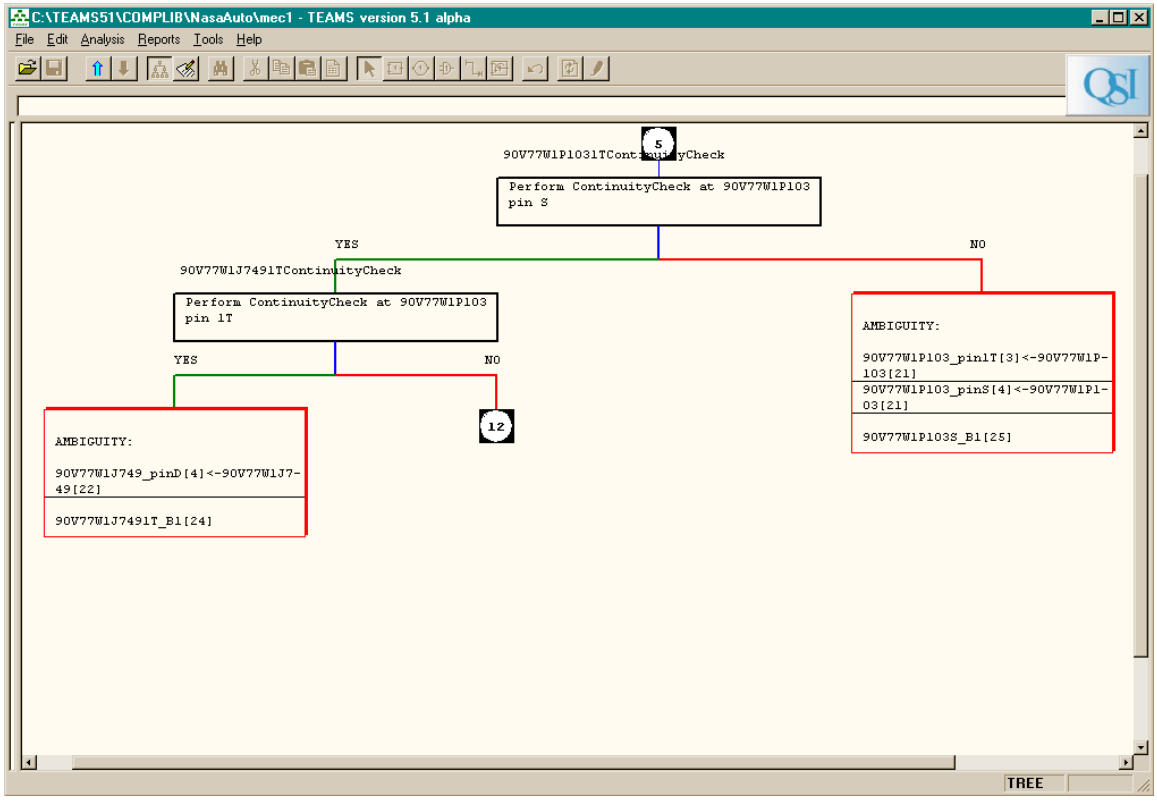

Figure 8: Partial view of Diagnostic Tree for MEC1 wiring model

5. The Review Meetings

Two iterations of the MEC1-J3 harness model were submitted to the WIRe team at NASA-ARC for review on April 12th and 19th. Tele-conferences were held to discuss the source information, models and assumptions. A final review meeting was conducted on May 8, 2000 at NASA-ARC. Peer review and feedback from domain experts are invaluable in improving the fidelity of the models. For example, based on feedback received in the final review meeting, the model was revised to accommodate isolation and Dielectric Withstanding Voltage tests consistent with current testing practices.

From the review process, it became clear that NASA was more concerned with coverage of wires than with fault isolation. Several interesting questions were raised by the WIRe team members that merit further exploration. The following captures the essence of these questions and the answers provided:

- **Question 1**: Given the mate and demate states of the connectors, how can one assess the maximum achievable fault coverage? TEAMS analysis computes the percentage fault detection and isolation, but it does not enumerate the covered and uncovered wires.
- **Question 2**: Connector 5 will be demated Tuesday for repairs. If I test all cable runs accessible through connector 5, what percent of all cable runs will I have tested?

  Answer: Fortunately, this problem can be solved utilizing our existing tools. Figure 9 presents a screendump of TEAMS-RT, which takes a fraction of a second to compute the numbers for the MEC1 model. The top half of the screen shows the list of failure modes (left column) and the

mate-demate status (right column). The lower half of the screen shows the components that will be covered (Good) and still untested (Unknown) if testing were to be performed utilizing the current configuration of connectors. The Modes, or Mate/Demate status can be set programmatically from SCAN database. Also, if the tests were performed and pass/fail tests results submitted to TEAMS-RT, it would also be able to compute the Bad and suspected components, still within a second of processing time. TEAMS-RT, when combined with TEAMS-KB, can also retain the state of the system, and quantify incremental test coverage, as more and more connectors are demated and tested. In addition, TEAMATE can be used to guide the technician(s) and expedite the testing process.

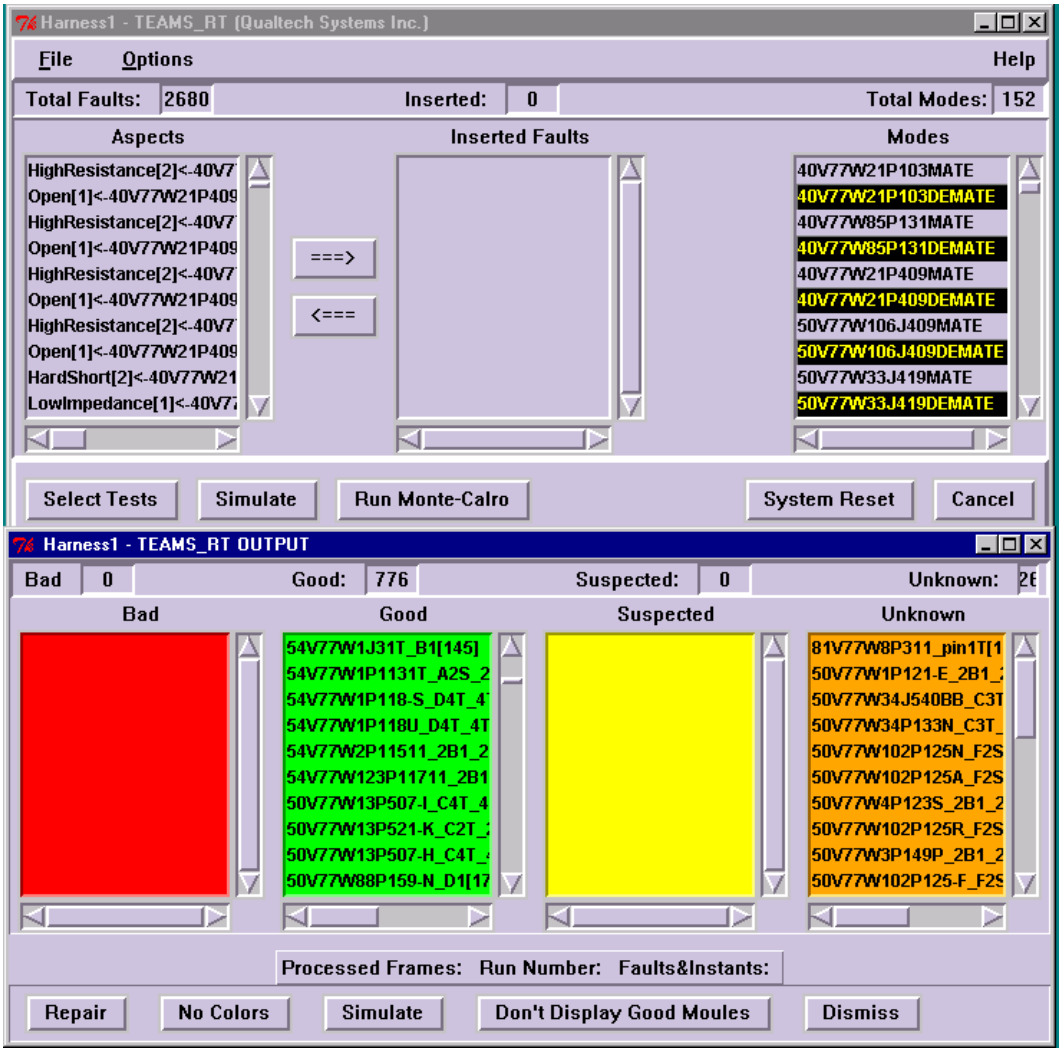

Figure 9: Screendump of TEAMS-RT assessing fault coverage for MEC1 system.

- **Question 4**: Given a wire network and given enough time to demate/test 2 connectors only, which connectors do I demate and test to maximize the number of cable runs tested?
- **Question 5**: I need to test the circuit containing run E. Which connector pair do I demate to access E, but use opportunities to test maximum number of other cable runs
- **Question 6**: Suppose connector 8 is hidden and inaccessible. What is the greatest number of wire runs I can possibly tests? How many connectors must I demate?

- **Question 7**: What are the fewest number of connectors demated to test all wire runs?

  Answer: All of the above questions, can be easily formulated as set-covering problems subject to constraints (e.g., inaccessible connectors, cost/time budget) and efficient search algorithms can be developed to solve the problems. The models and TEAMS-RT's ability to evaluate coverage will be essential components required for evaluation of the cost function to be optimized by the search process. While there is no off-the-shelf solution to these questions, we feel confident we can address these issues given the opportunity in the near future.

We also demonstrated a web-based version of TEAMATE that can guide the technician through the test process (see Fig. 11). The test ac

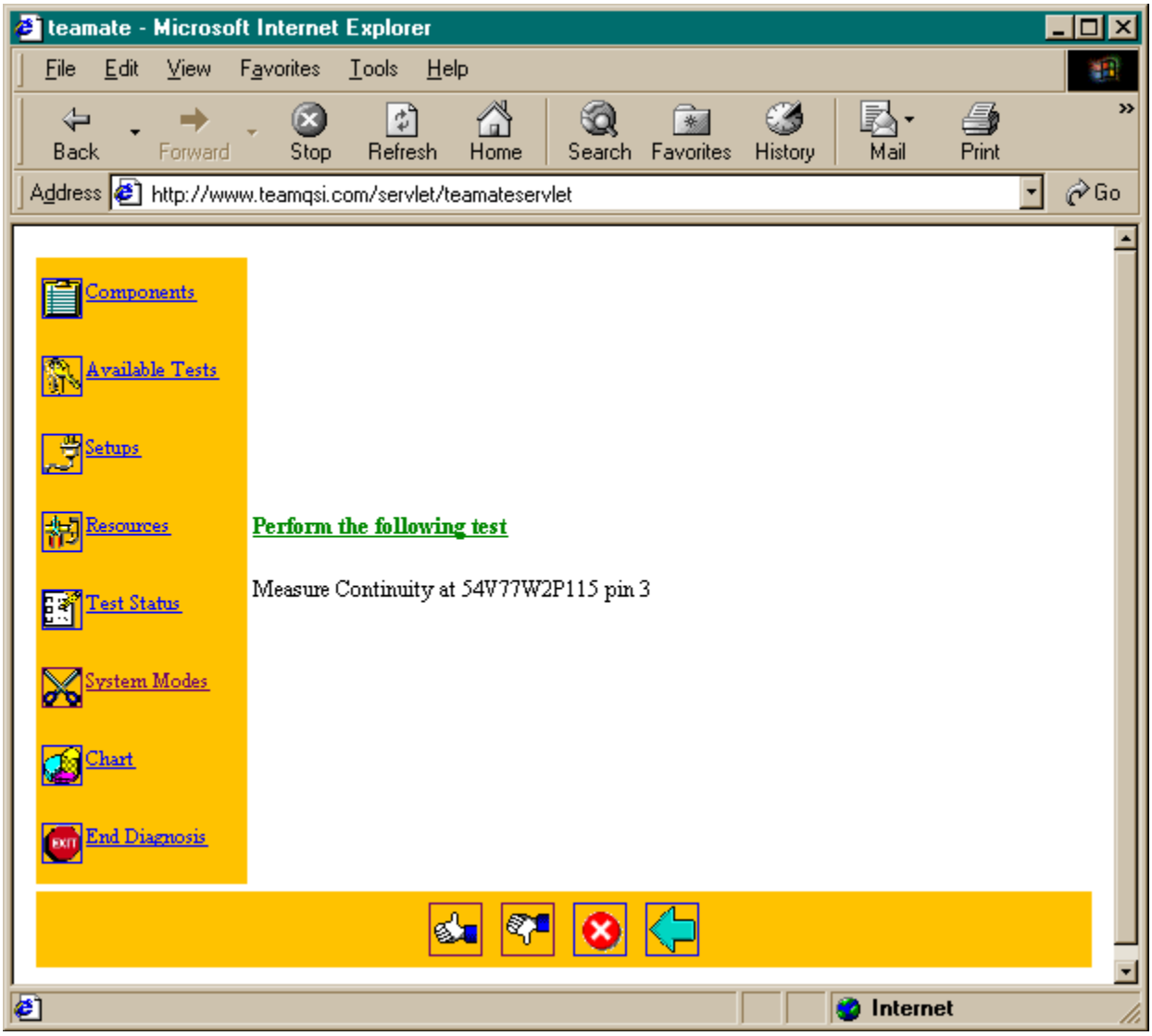

Figure 10: Screendump of a Web-based TEAMATE diagnosis session.

This project established the methodology for creation of a multi-signal TEAMS model of a typical space-shuttle wiring circuit of medium complexity. The process started creating the individual components of the system, and then added dependency paths that closely followed actual

interconnectivity. A partial block diagram of the MEC1 J3 connector harness, as modeled with TEAMS, is depicted in Figure 11.

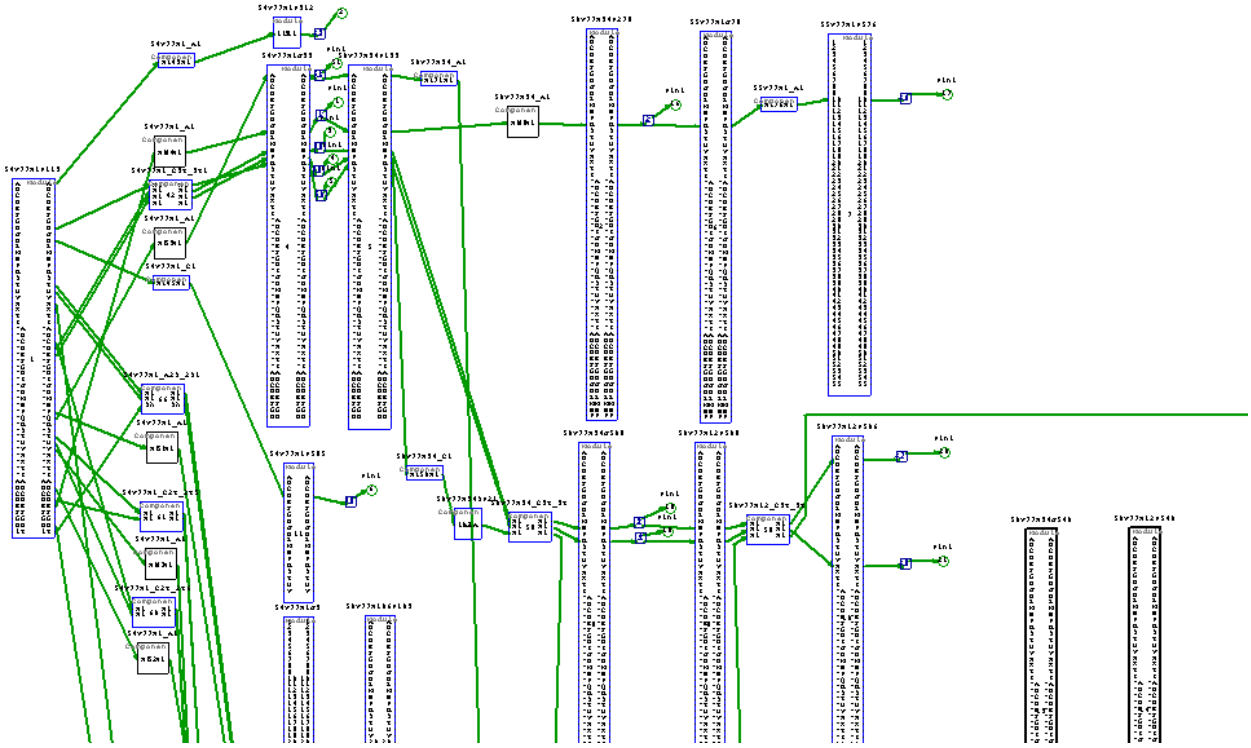

Figure 11: Segment of MEC1 J3 TEAMS Model Generated from SCAN data

By establishing some basic rules on wire failure modes and test methods, QSI was able to automatically create a MEC1 wiring assembly model in TEAMS. The many features available with the TEAMS tool helped to greatly simplify the task and perform the analysis. The resulting model closely resembles the physical structure of the wiring circuit, thus allowing updates to be made quickly and easily.

This project illustrated how TEAMS can be used to assess testing methods and to create a diagnostic strategy tailored to specific needs. QSI demonstrated that the run-time tools, TEAMS-RT and TEAMATE, can handle the analysis and runtime of the MEC1 subsystem in a simple laptop computer — and feel confident that theresolution will scale to about two orders of magnitude higher than the MEC1 model. We look forward to the opportunity to work with NASA in addressing the challenges in comprehensive testing and quality assurance of the space shuttle and other aging aircraft.

Based on the work accomplished in the pilot project, the following recommendations are provided:

APPENDIX A

Overview of TEAMS Integrated Toolset

The TEAMS Integrated Diagnostics Toolset

QSI s integrated tool set, consisting of nearly a million lines of C, C++ and Java code, automates the tasks of Design for Testability (DFT), Reliability Analysis, Failure Modes and Effects Criticality Analysis (FMECA), on-line monitoring and off-line diagnosis (see Fig. XX). The software tool set consists of:

- TEAMS 5.0: Testability assessment and improvement (DFT) , Reliability analysis, FMECA and pre-computed diagnostic test strategy generation in a variety of forms (e.g., XML-based Interactive Electronic Technical Manual);
- TEAMS-RT: onboard diagnostics, health and usage monitoring systems;
- TEAMATE: Portable Intelligent Maintenance Aids (PIMAs) with interactive electronic technical manuals and multi-media animation, dynamic Test Program Sets (TPSs) for ATEs.
- TEAMS-KB: Scheduled and unscheduled maintenance and diagnostics data collection, statistical data analysis and data mining for trend and anomaly detection/isolation.

Each of these functional modules are briefly described in the following subsections.

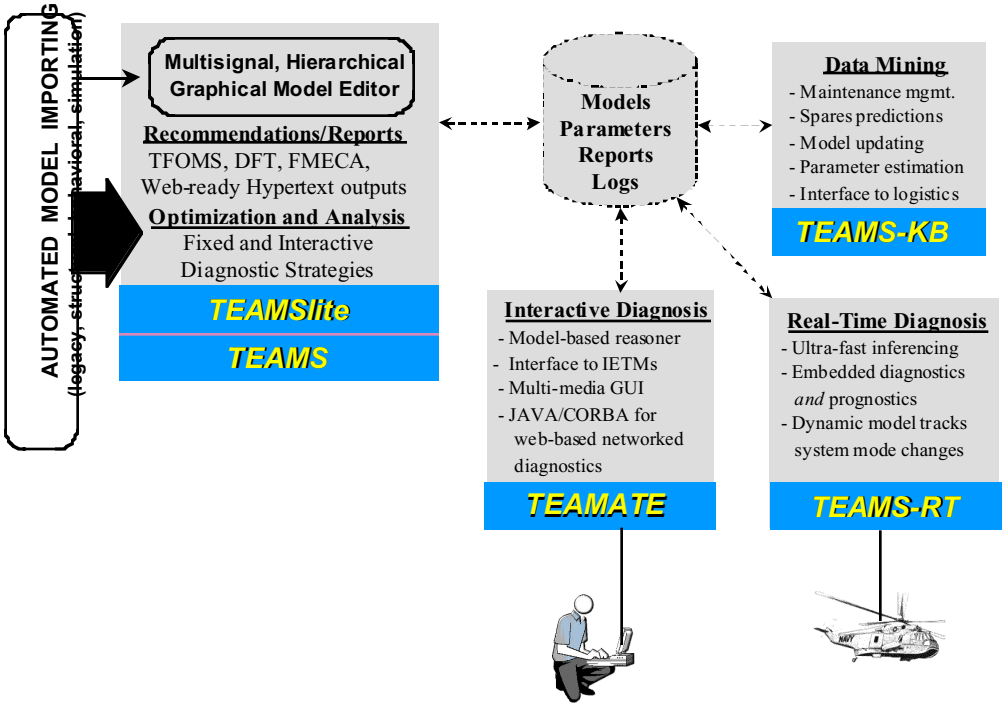

Figure 12: TEAMS Integrated Toolset with application to Integrated Diagnosis

TEAMS- The modeling and Analysis Environment

The ability to model and predict the failure behavior and resultant effect on the system is first and foremost in the development of an effective diagnostic and prognostic capability. The engineer must be able to see how the system will fail and then determine how to address the failure. For a given failure mode, the engineer must be given tools to help optimize the diagnostic/prognostic approach within the specification requirements for safety, mission reliability, system cost, weight, support costs, etc. The Testability Engineering and Maintenance System (TEAMS) software tool forms the foundation for this aspect of the project.

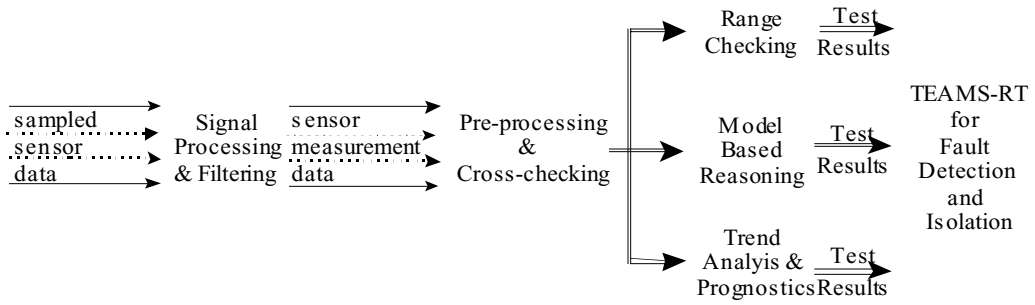

Figure 13 - Sensor signal preprocessing for a local *TEAMS-RT* module.

TEAMS-RT: On-board real-time diagnostics and prognostics.

Once the models have been created in TEAMS, and the design is optimized for diagnostics and prognostics, the TEAMS model along with its test specifications can be exported to the TEAMS-RT (RT stands for run-time) software tool. This is a seamless process within the integrated tools set. The TEAMS-RT based reasoning engine can efficiently process pass/fail outcomes of thousands of tests in a fraction of a second to assess the health of the system. It will, therefore, form the heart of our on-board diagnostics/prognostics health management solution. It, however, needs test decisions to assess system health. Thus, raw sensor data needs to be processed and converted into the binary pass/fail format required by the diagnostic engine. A modular signal-processing library, developed under contract by University of Connecticut, enables us to easily add new tests. The SP toolkit provides us with a flexible and versatile means of implementing a variety of test procedures, prognosis and trending algorithms, including sophisticated extraction of statistical features to support hypothesis testing and pattern recognition. Currently, the signal processing tool-kit contains a library of several noise filtering, basic spectral analysis, and statistical routines, as well as more specialized capabilities that include wavelets (Daubechies prototype), autoregressive spectral methods, and nonlinear transformations. The tool-kit is designed to be a continuously evolving library that can be customized to a target environment by simply modifying configuration files to expose the appropriate functions. QSI and the UConn continue to develop new and innovative prognostic routines to significantly improve the capabilities of the tool-kit.

A typical schematic of the preprocessing module is shown in Fig. XX. The task of the first stage would be to minimize the effects of noise by suitable filtering. The next stage would perform functional and heuristic cross-checks to exploit hardware and functional redundancies in the system to reduce, and possibly eliminate, erroneous, contradictory or duplicate sensor results. The third stage is the decision stage. In commonly occurring cases, the detection of anomalies simply involves comparing (de-noised) scalar signals to predefined thresholds for exceedances (Range Checking). In many complex systems, however, sensor signals cannot be de-linked and viewed independently of one another. In such cases, the vector of raw sensor signals (or the vector of features extracted from raw signals) must be correlated against an analytically derived pattern (Model based reasoning). Finally, the trend analysis and prognostics sub-module would monitor slow degradation in sensor signals. Often, the sensor data would need to be classified into one of a set of normal and anomalous categories, e.g., to assess the degree of degradation. Examples of classifiers include Neural networks/Multilayer perceptron (MLP), the Radial Basis Function (RBF), the Class Specific Classifier, and Bayesian Data Reduction etc. The resultant test decisions are processed by TEAMS-RT in real-time to assess system health, i.e., identify healthy components and isolate failing and

failed components. The architecture described in Fig. XX is data driven and configured by system models and test scripts.

TEAMS-KB: Ground Based Maintenance Management to Support Diagnostics and Prognostics.

This aspect of our approach involves the application of advanced computerized maintenance management systems to collect, analyze, trend, and project maintenance requirements. The TEAMS-KB tool is the basis for this portion of the system. TEAMS-KB provides capabilities to update a system s component reliabilities and failure rates in response to cumulative maintenance and repair data. TEAMS-KB can be used to track component usage and provide plots of life remaining (Fig. XX) against a number of maintenance/logistics parameters such as future mission reliability, spares consumption, support equipment needs, personnel needs/training, etc.

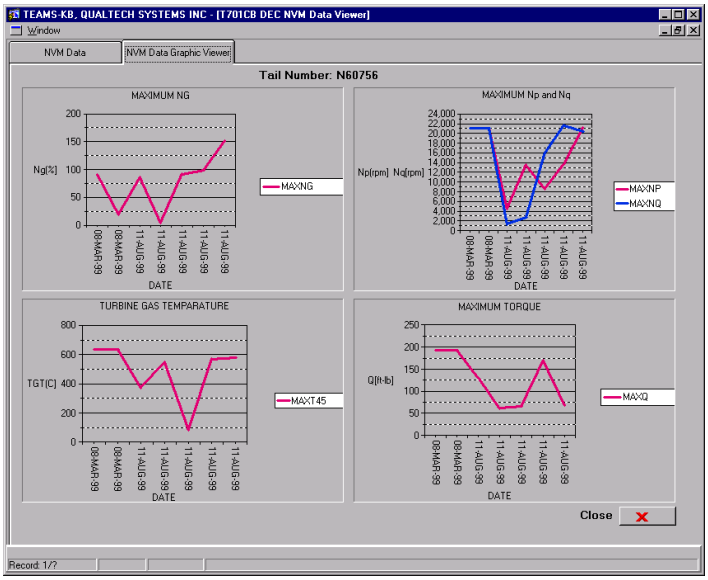

Figure 14: TEAMS-KB: Trending analysis of a helicopter engine performance data.

TEAMATE: Interactive diagnostics/prognostics for efficient maintenance

This is the final step in the seamless process of Integrated Diagnosis and closes the loop on the entire diagnostic/prognostic process. TEAMATE provides the smarts behind Interactive Electronic Technical Manual (IETM). It interacts and guides the operator through a dynamically optimized repair procedure, and presents the appropriate tests and setup instructions to the operator by displaying multimedia instructions from the technical manuals (see Fig. XX).

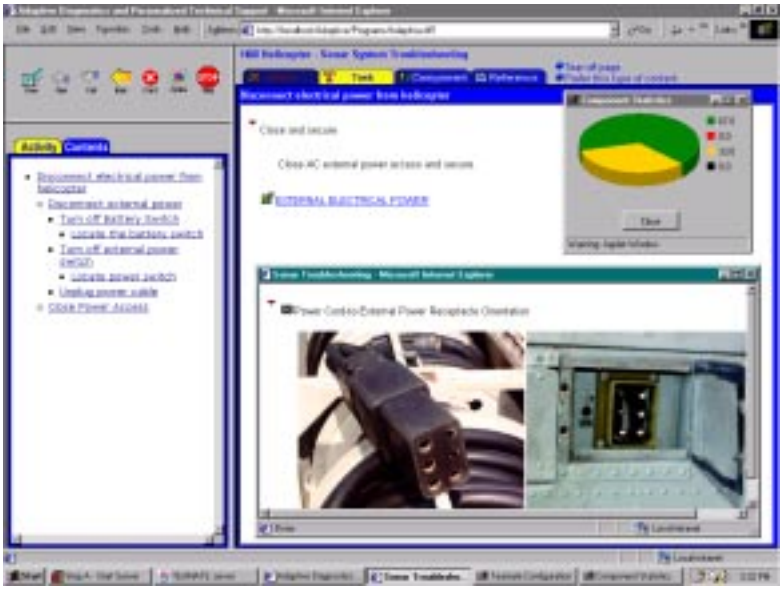

Figure 15: Example of the TEAMATE-IETM Environment on a Portable Maintenance Computer

APPENDIX B

Abbreviated Undetected Faults report for MEC1 wiring system

TEAMS: Testability Engineering and Maintenance System

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UNDETECTED FAULTS FOR
mec1

Wed May 17 15:42:47 2000

The following is a set of faults that are undetectable.

40V77W21P409[1]
- 40V77W21P409_pin47[1]
  - PinCorrosion[2]
  - PushedPin[1]
  - BentPin[3]
- 40V77W21P409_pin1T[2]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 40V77W21P409_pin48[3]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 40V77W21P409_pin46[4]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]

40V77W21P103[2]
- 40V77W21P103_pinR[1]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 40V77W21P103_pin1T[2]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 40V77W21P103_pinS[3]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 40V77W21P103_pinP[4]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]

40V77W21P40947_A2S_2S1__10[3]
- 40V77W21P40947_A2S_2S1__10_Shield[3]
  - BrokenShield[1]
- 40V77W21P40947_A2S_2S1__10_Wire[2]
  - BadDielectric[4]
  - HardShort[3]
  - DeltaResistance[2]
  - Open[1]
- 40V77W21P40947_A2S_2S1__10_Wire[1]
  - Open[1]
  - DeltaResistance[2]
  - HardShort[3]

BadDielectric[4]
40V77W21P1031T_B1[4]
40V77W21P1031T_B1_Wire[1]
BadDielectric[4]
HardShort[3]
DeltaResistance[2]
Open[1]
40V77W85P419[5]
40V77W85P419_pin125[1]
BentPin[3]
PinCorrosion[2]
PushedPin[1]
40V77W85P419_pin127[2]
BentPin[3]
PinCorrosion[2]
PushedPin[1]
40V77W85P131[6]
40V77W85P131_pin59[1]
BentPin[3]
PinCorrosion[2]
PushedPin[1]
40V77W85P131_pin61[2]
BentPin[3]
PinCorrosion[2]
PushedPin[1]
40V77W85P419125_C3T_3T1__1[7]
40V77W85P419125_C3T_3T1__1_Wire[3]
BadDielectric[4]
HardShort[3]
DeltaResistance[2]
Open[1]
40V77W85P419125_C3T_3T1__1_Wire[2]
Open[1]
DeltaResistance[2]
HardShort[3]
BadDielectric[4]
40V77W85P419125_C3T_3T1__1_Wire[1]
BadDielectric[4]
HardShort[3]
DeltaResistance[2]
Open[1]
40V77W21P40948_B1[8]
40V77W21P40948_B1_Wire[1]
BadDielectric[4]
HardShort[3]
DeltaResistance[2]
Open[1]
50V77W106J409[9]
50V77W106J409_pin1T[1]
BentPin[3]
PinCorrosion[2]
PushedPin[1]
50V77W106J409_pin48[2]
BentPin[3]
PinCorrosion[2]
PushedPin[1]

- 50V77W106J409_pin47[3]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 50V77W106J409_pin46[4]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]

50V77W106J4091T_B1[10]
- 50V77W106J4091T_B1_Wire[1]
  - BadDielectric[4]
  - HardShort[3]
  - DeltaResistance[2]
  - Open[1]

50V77W33P183[11]
- 50V77W33P183_pin71[1]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 50V77W33P183_pin73[2]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 50V77W33P183_pin67[3]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 50V77W33P183_pin78[4]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]

50V77W33J419[12]
- 50V77W33J419_pin125[1]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]
- 50V77W33J419_pin127[2]
  - BentPin[3]
  - PinCorrosion[2]
  - PushedPin[1]

50V77W33P18371_C3T_3T1__1[13]
- 50V77W33P18371_C3T_3T1__1_Wire[3]
  - BadDielectric[4]
  - HardShort[3]
  - DeltaResistance[2]
  - Open[1]
- 50V77W33P18371_C3T_3T1__1_Wire[2]
  - Open[1]
  - DeltaResistance[2]
  - HardShort[3]
  - BadDielectric[4]
- 50V77W33P18371_C3T_3T1__1_Wire[1]
  - BadDielectric[4]
  - HardShort[3]
  - DeltaResistance[2]
  - Open[1]

- 50V77W33P171[14]
  - 50V77W33P171_pinE[1]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pinF[2]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pinG[3]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pinH[4]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-A[5]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-B[6]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pinA[7]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pinB[8]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pinD[9]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-E[10]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-F[11]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-G[12]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-H[13]
    - BentPin[3]
    - PinCorrosion[2]
    - PushedPin[1]
  - 50V77W33P171_pin-I[14]
    - BentPin[3]
    - PinCorrosion[2]

PushedPin[1]
50V77W33P171_pin-J[15]
BentPin[3]
PinCorrosion[2]
PushedPin[1]
50V77W33P171_pin-K[16]
BentPin[3]
PinCorrosion[2]
PushedPin[1]

APPENDIX C

Abbreviated Ambiguity group report for MEC1 wiring system

TEAMS: Testability Engineering and Maintenance System

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AMBIGUITY GROUPS REPORT FOR
mec1

Wed May 17 15:42:47 2000

Ambiguity Group # 1

Node in Diagnostic Tree : 870 (Go Path)
Total Probability of Group: 0.046202
Total Unweighted Probability: 0.020952
Number of Modules in Group: 26

List of modules in this group:
---

[1] All_Systems_Go
Module Probability: 0.010000

[2] 50V77W34J540BB_C3T_3T1__1A[231]
Module Probability: 0.002785

[3] 50V77W1P121-E_2B1_2S2__2[234]
Module Probability: 0.001392

[4] 50V77W102P818A_D2S_2S1__2[168]
Module Probability: 0.001392

[5] 50V77W34P133N_C3T_3T1__1A[227]
Module Probability: 0.001392

[6] 50V77W102P125N_F2S_2S3__2[223]
Module Probability: 0.001392

[7] 50V77W102P125A_F2S_2S1__1[222]
Module Probability: 0.001392

[8] 50V77W4P123S_2B1_2S1__2[220]
Module Probability: 0.001392

[9] 50V77W102P125R_F2S_2S4__1[210]
Module Probability: 0.001392

[10] 50V77W3P149P_2B1_2S1__2[202]
Module Probability: 0.001392

[11] 50V77W102P125-F_F2S_2S11_1[192]
Module Probability: 0.001392

[12] 50V77W102P125-D_F2S_2S10_1[191]
Module Probability: 0.001392

[13] 50V77W102P125-B_F2S_2S9__2[190]
Module Probability: 0.001392

[14] 50V77W102P125X_F2S_2S7__1[188]
Module Probability: 0.001392

[15] 50V77W102P125S_F2S_2S5__1[186]
Module Probability: 0.001392

[16] 50V77W326P825A_D2S_2S1__1[35]
Module Probability: 0.001392

[17] 50V77W102P817A_D2S_2S1__2[165]
Module Probability: 0.001392

[18] 50V77W12P508N_C3T_3T1__1[159]
Module Probability: 0.001392

[19] 54V77W1P118P_C3T_3T1__7A[118]
Module Probability: 0.001392

[20] 50V77W325P822A_D2S_2S1__1[41]
Module Probability: 0.001392

[21] 50V77W324P821A_D2S_2S1__1[38]
Module Probability: 0.001392

[22] 50V77W328P826A_D2S_2S1__1[28]
Module Probability: 0.001392

[23] 50V77W326P825C_D2S_2S1__2[33]
Module Probability: 0.001392

[24] 50V77W328P826C_D2S_2S1__2[30]
Module Probability: 0.001392

[25] 40V77W85P419125_C3T_3T1__1[7]
Module Probability: 0.001392

[26] 50V77W33P18371_C3T_3T1__1[13]
Module Probability: 0.001392

Ambiguity Group # 2

Node in Diagnostic Tree : 455 (Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W2P115_pin3[1]<-54V77W2P115[96]
Module Probability: 0.000464

[2] 54V77W2P115_pin9[4]<-54V77W2P115[96]
Module Probability: 0.000464

[3] 54V77W2SP12_pin1T[1]<-54V77W2SP12[97]
Module Probability: 0.000464

[4] 54V77W2P115_pin7[3]<-54V77W2P115[96]
Module Probability: 0.000464

[5] 54V77W2P115_pin6[2]<-54V77W2P115[96]
Module Probability: 0.000464

[6] 54V77W2P1153_A1[98]
Module Probability: 0.000348

[7] 54V77W2P1156_A1[99]
Module Probability: 0.000348

[8] 54V77W2P1157_A1[100]
Module Probability: 0.000348

[9] 54V77W2P1159_A1[101]
Module Probability: 0.000348

Ambiguity Group # 3

Node in Diagnostic Tree : 453 (Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W122P116_pin3[1]<-54V77W122P116[102]
Module Probability: 0.000464

[2] 54V77W122P116_pin9[4]<-54V77W122P116[102]
Module Probability: 0.000464

[3] 54V77W122SP14_pin1T[1]<-54V77W122SP14[103]
Module Probability: 0.000464

[4] 54V77W122P116_pin7[3]<-54V77W122P116[102]
Module Probability: 0.000464

[5] 54V77W122P116_pin6[2]<-54V77W122P116[102]
Module Probability: 0.000464

[6] 54V77W122P1163_A1[104]
Module Probability: 0.000348

[7] 54V77W122P1166_A1[105]

Module Probability: 0.000348

[8] 54V77W122P1167_A1[106]
Module Probability: 0.000348

[9] 54V77W122P1169_A1[109]
Module Probability: 0.000348

Ambiguity Group # 4

Node in Diagnostic Tree : 32 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W122P116_pin3[1]<-54V77W122P116[102]
Module Probability: 0.000464

[2] 54V77W122P116_pin9[4]<-54V77W122P116[102]
Module Probability: 0.000464

[3] 54V77W122SP14_pin1T[1]<-54V77W122SP14[103]
Module Probability: 0.000464

[4] 54V77W122P116_pin7[3]<-54V77W122P116[102]
Module Probability: 0.000464

[5] 54V77W122P116_pin6[2]<-54V77W122P116[102]
Module Probability: 0.000464

[6] 54V77W122P1163_A1[104]
Module Probability: 0.000348

[7] 54V77W122P1166_A1[105]
Module Probability: 0.000348

[8] 54V77W122P1167_A1[106]
Module Probability: 0.000348

[9] 54V77W122P1169_A1[109]
Module Probability: 0.000348

Ambiguity Group # 5

Node in Diagnostic Tree : 31 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W122P116_pin3[1]<-54V77W122P116[102]
Module Probability: 0.000464

[2] 54V77W122P116_pin9[4]<-54V77W122P116[102]
Module Probability: 0.000464

[3] 54V77W122SP14_pin1T[1]<-54V77W122SP14[103]
Module Probability: 0.000464

[4] 54V77W122P116_pin7[3]<-54V77W122P116[102]
Module Probability: 0.000464

[5] 54V77W122P116_pin6[2]<-54V77W122P116[102]
Module Probability: 0.000464

[6] 54V77W122P1163_A1[104]
Module Probability: 0.000348

[7] 54V77W122P1166_A1[105]
Module Probability: 0.000348

[8] 54V77W122P1167_A1[106]
Module Probability: 0.000348

[9] 54V77W122P1169_A1[109]
Module Probability: 0.000348

Ambiguity Group # 6

Node in Diagnostic Tree : 30 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W123P117_pin7[1]<-54V77W123P117[44]
Module Probability: 0.000464

[2] 54V77W123P117_pin3[4]<-54V77W123P117[44]
Module Probability: 0.000464

[3] 54V77W123SP18_pin1T[1]<-54V77W123SP18[45]
Module Probability: 0.000464

[4] 54V77W123P117_pin6[3]<-54V77W123P117[44]
Module Probability: 0.000464

[5] 54V77W123P117_pin9[2]<-54V77W123P117[44]
Module Probability: 0.000464

[6] 54V77W123P1177_A1[46]
Module Probability: 0.000348

[7] 54V77W123P1179_A1[47]
Module Probability: 0.000348

[8] 54V77W123P1176_A1[76]
Module Probability: 0.000348

[9] 54V77W123P1173_A1[110]
Module Probability: 0.000348

Ambiguity Group # 7

Node in Diagnostic Tree : 29 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W123P117_pin7[1]<-54V77W123P117[44]
Module Probability: 0.000464

[2] 54V77W123P117_pin3[4]<-54V77W123P117[44]
Module Probability: 0.000464

[3] 54V77W123SP18_pin1T[1]<-54V77W123SP18[45]
Module Probability: 0.000464

[4] 54V77W123P117_pin6[3]<-54V77W123P117[44]
Module Probability: 0.000464

[5] 54V77W123P117_pin9[2]<-54V77W123P117[44]
Module Probability: 0.000464

[6] 54V77W123P1177_A1[46]
Module Probability: 0.000348

[7] 54V77W123P1179_A1[47]
Module Probability: 0.000348

[8] 54V77W123P1176_A1[76]
Module Probability: 0.000348

[9] 54V77W123P1173_A1[110]
Module Probability: 0.000348

Ambiguity Group # 8

Node in Diagnostic Tree : 451 (Go Path)

Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W123P117_pin7[1]<-54V77W123P117[44]
Module Probability: 0.000464

[2] 54V77W123P117_pin3[4]<-54V77W123P117[44]
Module Probability: 0.000464

[3] 54V77W123SP18_pin1T[1]<-54V77W123SP18[45]
Module Probability: 0.000464

[4] 54V77W123P117_pin6[3]<-54V77W123P117[44]
Module Probability: 0.000464

[5] 54V77W123P117_pin9[2]<-54V77W123P117[44]
Module Probability: 0.000464

[6] 54V77W123P1177_A1[46]
Module Probability: 0.000348

[7] 54V77W123P1179_A1[47]
Module Probability: 0.000348

[8] 54V77W123P1176_A1[76]
Module Probability: 0.000348

[9] 54V77W123P1173_A1[110]
Module Probability: 0.000348

Ambiguity Group # 9

Node in Diagnostic Tree : 28 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W121P114_pin3[1]<-54V77W121P114[88]
Module Probability: 0.000464

[2] 54V77W121P114_pin9[4]<-54V77W121P114[88]
Module Probability: 0.000464

[3] 54V77W121SP6_pin1T[1]<-54V77W121SP6[89]
Module Probability: 0.000464

[4] 54V77W121P114_pin7[3]<-54V77W121P114[88]
Module Probability: 0.000464

[5] 54V77W121P114_pin6[2]<-54V77W121P114[88]
Module Probability: 0.000464

[6] 54V77W121P1143_A1[90]
Module Probability: 0.000348

[7] 54V77W121P1146_A1[91]
Module Probability: 0.000348

[8] 54V77W121P1147_A1[92]
Module Probability: 0.000348

[9] 54V77W121P1149_A1[93]
Module Probability: 0.000348

Ambiguity Group # 10

Node in Diagnostic Tree : 27 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W121P114_pin3[1]<-54V77W121P114[88]
Module Probability: 0.000464

[2] 54V77W121P114_pin9[4]<-54V77W121P114[88]
Module Probability: 0.000464

[3] 54V77W121SP6_pin1T[1]<-54V77W121SP6[89]
Module Probability: 0.000464

[4] 54V77W121P114_pin7[3]<-54V77W121P114[88]
Module Probability: 0.000464

[5] 54V77W121P114_pin6[2]<-54V77W121P114[88]
Module Probability: 0.000464

[6] 54V77W121P1143_A1[90]
Module Probability: 0.000348

[7] 54V77W121P1146_A1[91]
Module Probability: 0.000348

[8] 54V77W121P1147_A1[92]
Module Probability: 0.000348

[9] 54V77W121P1149_A1[93]
Module Probability: 0.000348

Ambiguity Group # 11

Node in Diagnostic Tree : 25 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W2P115_pin3[1]<-54V77W2P115[96]
Module Probability: 0.000464

[2] 54V77W2P115_pin9[4]<-54V77W2P115[96]
Module Probability: 0.000464

[3] 54V77W2SP12_pin1T[1]<-54V77W2SP12[97]
Module Probability: 0.000464

[4] 54V77W2P115_pin7[3]<-54V77W2P115[96]
Module Probability: 0.000464

[5] 54V77W2P115_pin6[2]<-54V77W2P115[96]
Module Probability: 0.000464

[6] 54V77W2P1153_A1[98]
Module Probability: 0.000348

[7] 54V77W2P1156_A1[99]
Module Probability: 0.000348

[8] 54V77W2P1157_A1[100]
Module Probability: 0.000348

[9] 54V77W2P1159_A1[101]
Module Probability: 0.000348

Ambiguity Group # 12

Node in Diagnostic Tree : 21 (No Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W2P115_pin3[1]<-54V77W2P115[96]
Module Probability: 0.000464

[2] 54V77W2P115_pin9[4]<-54V77W2P115[96]
Module Probability: 0.000464

[3] 54V77W2SP12_pin1T[1]<-54V77W2SP12[97]

Module Probability: 0.000464

[4] 54V77W2P115_pin7[3]<-54V77W2P115[96]
Module Probability: 0.000464

[5] 54V77W2P115_pin6[2]<-54V77W2P115[96]
Module Probability: 0.000464

[6] 54V77W2P1153_A1[98]
Module Probability: 0.000348

[7] 54V77W2P1156_A1[99]
Module Probability: 0.000348

[8] 54V77W2P1157_A1[100]
Module Probability: 0.000348

[9] 54V77W2P1159_A1[101]
Module Probability: 0.000348

Ambiguity Group # 13

Node in Diagnostic Tree : 449 (Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 9

List of modules in this group:
---

[1] 54V77W121P114_pin3[1]<-54V77W121P114[88]
Module Probability: 0.000464

[2] 54V77W121P114_pin9[4]<-54V77W121P114[88]
Module Probability: 0.000464

[3] 54V77W121SP6_pin1T[1]<-54V77W121SP6[89]
Module Probability: 0.000464

[4] 54V77W121P114_pin7[3]<-54V77W121P114[88]
Module Probability: 0.000464

[5] 54V77W121P114_pin6[2]<-54V77W121P114[88]
Module Probability: 0.000464

[6] 54V77W121P1143_A1[90]
Module Probability: 0.000348

[7] 54V77W121P1146_A1[91]
Module Probability: 0.000348

[8] 54V77W121P1147_A1[92]
Module Probability: 0.000348

[9] 54V77W121P1149_A1[93]

Module Probability: 0.000348

Ambiguity Group # 14

Node in Diagnostic Tree : 3 (Go Path)
Total Probability of Group: 0.011139
Total Unweighted Probability: 0.003492
Number of Modules in Group: 8

List of modules in this group:
---

[1] 54V77W1P1111T_F2S_2S1__1[121]
Module Probability: 0.001392

[2] 54V77W1P111W_F2S_2S11_11[143]
Module Probability: 0.001392

[3] 54V77W1P111F_F2S_2S10_10[142]
Module Probability: 0.001392

[4] 54V77W1P111T_F2S_2S9__9[141]
Module Probability: 0.001392

[5] 54V77W1P111P_F2S_2S7__7[140]
Module Probability: 0.001392

[6] 54V77W1P111N_F2S_2S5__5[139]
Module Probability: 0.001392

[7] 54V77W1P111R_F2S_2S4__4[138]
Module Probability: 0.001392

[8] 54V77W1P1111T_F2S_2S3__3[137]
Module Probability: 0.001392

Ambiguity Group # 15

Node in Diagnostic Tree : 459 (Go Path)
Total Probability of Group: 0.003713
Total Unweighted Probability: 0.003928
Number of Modules in Group: 7

List of modules in this group:
---

[1] 50V77W102P817A_D2S_2S1__2[165]
Module Probability: 0.000696

[2] 50V77W102P125S_F2S_2S5__1[186]
Module Probability: 0.000696

[3] 50V77W102P125_pinS[1]<-50V77W102P125[185]
Module Probability: 0.000464

[4] 50V77W102SP686_pin1T[1]<-50V77W102SP686[164]
Module Probability: 0.000464

[5] 50V77W102P817_pinB[2]<-50V77W102P817[163]
Module Probability: 0.000464

[6] 50V77W102P817_pinA[1]<-50V77W102P817[163]
Module Probability: 0.000464

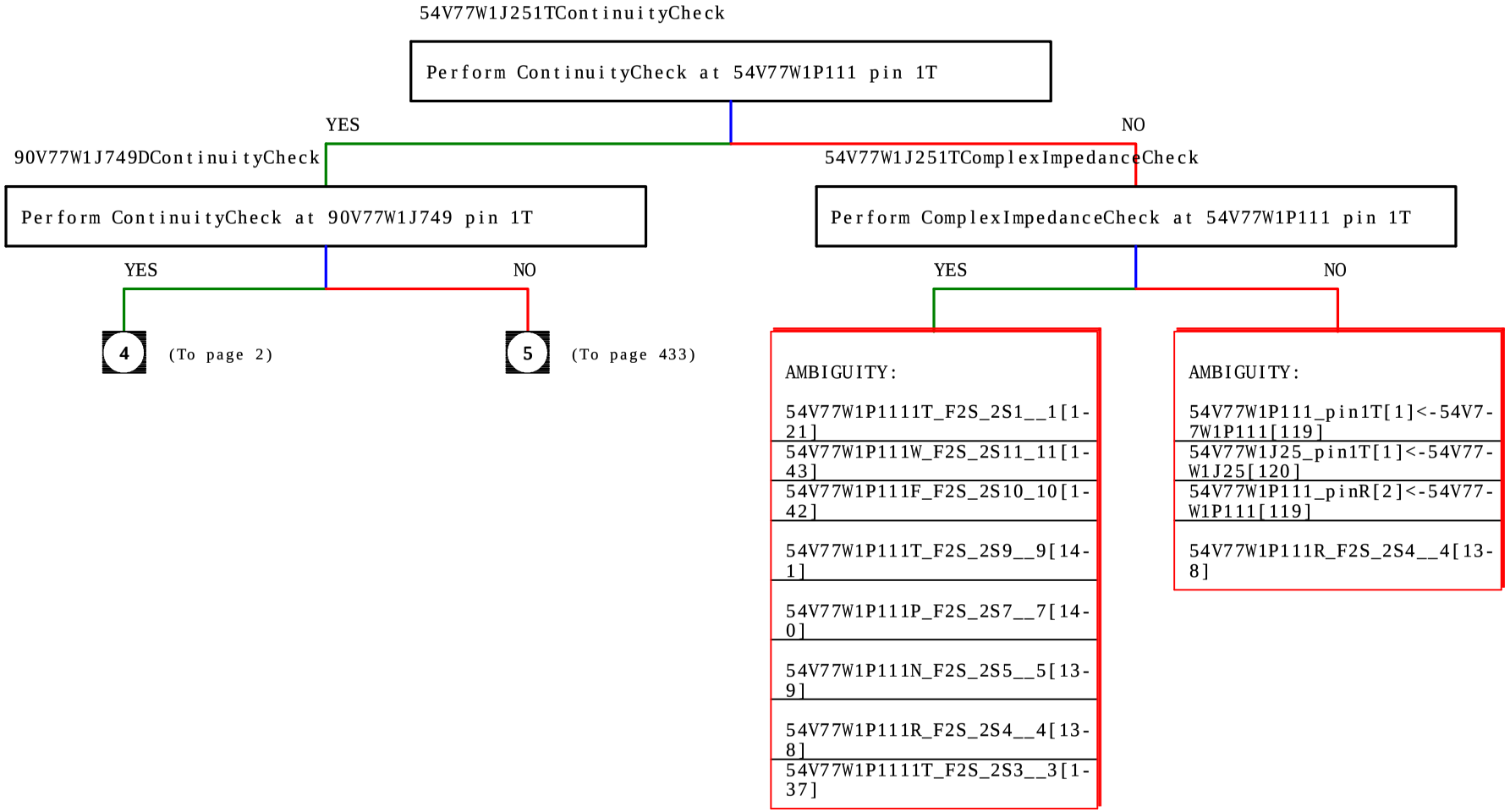
[7] 50V77W102P125_pinT[2]<-50V77W102P125[185]
Module Probability: 0.000464

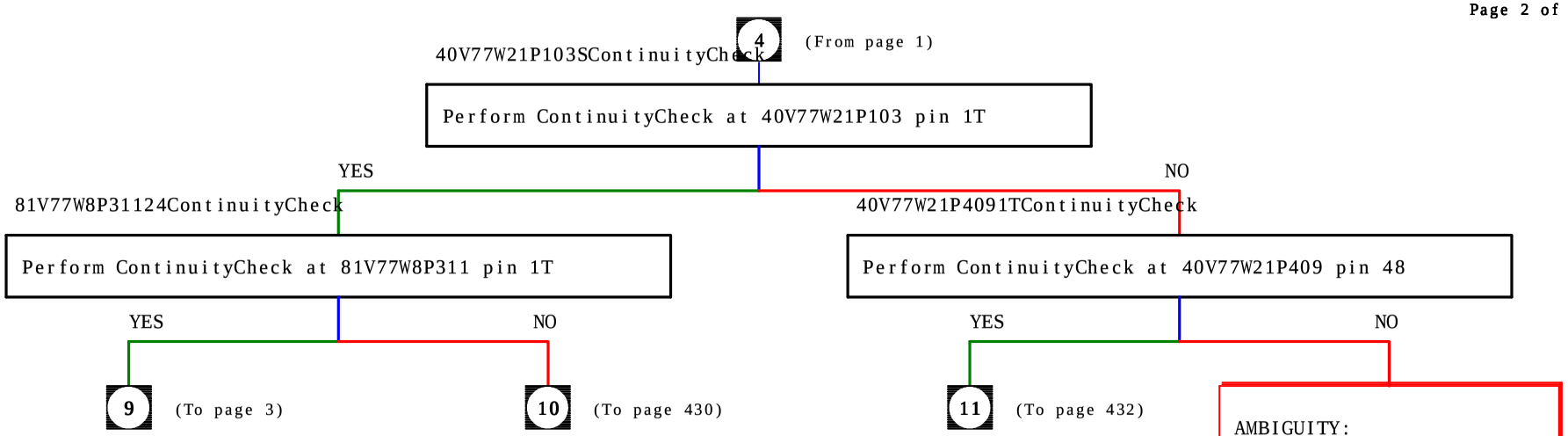
Ambiguity Group Summary Table

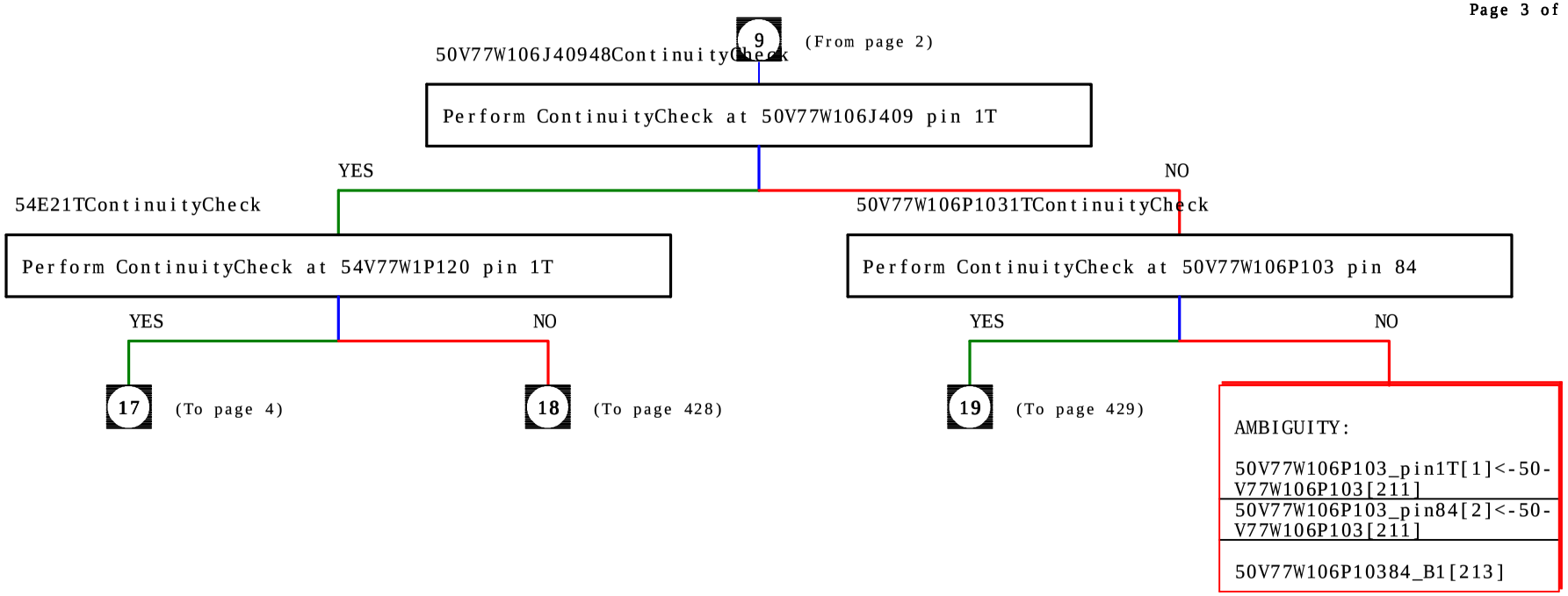
Size	No. of groups	Group Size (%)	Weighted(%)	Unweighted(%)
26	1	0.114811	4.620250	2.095150
9	12	1.377727	4.455700	4.714100
8	1	0.114811	1.113920	0.349192
7	6	0.688863	2.227850	2.357050
5	3	0.344432	0.626582	0.654736
4	7	0.803674	1.079110	1.222170
3	573	65.786452	73.136097	75.032699
2	39	4.477612	3.411390	3.579220
1	229	26.291619	9.329110	9.995640

APPENDIX D

Abbreviated Diagnostic Strategy Report for MEC1 wiring system

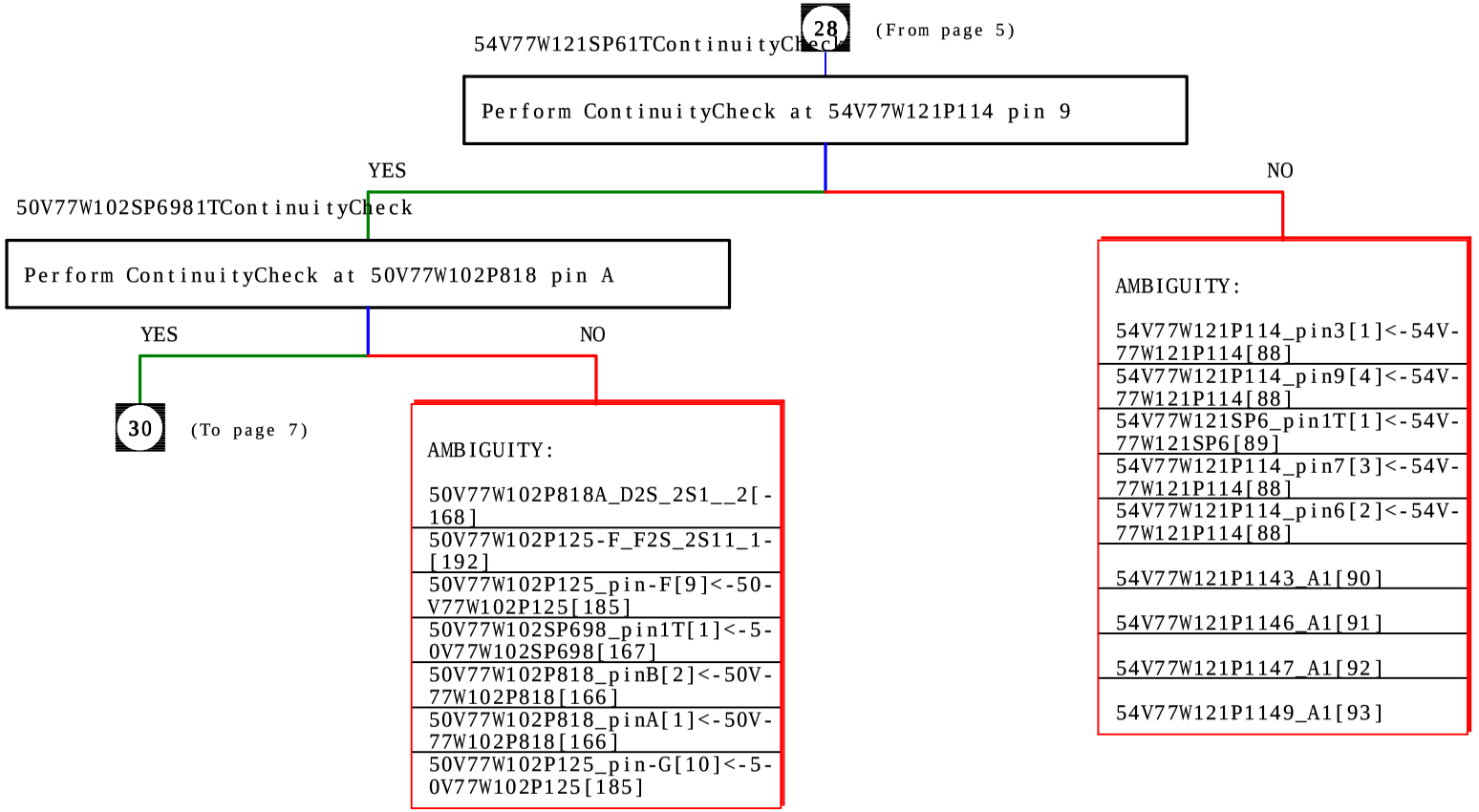

54V77W1J251TContinuityCheck
Perform ContinuityCheck at 54V77W1P111 pin 1T
YES
NO
90V77W1J749DContinuityCheck
54V77W1J251TComplexImpedanceCheck
Perform ContinuityCheck at 90V77W1J749 pin 1T
Perform ComplexImpedanceCheck at 54V77W1P111 pin 1T
YES
NO
YES
NO
4
(To page 2)
5
(To page 433)
AMBIGUITY:
54V77W1P1111T_F2S_2S1__1[1-21]
54V77W1P111W_F2S_2S11_11[1-43]
54V77W1P111F_F2S_2S10_10[1-42]
54V77W1P111T_F2S_2S9__9[14-1]
54V77W1P111P_F2S_2S7__7[14-0]
54V77W1P111N_F2S_2S5__5[13-9]
54V77W1P111R_F2S_2S4__4[13-8]
54V77W1P1111T_F2S_2S3__3[1-37]
AMBIGUITY:
54V77W1P111_pin1T[1]<-54V77W1P111[119]
54V77W1J25_pin1T[1]<-54V77W1J25[120]
54V77W1P111_pinR[2]<-54V77W1P111[119]
54V77W1P111R_F2S_2S4__4[13-8]

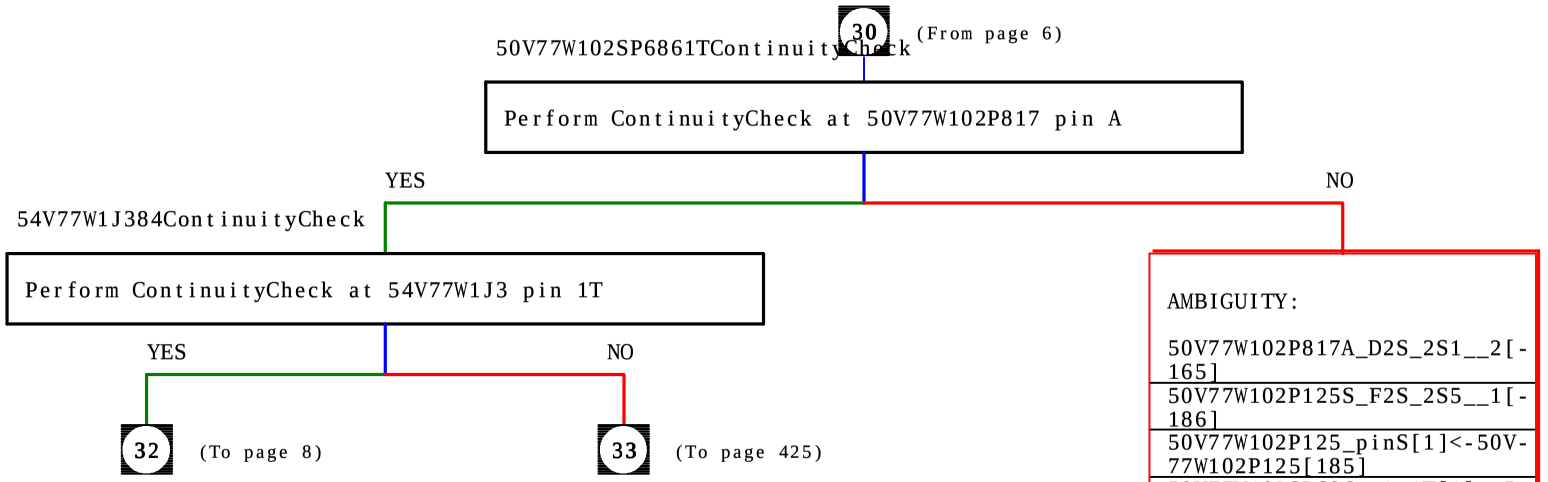

4
(From page 1)
40V77W21P103SContinuityCheck
Perform ContinuityCheck at 40V77W21P103 pin 1T
YES
NO
81V77W8P31124ContinuityCheck
40V77W21P4091TContinuityCheck
Perform ContinuityCheck at 81V77W8P311 pin 1T
Perform ContinuityCheck at 40V77W21P409 pin 48
YES
NO
YES
NO
9
(To page 3)
10
(To page 430)
11
(To page 432)
AMBIGUITY:
40V77W21P409_pin1T[2]<-40V-77W21P409[1]
40V77W21P409_pin48[3]<-40V-77W21P409[1]
40V77W21P40948_B1[8]

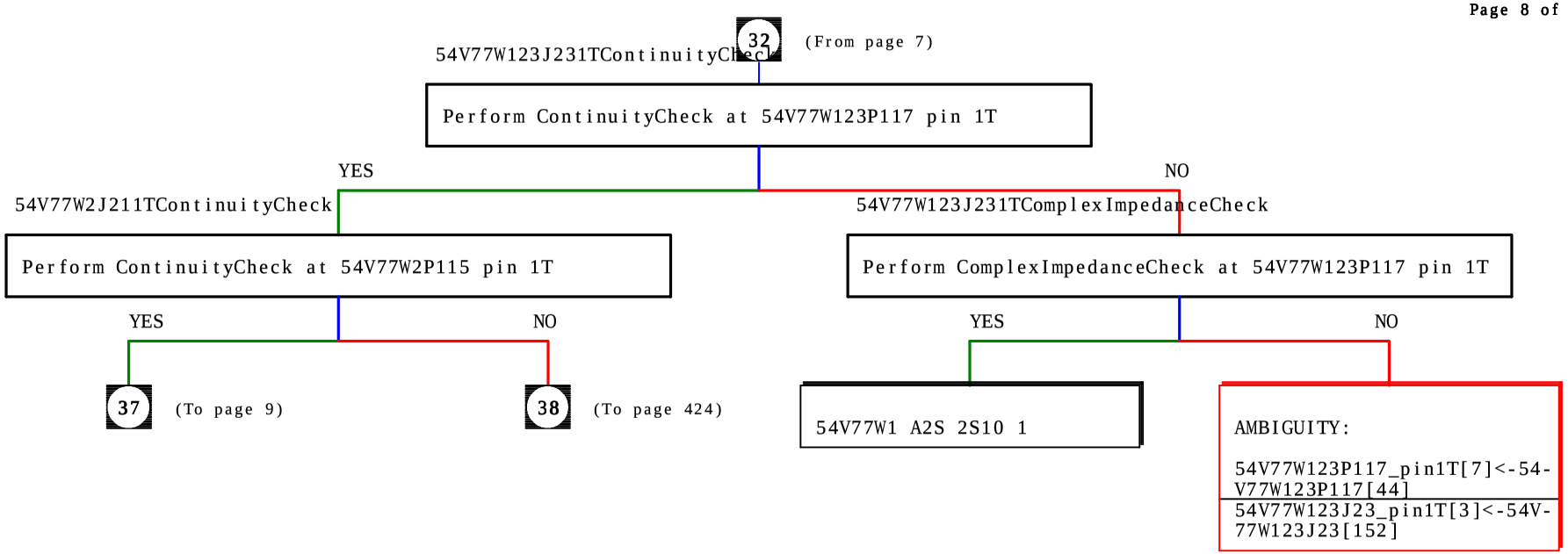

9
(From page 2)
50V77W106J40948ContinuityCheck
Perform ContinuityCheck at 50V77W106J409 pin 1T
YES
NO
54E21TContinuityCheck
50V77W106P1031TContinuityCheck
Perform ContinuityCheck at 54V77W1P120 pin 1T
Perform ContinuityCheck at 50V77W106P103 pin 84
YES
NO
YES
NO
17
(To page 4)
18
(To page 428)
19
(To page 429)
AMBIGUITY:
50V77W106P103_pin1T[1]<-50-V77W106P103[211]
50V77W106P103_pin84[2]<-50-V77W106P103[211]
50V77W106P10384_B1[213]

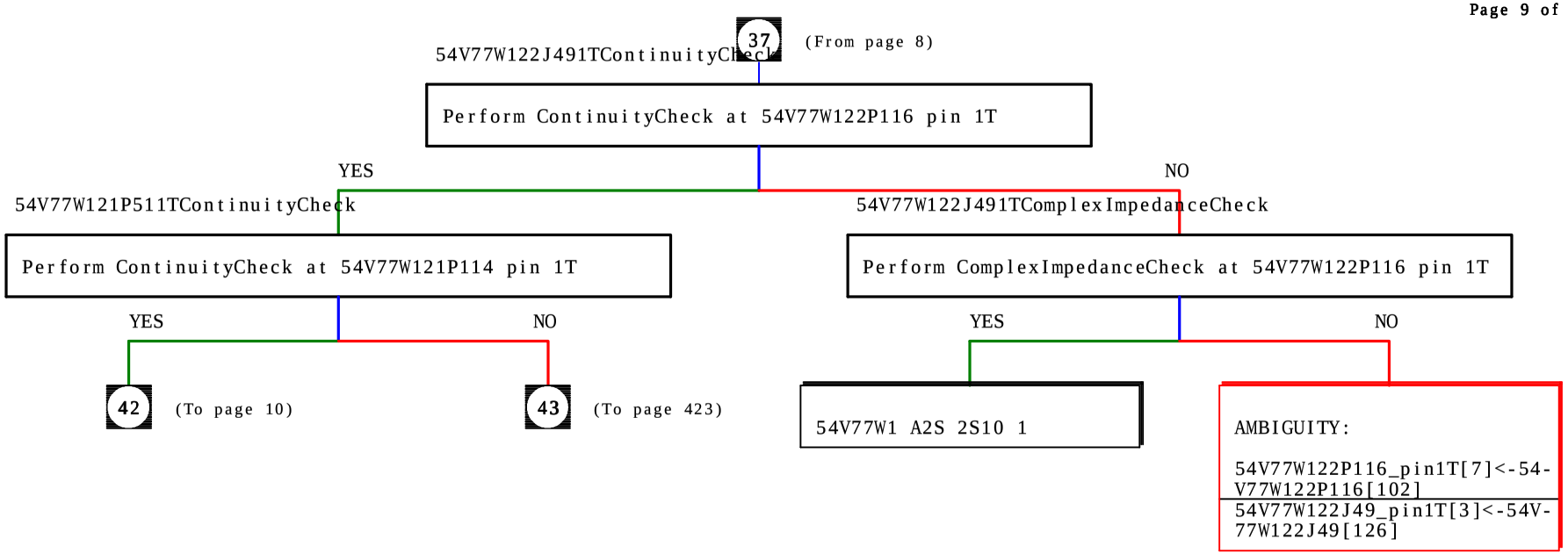

54E31TContinuityCheck
17
(From page 3)
Perform ContinuityCheck at 54V77W1P119 pin 1T
YES
NO
54V77W2SP121TContinuityCheck
54V77W1P1191TContinuityCheck
Perform ContinuityCheck at 54V77W2P115 pin 7
Perform ContinuityCheck at 54V77W1P119 pin 1T
YES
NO
YES
NO
25
(To page 5)
AMBIGUITY:
54V77W2P115_pin3[1]<-54V77-W2P115[96]
54V77W2P115_pin9[4]<-54V77-W2P115[96]
54V77W2SP12_pin1T[1]<-54V7-7W2SP12[97]
54V77W2P115_pin7[3]<-54V77-W2P115[96]
54V77W2P115_pin6[2]<-54V77-W2P115[96]
54V77W2P1153_A1[98]
54V77W2P1156_A1[99]
54V77W2P1157_A1[100]
54V77W2P1159_A1[101]
26
(To page 427)
AMBIGUITY:
54V77W1P119_pin1T[4]<-54V7-7W1P119[51]
54V77W1P1191T_C1[56]


25
(From page 4)
54V77W123SP181TContinuityCheck
Perform ContinuityCheck at 54V77W123P117 pin 9
YES
NO
54V77W122SP141TContinuityCheck
Perform ContinuityCheck at 54V77W122P116 pin 9
YES
NO
28
(To page 6)
AMBIGUITY:
54V77W122P116_pin3[1]<-54V-77W122P116[102]
54V77W122P116_pin9[4]<-54V-77W122P116[102]
54V77W122SP14_pin1T[1]<-54-V77W122SP14[103]
54V77W122P116_pin7[3]<-54V-77W122P116[102]
54V77W122P116_pin6[2]<-54V-77W122P116[102]
54V77W122P1163_A1[104]
54V77W122P1166_A1[105]
54V77W122P1167_A1[106]
54V77W122P1169_A1[109]
AMBIGUITY:
54V77W123P117_pin7[1]<-54V-77W123P117[44]
54V77W123P117_pin3[4]<-54V-77W123P117[44]
54V77W123SP18_pin1T[1]<-54-V77W123SP18[45]
54V77W123P117_pin6[3]<-54V-77W123P117[44]
54V77W123P117_pin9[2]<-54V-77W123P117[44]
54V77W123P1177_A1[46]
54V77W123P1179_A1[47]
54V77W123P1176_A1[76]
54V77W123P1173_A1[110]


28
(From page 5)
54V77W121SP61TContinuityCheck
Perform ContinuityCheck at 54V77W121P114 pin 9
YES
NO
50V77W102SP6981TContinuityCheck
Perform ContinuityCheck at 50V77W102P818 pin A
YES
NO
30
(To page 7)
AMBIGUITY:
50V77W102P818A_D2S_2S1__2[168]
50V77W102P125-F_F2S_2S11_1-[192]
50V77W102P125_pin-F[9]<-50V77W102P125[185]
50V77W102SP698_pin1T[1]<-50V77W102SP698[167]
50V77W102P818_pinB[2]<-50V77W102P818[166]
50V77W102P818_pinA[1]<-50V77W102P818[166]
50V77W102P125_pin-G[10]<-50V77W102P125[185]
AMBIGUITY:
54V77W121P114_pin3[1]<-54V77W121P114[88]
54V77W121P114_pin9[4]<-54V77W121P114[88]
54V77W121SP6_pin1T[1]<-54V77W121SP6[89]
54V77W121P114_pin7[3]<-54V77W121P114[88]
54V77W121P114_pin6[2]<-54V77W121P114[88]
54V77W121P1143_A1[90]
54V77W121P1146_A1[91]
54V77W121P1147_A1[92]
54V77W121P1149_A1[93]


30
(From page 6)
50V77W102SP6861TContinuityCheck
Perform ContinuityCheck at 50V77W102P817 pin A
YES
NO
54V77W1J384ContinuityCheck
Perform ContinuityCheck at 54V77W1J3 pin 1T
YES
NO
32
(To page 8)
33
(To page 425)
AMBIGUITY:
50V77W102P817A_D2S_2S1__2[-165]
50V77W102P125S_F2S_2S5__1[-186]
50V77W102P125_pinS[1]<-50V-77W102P125[185]
50V77W102SP686_pin1T[1]<-5-0V77W102SP686[164]
50V77W102P817_pinB[2]<-50V-77W102P817[163]
50V77W102P817_pinA[1]<-50V-77W102P817[163]
50V77W102P125_pinT[2]<-50V-77W102P125[185]

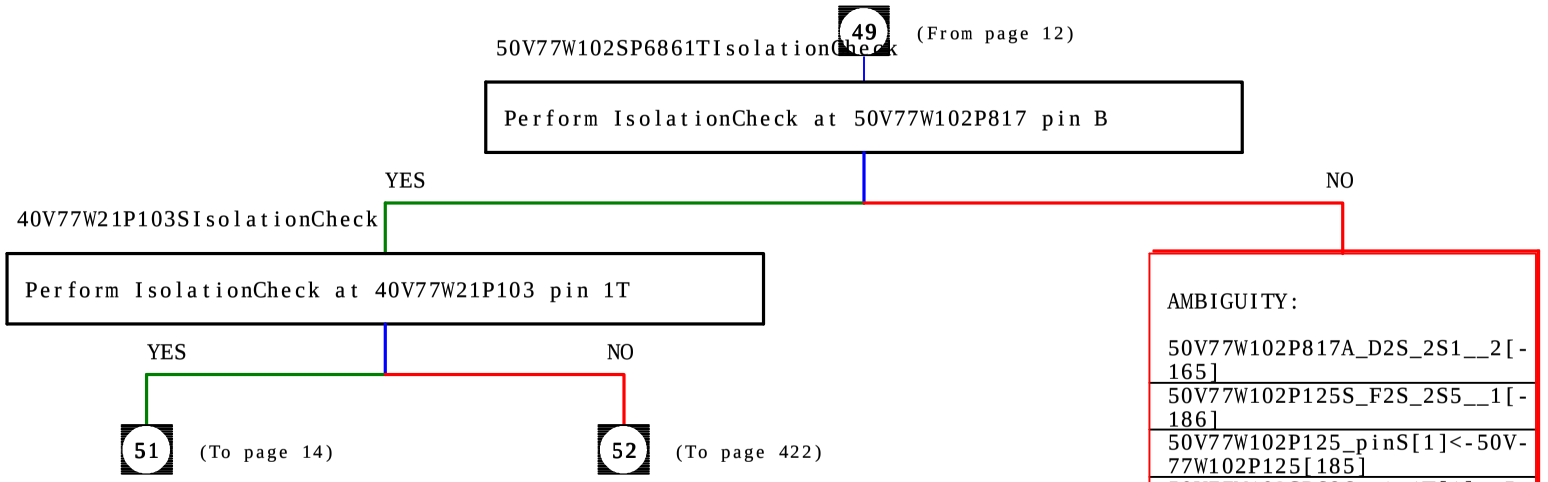

32
54V77W123J231TContinuityCheck
(From page 7)
Perform ContinuityCheck at 54V77W123P117 pin 1T
YES
NO
54V77W2J211TContinuityCheck
54V77W123J231TComplexImpedanceCheck
Perform ContinuityCheck at 54V77W2P115 pin 1T
Perform ComplexImpedanceCheck at 54V77W123P117 pin 1T
YES
NO
YES
NO
37
(To page 9)
38
(To page 424)
54V77W1 A2S 2S10 1
AMBIGUITY:
54V77W123P117_pin1T[7]<-54-V77W123P117[44]
54V77W123J23_pin1T[3]<-54V-77W123J23[152]

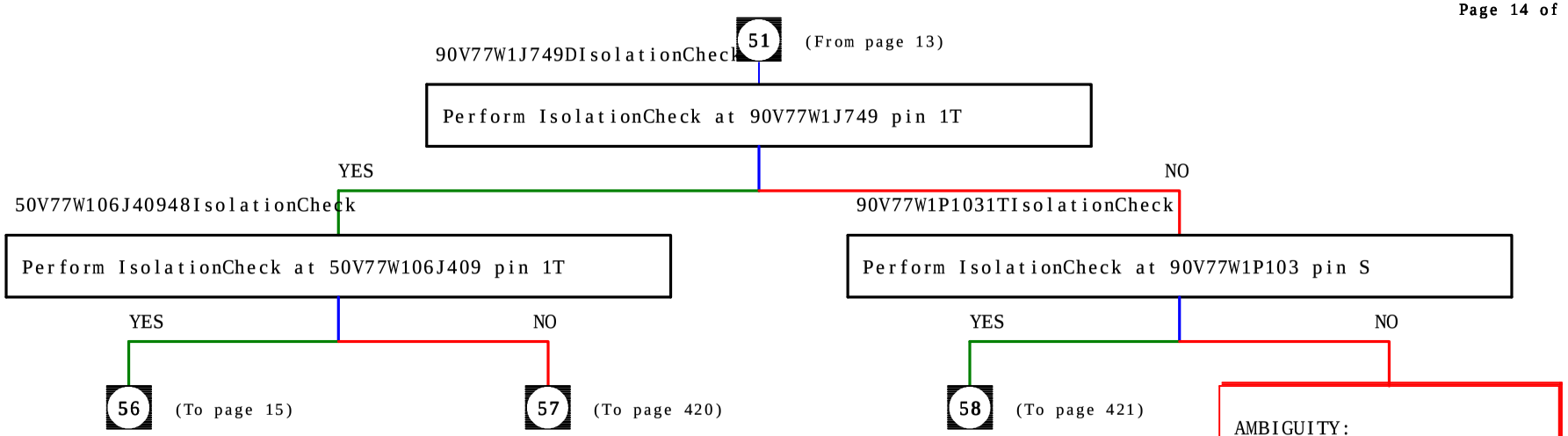

37
(From page 8)
54V77W122J491TContinuityCheck
Perform ContinuityCheck at 54V77W122P116 pin 1T
YES
NO
54V77W121P511TContinuityCheck
54V77W122J491TComplexImpedanceCheck
Perform ContinuityCheck at 54V77W121P114 pin 1T
Perform ComplexImpedanceCheck at 54V77W122P116 pin 1T
YES
NO
YES
NO
42
(To page 10)
43
(To page 423)
54V77W1 A2S 2S10 1
AMBIGUITY:
54V77W122P116_pin1T[7]<-54-V77W122P116[102]
54V77W122J49_pin1T[3]<-54V-77W122J49[126]

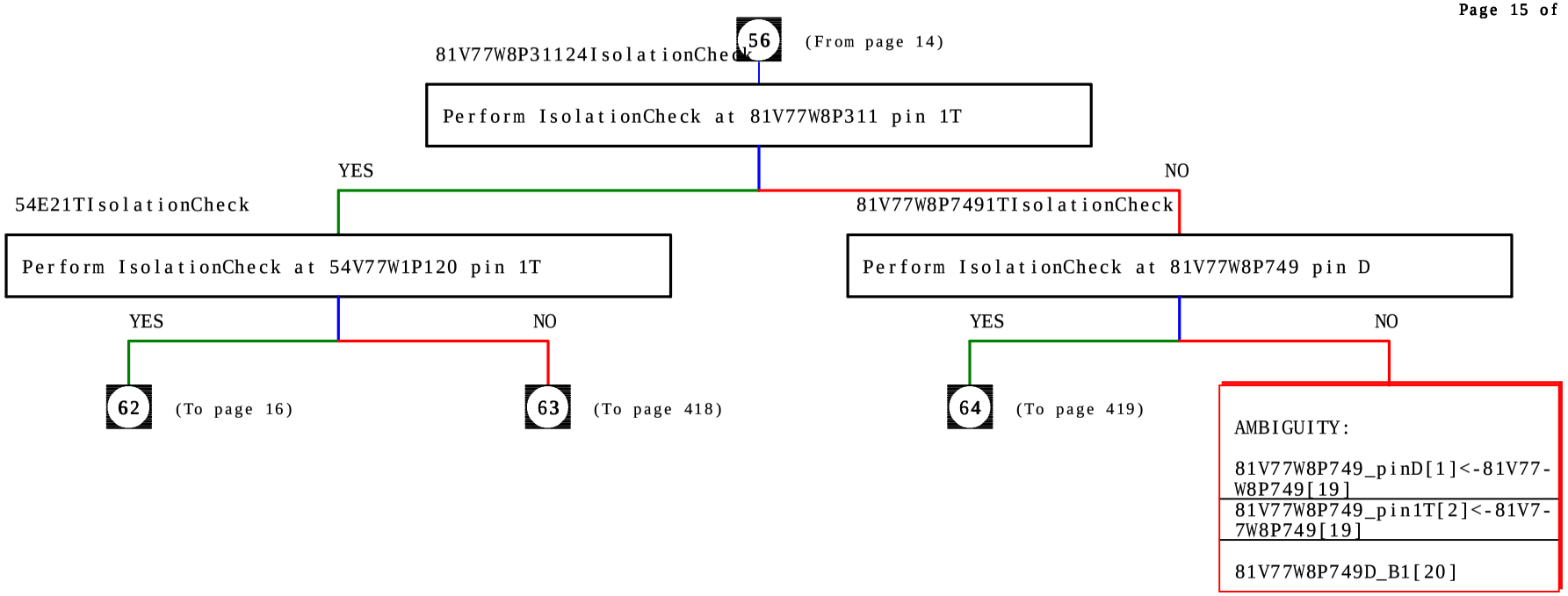

42
(From page 9)
50V77W34SP211TContinuityCheck
Perform ContinuityCheck at 50V77W34P133 pin P
YES
NO
54V77W121SP61TIsolationCheck
PRE-SETUPS:
Connect all other pins to ground.
TEST:
Perform IsolationCheck at 54V77W121P114 pin 7
YES
NO
45
(To page 11)
AMBIGUITY:
54V77W121P114_pin3[1]<-54V-77W121P114[88]
54V77W121P114_pin9[4]<-54V-77W121P114[88]
54V77W121SP6_pin1T[1]<-54V-77W121SP6[89]
54V77W121P114_pin7[3]<-54V-77W121P114[88]
54V77W121P114_pin6[2]<-54V-77W121P114[88]
54V77W121P1143_A1[90]
54V77W121P1146_A1[91]
54V77W121P1147_A1[92]
54V77W121P1149_A1[93]
AMBIGUITY:
50V77W34P133_pinP[3]<-50V7-7W34P133[193]
50V77W34J540_pinBB[1]<-50V-77W34J540[230]
50V77W34SP21_pin1T[1]<-50V-77W34SP21[198]
50V77W34P133P_C1[199]
50V77W34J540BB_C3T_3T1__1A-[231]

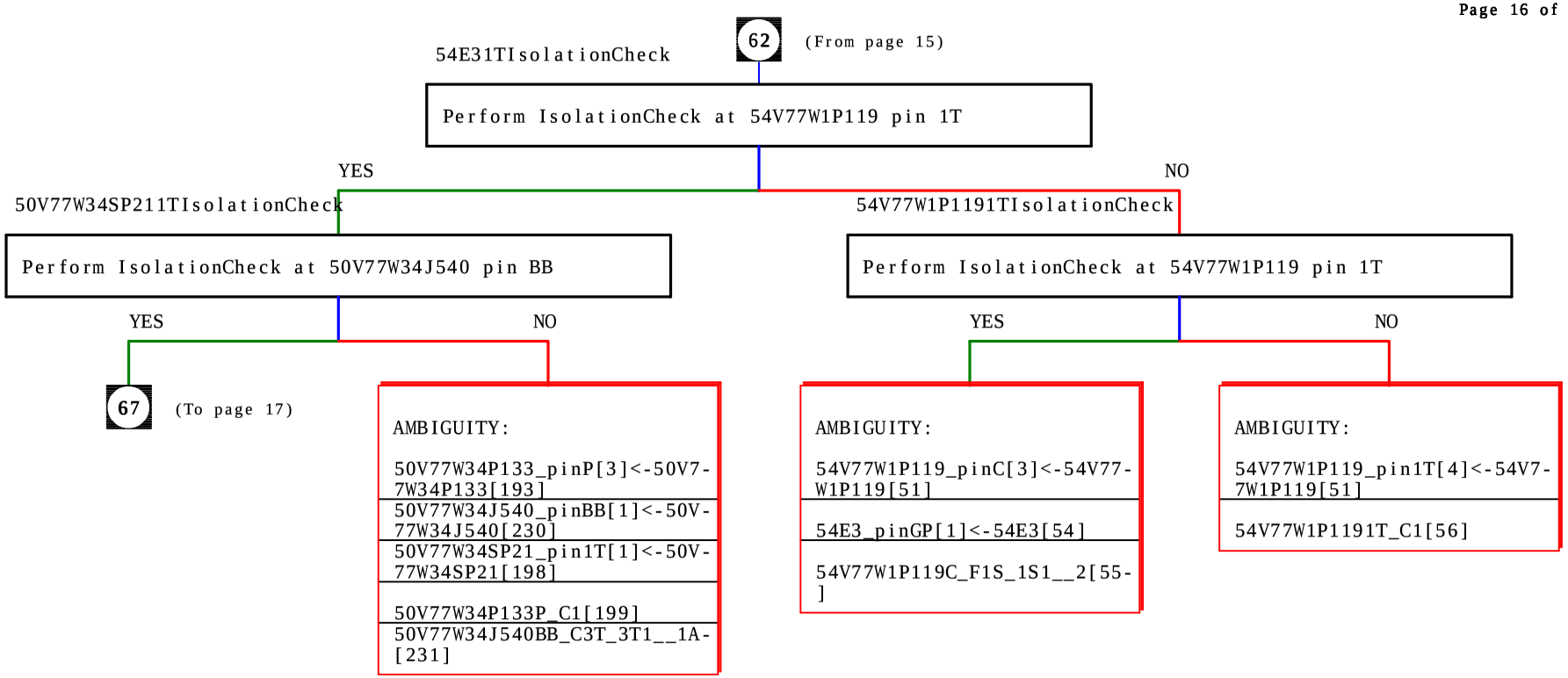

45
(From page 10)
54V77W123SP181TIsolationCheck
Perform IsolationCheck at 54V77W123P117 pin 3
YES
NO
54V77W122SP141TIsolationCheck
Perform IsolationCheck at 54V77W122P116 pin 9
YES
NO
47
(To page 12)
AMBIGUITY:
54V77W122P116_pin3[1]<-54V-77W122P116[102]
54V77W122P116_pin9[4]<-54V-77W122P116[102]
54V77W122SP14_pin1T[1]<-54-V77W122SP14[103]
54V77W122P116_pin7[3]<-54V-77W122P116[102]
54V77W122P116_pin6[2]<-54V-77W122P116[102]
54V77W122P1163_A1[104]
54V77W122P1166_A1[105]
54V77W122P1167_A1[106]
54V77W122P1169_A1[109]
AMBIGUITY:
54V77W123P117_pin7[1]<-54V-77W123P117[44]
54V77W123P117_pin3[4]<-54V-77W123P117[44]
54V77W123SP18_pin1T[1]<-54-V77W123SP18[45]
54V77W123P117_pin6[3]<-54V-77W123P117[44]
54V77W123P117_pin9[2]<-54V-77W123P117[44]
54V77W123P1177_A1[46]
54V77W123P1179_A1[47]
54V77W123P1176_A1[76]
54V77W123P1173_A1[110]

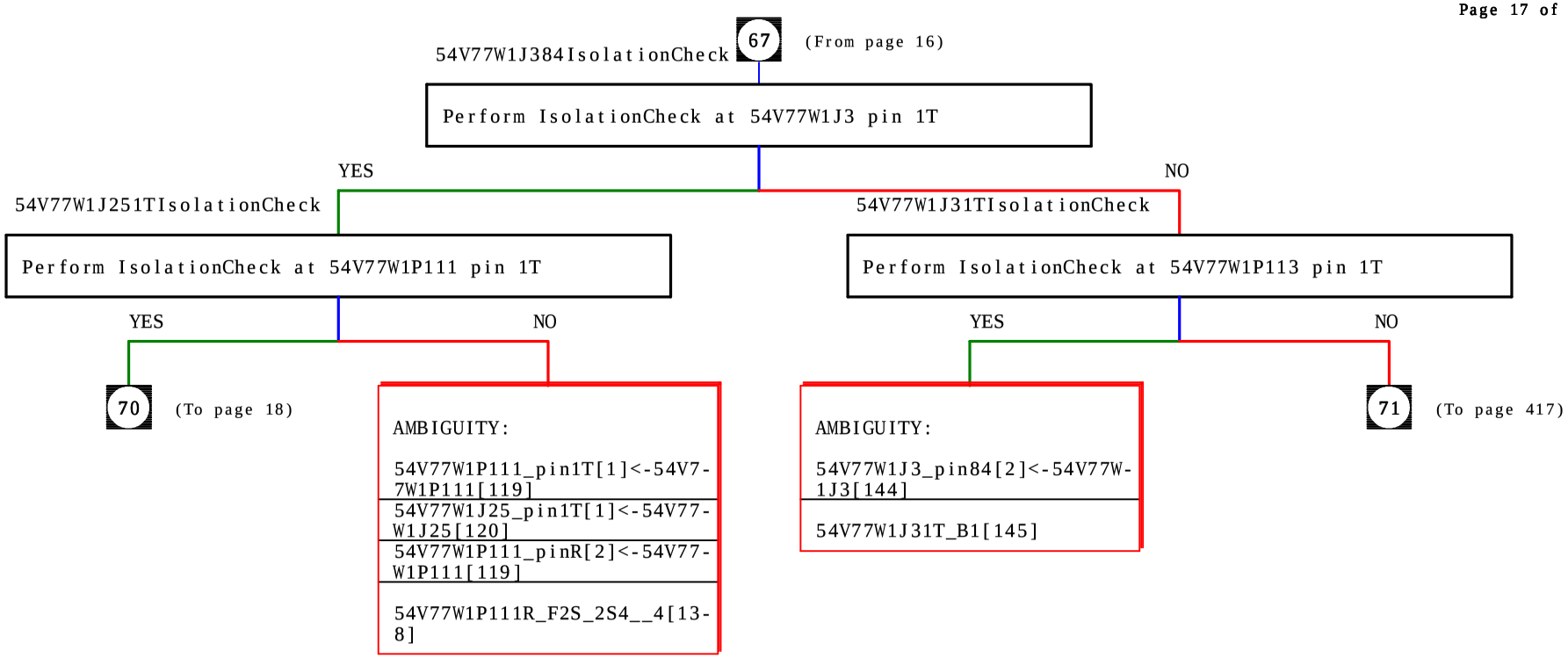

54V77W2SP121TIsolationCheck
47
(From page 11)
Perform IsolationCheck at 54V77W2P115 pin 9
YES
NO
50V77W102SP6981TIsolationCheck
Perform IsolationCheck at 50V77W102P818 pin B
YES
NO
49
(To page 13)
AMBIGUITY:
50V77W102P818A_D2S_2S1__2[168]
50V77W102P125-F_F2S_2S11_1-[192]
50V77W102P125_pin-F[9]<-50V77W102P125[185]
50V77W102SP698_pin1T[1]<-50V77W102SP698[167]
50V77W102P818_pinB[2]<-50V77W102P818[166]
50V77W102P818_pinA[1]<-50V77W102P818[166]
50V77W102P125_pin-G[10]<-50V77W102P125[185]
AMBIGUITY:
54V77W2P115_pin3[1]<-54V77W2P115[96]
54V77W2P115_pin9[4]<-54V77W2P115[96]
54V77W2SP12_pin1T[1]<-54V77W2SP12[97]
54V77W2P115_pin7[3]<-54V77W2P115[96]
54V77W2P115_pin6[2]<-54V77W2P115[96]
54V77W2P1153_A1[98]
54V77W2P1156_A1[99]
54V77W2P1157_A1[100]
54V77W2P1159_A1[101]

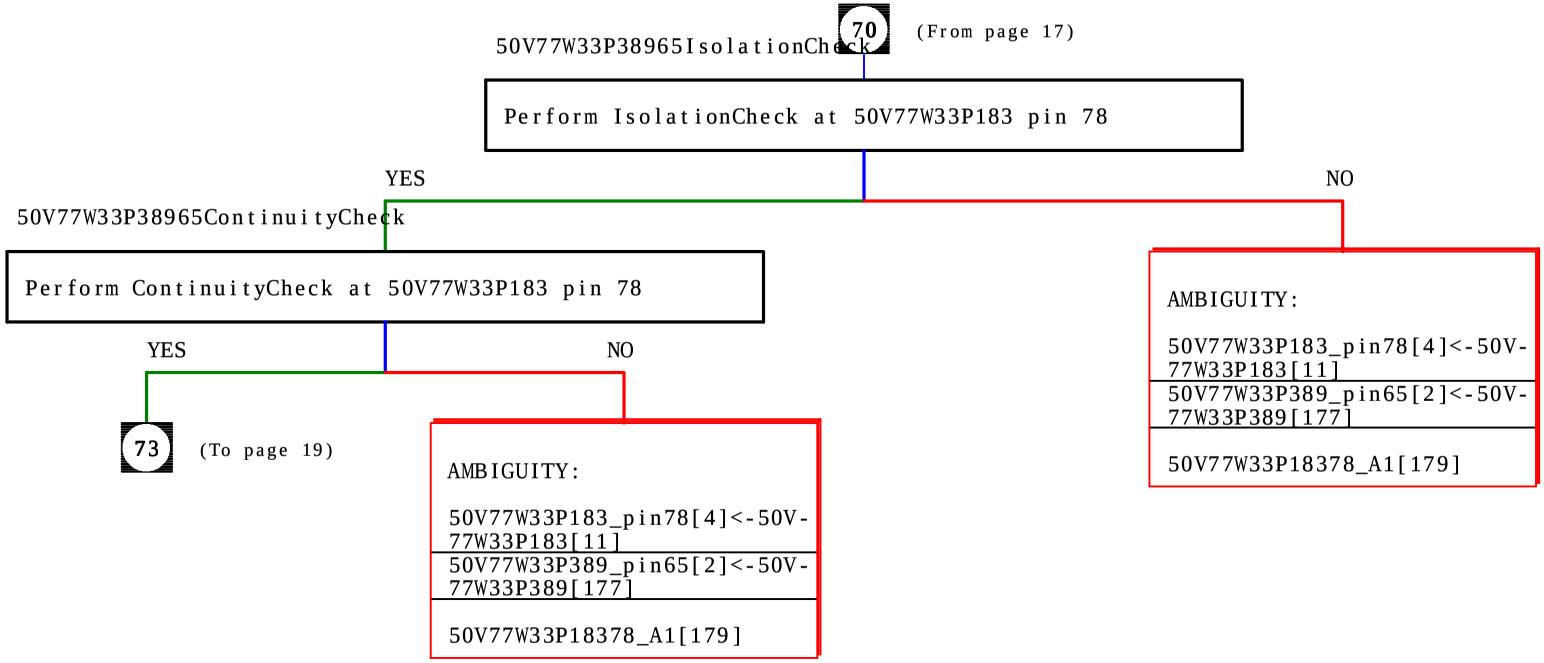

49
(From page 12)
50V77W102SP6861TIsolationCheck
Perform IsolationCheck at 50V77W102P817 pin B
YES
NO
40V77W21P103SIsolationCheck
Perform IsolationCheck at 40V77W21P103 pin 1T
YES
NO
51
(To page 14)
52
(To page 422)
AMBIGUITY:
50V77W102P817A_D2S_2S1__2[-165]
50V77W102P125S_F2S_2S5__1[-186]
50V77W102P125_pinS[1]<-50V-77W102P125[185]
50V77W102SP686_pin1T[1]<-5-0V77W102SP686[164]
50V77W102P817_pinB[2]<-50V-77W102P817[163]
50V77W102P817_pinA[1]<-50V-77W102P817[163]
50V77W102P125_pinT[2]<-50V-77W102P125[185]

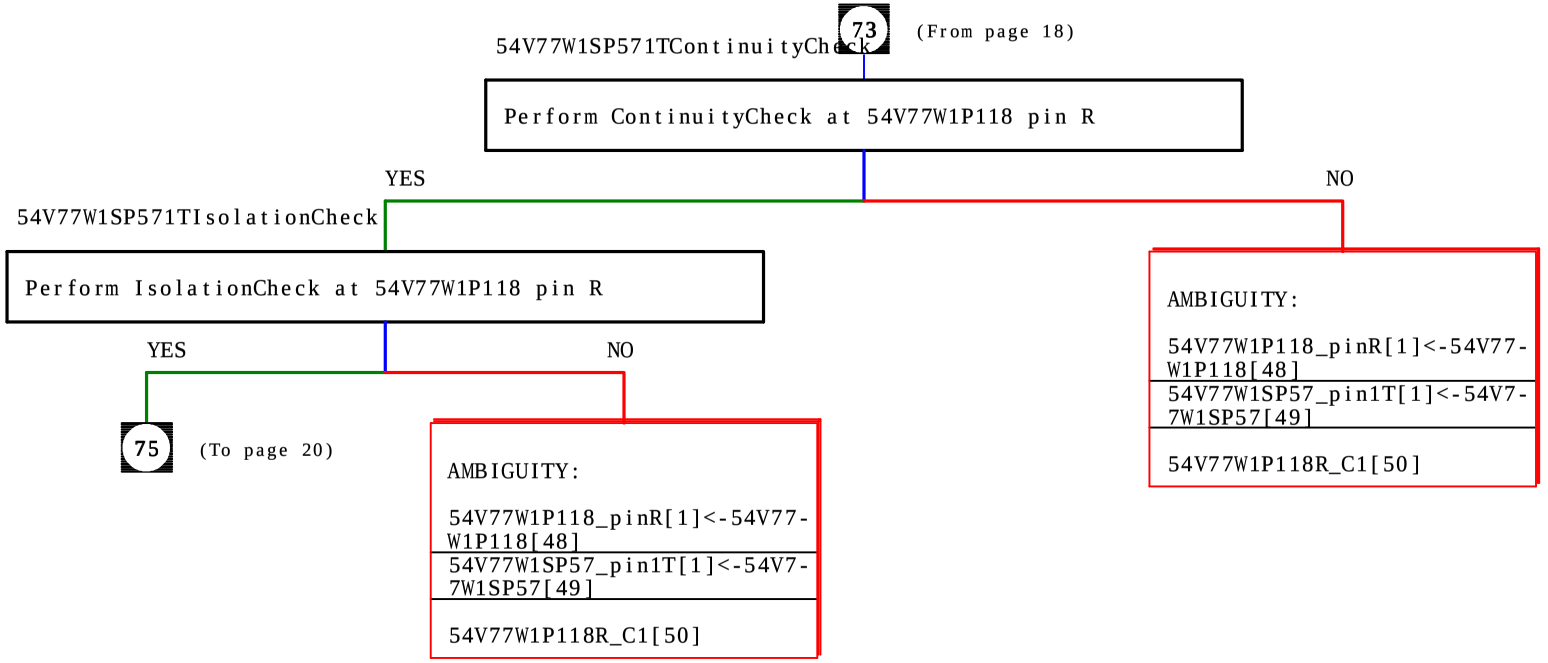

90V77W1J749DIsolationCheck
51
(From page 13)
Perform IsolationCheck at 90V77W1J749 pin 1T
YES
NO
50V77W106J40948IsolationCheck
90V77W1P1031TIsolationCheck
Perform IsolationCheck at 50V77W106J409 pin 1T
Perform IsolationCheck at 90V77W1P103 pin S
YES
NO
YES
NO
56
(To page 15)
57
(To page 420)
58
(To page 421)
AMBIGUITY:
90V77W1P103_pin1T[3]<-90V77W1P103[21]
90V77W1P103_pinS[4]<-90V77W1P103[21]
90V77W1P103S_B1[25]

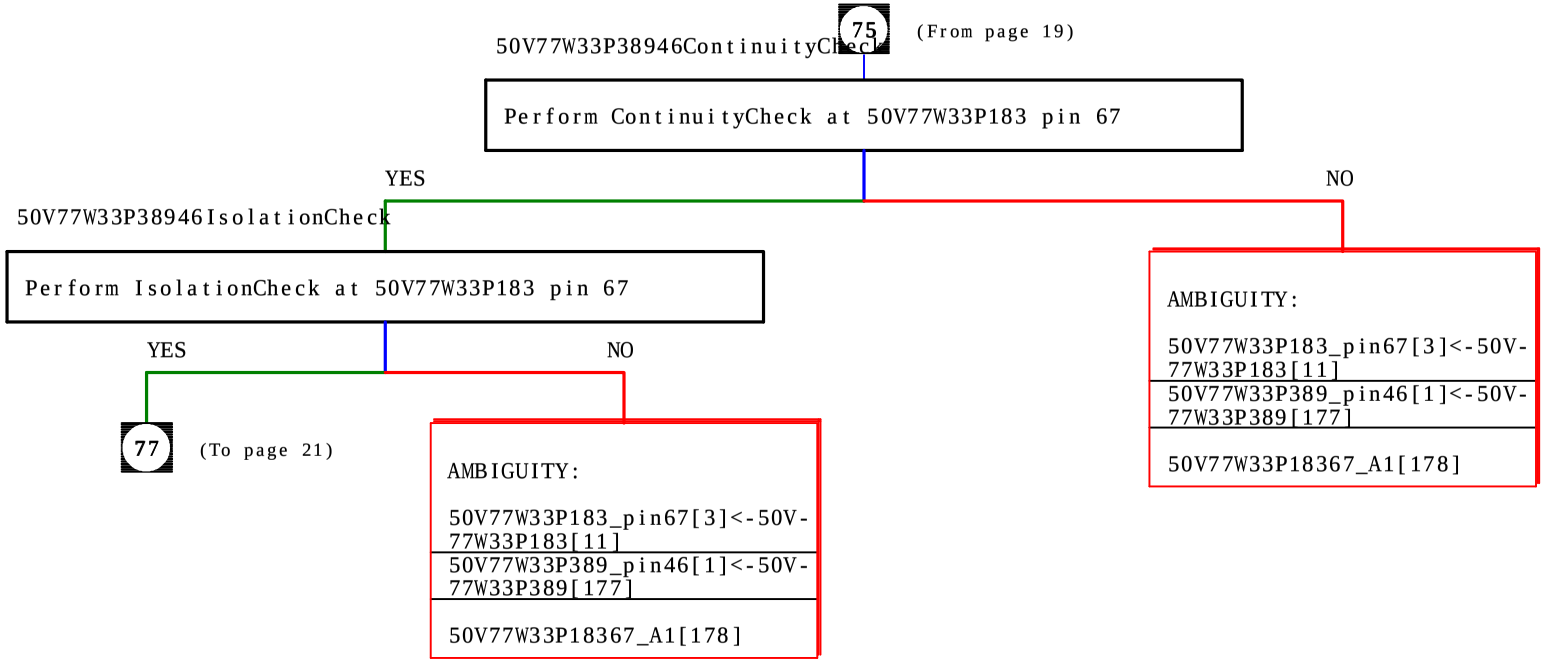

81V77W8P31124IsolationCheck
56
(From page 14)
Perform IsolationCheck at 81V77W8P311 pin 1T
YES
NO
54E21TIsolationCheck
81V77W8P7491TIsolationCheck
Perform IsolationCheck at 54V77W1P120 pin 1T
Perform IsolationCheck at 81V77W8P749 pin D
YES
NO
YES
NO
62
(To page 16)
63
(To page 418)
64
(To page 419)
AMBIGUITY:
81V77W8P749_pinD[1]<-81V77-W8P749[19]
81V77W8P749_pin1T[2]<-81V7-7W8P749[19]
81V77W8P749D_B1[20]


54E31TIsolationCheck
62
(From page 15)
Perform IsolationCheck at 54V77W1P119 pin 1T
YES
NO
50V77W34SP211TIsolationCheck
54V77W1P1191TIsolationCheck
Perform IsolationCheck at 50V77W34J540 pin BB
Perform IsolationCheck at 54V77W1P119 pin 1T
YES
NO
YES
NO
67
(To page 17)
AMBIGUITY:
50V77W34P133_pinP[3]<-50V77W34P133[193]
50V77W34J540_pinBB[1]<-50V77W34J540[230]
50V77W34SP21_pin1T[1]<-50V77W34SP21[198]
50V77W34P133P_C1[199]
50V77W34J540BB_C3T_3T1__1A[231]
AMBIGUITY:
54V77W1P119_pinC[3]<-54V77W1P119[51]
54E3_pinGP[1]<-54E3[54]
54V77W1P119C_F1S_1S1__2[55]
AMBIGUITY:
54V77W1P119_pin1T[4]<-54V77W1P119[51]
54V77W1P1191T_C1[56]


54V77W1J384IsolationCheck
67
(From page 16)
Perform IsolationCheck at 54V77W1J3 pin 1T
YES
NO
54V77W1J251TIsolationCheck
54V77W1J31TIsolationCheck
Perform IsolationCheck at 54V77W1P111 pin 1T
Perform IsolationCheck at 54V77W1P113 pin 1T
YES
NO
YES
NO
70
(To page 18)
AMBIGUITY:
54V77W1P111_pin1T[1]<-54V77W1P111[119]
54V77W1J25_pin1T[1]<-54V77W1J25[120]
54V77W1P111_pinR[2]<-54V77W1P111[119]
54V77W1P111R_F2S_2S4__4[138]
AMBIGUITY:
54V77W1J3_pin84[2]<-54V77W1J3[144]
54V77W1J31T_B1[145]
71
(To page 417)


70
(From page 17)
50V77W33P38965IsolationCheck
Perform IsolationCheck at 50V77W33P183 pin 78
YES
NO
50V77W33P38965ContinuityCheck
Perform ContinuityCheck at 50V77W33P183 pin 78
YES
NO
AMBIGUITY:
50V77W33P183_pin78[4]<-50V-77W33P183[11]
50V77W33P389_pin65[2]<-50V-77W33P389[177]
50V77W33P18378_A1[179]
73
(To page 19)
AMBIGUITY:
50V77W33P183_pin78[4]<-50V-77W33P183[11]
50V77W33P389_pin65[2]<-50V-77W33P389[177]
50V77W33P18378_A1[179]


73
(From page 18)
54V77W1SP571TContinuityCheck
Perform ContinuityCheck at 54V77W1P118 pin R
YES
NO
54V77W1SP571TIsolationCheck
Perform IsolationCheck at 54V77W1P118 pin R
YES
NO
75
(To page 20)
AMBIGUITY:
54V77W1P118_pinR[1]<-54V77-W1P118[48]
54V77W1SP57_pin1T[1]<-54V7-7W1SP57[49]
54V77W1P118R_C1[50]
AMBIGUITY:
54V77W1P118_pinR[1]<-54V77-W1P118[48]
54V77W1SP57_pin1T[1]<-54V7-7W1SP57[49]
54V77W1P118R_C1[50]


75
(From page 19)
50V77W33P38946ContinuityCheck
Perform ContinuityCheck at 50V77W33P183 pin 67
YES
NO
50V77W33P38946IsolationCheck
Perform IsolationCheck at 50V77W33P183 pin 67
YES
NO
77
(To page 21)
AMBIGUITY:
50V77W33P183_pin67[3]<-50V-77W33P183[11]
50V77W33P389_pin46[1]<-50V-77W33P389[177]
50V77W33P18367_A1[178]
AMBIGUITY:
50V77W33P183_pin67[3]<-50V-77W33P183[11]
50V77W33P389_pin46[1]<-50V-77W33P389[177]
50V77W33P18367_A1[178]

APPENDIX E

Sample FMECA report for MEC1 wiring system

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1

INDENTURE LEVEL Component

REFERENCE DRAWING

MISSION

DATE 09/07/00

SHEET 1 OF 847

COMPILED BY

APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BrokenShield				40V77W2-1P103SCo-ntinuityCh-eck, 40V77W2-1P1031TC-ontinuityC-heck	40V77W21P1-031TContinuit-yCheck		IV - Minor	Open
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				40V77W2-1P103PC-omplexImp-edanceCh-eck, 40V77W2-1P103PDie-lectricWiths-tandingVol-tageCheck	40V77W21P1-03PDielectric-WithstandingVoltageCheck		IV - Minor	Short to Ground
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance,	HardShort				40V77W2-1P103PIso-lationCheck	40V77W21P1-03PIsolationC-heck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 2 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				40V77W2-1P103PC-omplexImp-edanceCh-eck	40V77W21P1-03PComplexI-mpedanceCh-eck		IV - Minor	Open
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				40V77W2-1P103PCo-ntinuityCh-eck, 40V77W2-1P103PC-omplexImp-edanceCh-eck	40V77W21P1-03PComplexI-mpedanceCh-eck		IV - Minor	Open
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance,	Open				40V77W2-1P103RCo-	40V77W21P1-03RComplexI-		IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 3 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance					ntinuityCheck, 40V77W21P103RComplexImpedanceCheck	mpedanceCheck			
M.mec1.3.0	40V77W21P40947_A2S__2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				40V77W21P103RComplexImpedanceCheck	40V77W21P103RComplexImpedanceCheck		IV - Minor	Open
M.mec1.3.0	40V77W21P40947_A2S__2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk,	HardShort				40V77W21P103RIsolationCheck	40V77W21P103RIsolationCheck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 4 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.3.0	40V77W21P40947_A2S-_2S1__10	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				40V77W2-1P103RC-omplexImp-edanceCh-eck, 40V77W2-1P103RDie-lectricWiths-tandingVol-tageCheck	40V77W21P1-03RDielectric-Withstanding-VoltageCheck		IV - Minor	Short to Ground
M.mec1.4.0	40V77W21P1031T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				40V77W2-1P103SC-omplexImp-edanceCh-eck, 40V77W2-1P103SDie-lectricWiths-tandingVol-tageCheck	40V77W21P1-03SDielectric-Withstanding-VoltageCheck		IV - Minor	Short to Ground
M.mec1.4.0	40V77W21P1031T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk,	HardShort				40V77W2-1P103SIso-lationCheck	40V77W21P1-03SIsolationC-heck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 5 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.4.0	40V77W21P1031T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				40V77W21P1031SComplexImpedanceCheck	40V77W21P103SComplexImpedanceCheck		IV - Minor	Open
M.mec1.4.0	40V77W21P1031T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance,	Open				40V77W21P1031SContinuityCheck, 40V77W21P1031SComplexImpedanceCheck	40V77W21P103SComplexImpedanceCheck		IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 6 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		HiPotential, DWV, Resistance									
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric							IV - Minor	Short to Ground
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort							IV - Minor	Short to Ground
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-	DeltaResistance							IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 7 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open							IV - Minor	Open
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				40V77W8-5P13161C-ontinuityC-heck, 40V77W8-5P13161C-omplexImp-edanceCh-eck	40V77W85P1-3161Complex-ImpedanceCh-eck		IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 8 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				40V77W85P13161ComplexImpedanceCheck	40V77W85P13161ComplexImpedanceCheck		IV - Minor	Open
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort				40V77W85P13161IsolationCheck	40V77W85P13161IsolationCheck		IV - Minor	Short to Ground
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance,	BadDielectric				40V77W85P13161ComplexImpedanceCheck, 40V77W85P13161DielectricWithstanding-	40V77W85P13161DielectricWithstandingVoltageCheck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

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MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance					VoltageCh-eck				
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				40V77W8-5P13159C-omplexImp-edanceCh-eck, 40V77W8-5P13159D-ielectricWit-hstanding-VoltageCh-eck	40V77W85P1-3159Dielectri-cWithstanding-VoltageCheck		IV - Minor	Short to Ground
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort				40V77W8-5P13159Is-olationChe-ck	40V77W85P1-3159Isolation-Check		IV - Minor	Short to Ground
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance,	DeltaResistance				40V77W8-5P13159C-	40V77W85P1-3159Complex-		IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

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IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance					omplexImpedanceCheck	ImpedanceCheck			
M.mec1.7.0	40V77W85P419125_C3-T_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				40V77W85P13159COntinuityCheck, 40V77W85P13159COmplexImpedanceCheck	40V77W85P13159ComplexImpedanceCheck		IV - Minor	Open
M.mec1.8.0	40V77W21P40948_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk,	BadDielectric				40V77W21P103SComplexImpedanceCheck, 40V77W21P103SDielectricWithstandingVoltageCheck, 40V77W2-	40V77W21P4091TDielectricWithstandingVoltageCheck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

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IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance					1P1031TC-omplexImp-edanceCh-eck, 40V77W2-1P1031TD-ielectricWit-hstanding-VoltageCh-eck, 40V77W2-1P4091TC-omplexImp-edanceCh-eck, 40V77W2-1P4091TD-ielectricWit-hstanding-VoltageCh-eck				
M.mec1.8.0	40V77W21P40948_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort				40V77W2-1P103SIso-lationChec-k, 40V77W2-1P1031TIs-olationChe-ck, 40V77W2-1P4091TIs-olationChe-ck	40V77W21P4-091TIsolation-Check		IV - Minor	Short to Ground
M.mec1.8.0	40V77W21P40948_B1	Continuity, SeriesResistance, Isolation, Noise,	DeltaResistance				40V77W2-1P103SC-omplexImp-	40V77W21P4-091TComplex-ImpedanceCh-		IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

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MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance					edanceCheck, 40V77W2-1P1031TComplexImpedanceCheck, 40V77W2-1P4091TComplexImpedanceCheck	eck			
M.mec1.8.0	40V77W21P40948_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				40V77W2-1P103SContinuityCheck, 40V77W2-1P103SComplexImpedanceCheck, 40V77W2-1P1031TContinuityCheck, 40V77W2-1P1031TComplexImpedanceCheck, 40V77W2-1P4091TContinuityCheck, 40V77W2-1P4091TComplexImpedanceCheck	40V77W21P4-091TComplex-ImpedanceCheck		IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1

INDENTURE LEVEL Component

REFERENCE DRAWING

MISSION

DATE 09/07/00

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COMPILED BY

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IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
M.mec1.10.0	50V77W106J4091T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				50V77W106J40948ComplexImpedanceCheck, 50V77W106J40948DielectricWithstandingVoltageCheck	50V77W106J40948DielectricWithstandingVoltageCheck		IV - Minor	Short to Ground
M.mec1.10.0	50V77W106J4091T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort				50V77W106J40948IsolationCheck	50V77W106J40948IsolationCheck		IV - Minor	Short to Ground
M.mec1.10.0	50V77W106J4091T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance,	DeltaResistance				50V77W106J40948ComplexImpedanceCheck	50V77W106J40948ComplexImpedanceCheck		IV - Minor	Open

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SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 14 OF 847

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IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.10.0	50V77W106J4091T_B1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				50V77W1-06J40948-Continuity-Check, 50V77W1-06J40948-ComplexImpedance-Check	50V77W106J-40948ComplexImpedanceCheck		IV - Minor	Open
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric							IV - Minor	Short to Ground
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance,	HardShort							IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 15 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance							IV - Minor	Open
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk,	Open							IV - Minor	Open

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

INDENTURE LEVEL Component SHEET 16 OF 847

REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				50V77W33-J419127C-ontinuityC-heck, 50V77W33-J419127C-omplexImp-edanceCh-eck	50V77W33J4-19127Comple-xImpedanceC-heck		IV - Minor	Open
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				50V77W33-J419127C-omplexImp-edanceCh-eck	50V77W33J4-19127Comple-xImpedanceC-heck		IV - Minor	Open
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk,	HardShort				50V77W33-J419127Iso-lationCheck	50V77W33J4-19127Isolatio-nCheck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

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MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance									
M.mec1.13.0	50V77W33P18371_C3T__3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				50V77W33J419127ComplexImpedanceCheck, 50V77W33J419127DielectricWithstandingVoltageCheck	50V77W33J419127DielectricWithstandingVoltageCheck		IV - Minor	Short to Ground
M.mec1.13.0	50V77W33P18371_C3T__3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance,	BadDielectric				50V77W33J419125ComplexImpedanceCheck, 50V77W33J419125DielectricWithstandingVoltageCheck	50V77W33J419125DielectricWithstandingVoltageCheck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1 DATE 09/07/00

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REFERENCE DRAWING COMPILED BY

MISSION APPROVED BY

IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		HiPotential, DWV, Resistance									
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort				50V77W33-J419125Iso-lationCheck	50V77W33J4-19125Isolatio-nCheck		IV - Minor	Short to Ground
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				50V77W33-J419125C-omplexImp-edanceCh-eck	50V77W33J4-19125Comple-xImpedanceC-heck		IV - Minor	Open
M.mec1.13.0	50V77W33P18371_C3T-_3T1__1	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-	Open				50V77W33-J419125C-ontinuityC-heck, 50V77W33-J419125C-	50V77W33J4-19125Comple-xImpedanceC-heck		IV - Minor	Open

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SYSTEM mec1 DATE 09/07/00

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IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
		n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance					omplexImp-edanceCh-eck				
M.mec1.16.0	50V77W33P171E_C4T_-4T2__2	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	BadDielectric				50V77W33-J507NCo-mplexImpe-danceChe-ck, 50V77W33-J507NDiel-ectricWiths-tandingVol-tageCheck	50V77W33J5-07NDielectric-Withstanding-VoltageCheck		IV - Minor	Short to Ground
M.mec1.16.0	50V77W33P171E_C4T_-4T2__2	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdow-n, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	HardShort				50V77W33-J507NIsola-tionCheck	50V77W33J5-07NIsolationC-heck		IV - Minor	Short to Ground

FAILURE MODE AND EFFECTS ANALYSIS

SYSTEM mec1

INDENTURE LEVEL Component

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IDENTIFICATION NUMBER	ITEM/FUNCTIONAL IDENTIFICATION (NOMENCLATURE)	FUNCTION	FAILURE MODES AND CAUSES	MISSION PHASE/ OPERATIONAL MODE	FAILURE EFFECTS			FAILURE DETECTION METHOD	COMPENSATING PROVISIONS	SEVERITY CLASS	REMARKS
					LOCAL EFFECTS	NEXT HIGHER LEVEL	END EFFECTS				
M.mec1.16.0	50V77W33P171E_C4T_-4T2__2	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	DeltaResistance				50V77W33-J507NComplexImpedanceCheck	50V77W33J5-07NComplexImpedanceCheck		IV - Minor	Open
M.mec1.16.0	50V77W33P171E_C4T_-4T2__2	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance, ACImpedance, HFCrosstalk, Loss_Attenuation, ComplexImpedance, HiPotential, DWV, Resistance	Open				50V77W33-J507NContinuityCheck, 50V77W33-J507NComplexImpedanceCheck	50V77W33J5-07NComplexImpedanceCheck		IV - Minor	Open
M.mec1.16.0	50V77W33P171E_C4T_-4T2__2	Continuity, SeriesResistance, Isolation, Noise, Crosstalk, Reactance, DielectricBreakdown, PinShort, GndShort, DCResistance,	Open				50V77W33-J507MContinuityCheck, 50V77W33-J507MComplexImpedanceCheck	50V77W33J5-07MComplexImpedanceCheck		IV - Minor	Open

APPENDIX F

Processing of SCAN Database Tables

SCAN Database Table Format

The following is the format of the database tables supplied by NASA AMES.

List of Columns for `Mate_Relation_Ames` Table

1. Plug_Comp_Item
2. Plug_Comp_Area
3. Plug_Comp_Subname
4. Jack_Comp_Item
5. Jack_Comp_Area
6. Jack_Comp_Subname
7. PB_State
8. CC
9. Flt_No
10. IC
11. Init_Flow_Config
12. Plug_Status
13. Jack_Status
14. Record_set_Id
15. Package_Id
16. Demate_Hist_Log
17. Mate_Hist_Log
18. Initial_Mate
19. Perm_Demate
20. Unauth_Demate
21. Unauth_Mate
22. Skip_Retest

List of Columns for `Component_Ames` Table

1. Item
2. Subname
3. PB_State
4. Nomen
5. Record_Set_Id
6. Package_Id
7. Pseudo_area
8. AKO
9. Element
10. No_Terms
11. Part_No
12. General_Note_code
13. Flt_No
14. AWL_Mate
15. Qty_Required
16. Line_No
17. Location

18. Mating_Part_No
19. Mcr_No
20. Mcr_Rev
21. Mod_Code
22. Mod_Kit_Doc_No
23. Edit_signature

List of Columns for `Wire_Ames` Table

1. FR_Comp_Item
2. Fr_Comp_Area
3. Fr_Comp_Subname
4. To_Comp_Item
5. To_Comp_Area
6. To_Comp_Subname
7. FR_Pin
8. To_Pin
9. PB_State
10. Record_set
11. Harn_Id
12. Path_Id
13. Sequence
14. Package_Id
15. Upstream_End
16. FR_Zone
17. To_Zone
18. Funct_Remarks
19. Chg_Auth
20. DWG_Code
21. Color
22. Type
23. Cable
24. Circ_Seg
25. Signal_Code
26. Shield_Flag
27. EMC
28. Length

List of Columns for `Path_AMES` Table

1. Id
2. Down_Comp_Item
3. Down_Comp_Area
4. Down_Comp_Subnmae
5. Down_Pin
6. Up_Comp_Item
7. Up_Comp_Area
8. Up_Comp_Subname

9. Up_Pin
10. PB_State
11. CC
12. Nomen
13. Package_Id
14. Dispo_Log_No
15. Retest_Log_
16. Prev_Dispo_Log_No
17. Prev_Retest_Log_No
18. Edit_Signature
19. Edit_Date
20. Proposed_Sys
21. To_Page
22. FR_Page
23. Signal_Code
24. Retest_Flag

`TEAMS-KB Database Table Format`

We wrote a PL/SQL script to convert the SCAN database tables into TEAMS-KB tables, which capture all the necessary topology information. We then wrote a filter in TEAMS that would access these tables using ODBC link and auto-generate the wiring model. The format of the TEAMS-KB tables, with brief explanation is provided next, followed the PL/SQL code listing in Appendix C.

List of Columns for `Connector_Location` Table

1. Connector_Id: The unique identifier of the (upstream) connector
2. Mating_Connector: The unique identifier of the (downstream) mating Connector
3. Location:The direction at which the connector resides corresponding to its mate
4. No_Terms: Number of pins for that connector

List of Columns for `Connector_To_From_Info` Table

1. Connector_From: The start Connnector_Id from which the wire originates (the upstream connector)
2. Pin_From: The starting pin of the above connector for the wire.
3. Connector_To: The end Connnector_Id where the wire terminates (downstream connector)
4. Pin_To: The pin at which the wire terminates
5. Name_Signal: Name of the signal attached to this connector
6. EMC: Electro magnetic compatible
7. Wire_Type: The type of the wire
8. Wire_Length: The length of the wire
9. Dwg_Code: The reference drawing
10. Cable_Descriptor: The description of the cable
11. Up_Stream_End: Indicates which direction the signal is traveling
12. Color: Color of the wire
13. Circ_Seg : Uniquely identifies a wire path

APPENDIX G

PL/SQL script for Database Conversion

```
Declare
    Cursor c1 is select * from Mate_Relation_Ames;
    Row_Mate_Relation C1%rowtype;
    Var_Jack_Item varchar2(120);
    Var_mate varchar2(120);
    Var_Mate1 varchar2(120);
    Var_Mate3 varchar2(120);
     No_Terms Number(10);
     Var_Plug_Item varchar2(120);
     Cursor C2 is select Distinct FR_Comp_Subname,Fr_Comp_Item from Wire_Ames
     where To_Comp_Subname||To_Comp_Item=Var_Plug_Item;
     Row_Mate_Relation1 C2%rowtype;
     Cursor C3 is select Distinct To_Comp_Subname,To_Comp_Item from Wire_Ames
     where Fr_Comp_Subname||Fr_Comp_Item=Var_Plug_Item;
     Row_Mate_Relation2 c3%rowtype;
     Cursor c4 is select * from wire_ames;
     Mating_Relation_Info3 c4%rowtype;
     Duplicate_Value  EXCEPTION;
     PRAGMA Exception_Init (Duplicate_Value, -1);
     Null_Value  EXCEPTION;
     PRAGMA Exception_Init (Null_Value, -1400);

BEGIN
        Open c1;
        Loop
              Begin
                    Fetch c1 into Row_Mate_Relation;
                    Exit when C1%notFound;
                          Var_Jack_Item:=Concat(Row_Mate_Relation.Jack_comp_Subname,Row_
                          Mate_Relation.Jack_comp_Item);
                          Var_Plug_Item:=Concat(Row_Mate_Relation.Plug_comp_Subname,Row_
                          Mate_Relation.Plug_comp_Item);
                          Insert into Connector_Location(Connector_Id, Location,Mating_Connector)
                    Values(      Var_Jack_Item, 'R',var_Plug_Item);
                          Insert into Connector_Location(Connector_Id, Location,Mating_Connector)
                    Values(      Var_Plug_Item, 'L',Var_Jack_Item);
                     Begin
                          Open c2;
                          Loop
                                Begin
                                      Fetch c2 into Row_Mate_Relation1;
                                      Exit when C2%notFound;
                                            Var_Mate1:=concat(Row_Mate_Relation1.FR_Com
                                            p_Subname,Row_Mate_Relation1.Fr_Comp_Item);
                                            Select No_Terms,AWL_Mate into
                                            No_Terms,Var_Mate3 from Component_Ames
                                            where subname||Item=Var_Mate1;
                                            Insert into Connector_Location(Connector_Id,
                                            Location,Mating_Connector,No_Terms)
                                            Values(Var_Mate1 , 'R',Var_Mate3,No_Terms);
                                       Get_Mate_For_Subname(Var_Mate1);

                          Exception when No_Data_Found then
```

```
                        Insert into Connector_Location(Connector_Id,
                        Location,Mating_Connector,No_Terms)
                values(Var_Mate1 , 'R',Var_Mate3,No_Terms);
                 Get_Mate_For_Subname(Var_Mate1);
            When  Duplicate_Value then
                  Null;
            When Null_Value then
                  Null;
            End;
      End loop;
      commit;
      Close c2;
      End;
      Begin
            Open c3;
            Loop
            Begin
                  Fetch c3 into Row_Mate_Relation2;
                  Exit when C3%notFound;
                        Var_Mate1:=concat(Row_Mate_Relation2.To_Comp_Subna
                        me,Row_Mate_Relation2.To_Comp_Item);
                        Select No_Terms,Awl_Mate into No_Terms,Var_Mate3
                        from Component_Ames where subname||Item=Var_Mate1;
                        Insert into Connector_Location(Connector_Id,
                        Location,Mating_Connector,No_Terms)
                  values(Var_Mate1 , 'R',Var_Mate3,No_Terms);
                  Get_Mate_for_subname(Var_Mate1);

                     Exception when no_data_Found then
                        Insert into Connector_Location(Connector_Id,
                        Location,Mating_Connector,No_Terms)
                  values(Var_Mate1 , 'R',Var_Plug_Item,No_Terms);
                  Get_Mate_for_subname(Var_Mate1);
            when  Duplicate_Value then
            Null;
            when Null_Value then
            Null;
      End;
   End loop;
   commit;
   Close c3;
   End;
Exception when duplicate_value then
Null;
End;
 End loop;
commit;
  Close c1;
end;
check_for_direction;
Message('successfully imported scan data base');


PROCEDURE Get_Mate_For_subname(Var_Mate varchar2) IS
```

```
        Num_Times Number(10);
        Var_Mate1 varchar2(120);
        No_Terms number(10);
        Var_Mate2 varchar2(120);
        Duplicate_Value  EXCEPTION;
        PRAGMA Exception_Init (Duplicate_Value , -1);
        Null_Value  EXCEPTION;
        PRAGMA Exception_Init (Null_Value , -1400);
 BEGIN
        Begin
              Select AWL_Mate,No_Terms into Var_Mate1,No_Terms from Component_Ames
where              Subname||Item=Var_Mate;
             Insert into Connector_Location(Connector_Id,Location,Mating_Connector,No_Terms)
        values(Var_Mate1,'L',Var_Mate,No_Terms);
             Get_wiring_Information(Var_mate1);
         Exception when No_Data_Found then
                   Get_wiring_Information(Var_mate1);
        when Duplicate_Value then
             Get_wiring_Information(Var_mate1);
        when Null_value then
              Get_wiring_Information(Var_mate1);
        END;
             Commit;
END;

PROCEDURE Get_Wiring_Information(Var_Mate varchar2) IS
           Cursor c1 is select Distinct FR_Comp_Subname,Fr_Comp_Item from Wire_Ames    where
          To_Comp_Subname||To_Comp_Item=Var_Mate;
           Cursor c2 is select Distinct To_Comp_Subname,To_Comp_Item from Wire_Ames    where
           Fr_Comp_Subname||Fr_Comp_Item=Var_Mate;
         Row_Mate_Relation1 c1%rowtype;
         Row_Mate_Relation2 C2%rowtype;
         Var_Mate1 varchar2(120);
         Var_Mate2 Varchar2(120);
         Var_Mate3 varchar2(120);
         Var_Mate4 varchar2(120);
         Duplicate_Value  EXCEPTION;
         PRAGMA Exception_Init (Duplicate_Value, -1);
        Null_Value  EXCEPTION;
        PRAGMA Exception_Init (Null_Value, -1400);
       No_Terms Number(10);

   BEGIN
        Open c1;
                   Loop
                   Begin
                        Fetch c1 into Row_Mate_Relation1;
                        Exit when C1%notFound;

                                  Var_Mate1:=concat(Row_Mate_Relation1.FR_Comp_Subname,Ro
                                  w_Mate_Relation1.Fr_Comp_Item);
                                  Select No_Terms,AWL_Mate into No_Terms,Var_Mate3 from
                                  Component_Ames where subname||Item=Var_Mate1;
                                  Insert into Connector_Location(Connector_Id,
```

```
                                Location,Mating_Connector,No_Terms)
                        values(Var_Mate1 , 'R',Var_Mate3,No_terms);
                         Get_Mate_for_subname(Var_Mate1);
                    Exception when  Duplicate_Value then
                        Null;
                    when Null_Value then
                        Null;
                    End;
                End loop;
        commit;
        Close c1;
Open c2;
        Loop
            Begin
                Fetch c2 into Row_Mate_Relation2;
                Exit when C2%notFound;
                    Var_Mate2:=concat(Row_Mate_Relation2.To_Comp_Subname,Row_Mate
                    _Relation2.To_Comp_Item);
                    Select No_Terms,AwL_Mate into No_Terms,Var_Mate4 from
                    Component_Ames where subname||Item=Var_Mate2;
                    Insert into Connector_Location(Connector_Id,
                    Location,Mating_Connector,No_Terms)
                 values(Var_Mate2 , 'R',Var_Mate4,No_Terms);
                  Get_Mate_for_subname(Var_Mate2);
             Exception when  Duplicate_Value then
               Null;
             when Null_value then
               Null;
            End;
       End loop;
       commit;
        Close c2;
END;

PROCEDURE Check_For_Direction IS
         Cursor c4 is select * from wire_ames;
        Mating_Relation_Info3 c4%rowtype;
        Var_Connector2 varchar2(120);
        Connector_from varchar2(120);
        Var_Location1 varchar2(120);
         Var_location2 varchar2(120);
        Var_UpStream_End varchar2(1);
         cannot_del_parent  EXCEPTION;
         PRAGMA Exception_Init (cannot_del_parent, -1);
Begin
       Begin
          Loop
            Begin
             If Not C4%ISOpen then
                    Open c4;
             End if;
             Fetch C4 into Mating_Relation_Info3;
              EXIT when C4%NOTFOUND;
```

```
                Var_Connector2:=concat(Mating_Relation_Info3.To_Comp_Subname,Mating_Rel
                ation_Info3.To_Comp_Item);
                Connector_From:=concat(Mating_Relation_Info3.Fr_Comp_Subname,Mating_Rel
                ation_Info3.Fr_Comp_Item);
                Select Location into Var_Location1 from Connector_Location where
                connector_Id=Var_Connector2;
          If (Var_Location1='R') then
                Insert into
                Connector_To_From_Info(Connector_From,Pin_From,Name_Signal,Connector_T
                o,
                Pin_To,EMC,Wire_Type,Wire_Length,Dwg_Code,Cable_Descriptor,Up_stream_E
                nd,Color,Circ_Seg)
             Values(Connector_From,Mating_Relation_Info3.FR_Pin,
                   Mating_Relation_Info3.Funct_Remarks,Var_Connector2,
               Mating_Relation_Info3.To_Pin,Mating_Relation_Info3.EMC,
                  Mating_Relation_Info3.Type,Mating_Relation_Info3.Length,
              Mating_Relation_Info3.Dwg_Code,Mating_Relation_Info3.Cable,
                 Mating_Relation_Info3.UpStream_End,Mating_Relation_Info3.Color,
                 Mating_Relation_Info3.Circ_Seg);
        Else
          If ( Mating_Relation_Info3.UpStream_End='T') then
                 Var_UpStream_End:='F';
            Else
                Var_UpStream_End:='T';
             End if;
                  Insert into
                Connector_To_From_Info(Connector_From,Pin_From,Name_Signal,Connector_T
                o,
                Pin_To,EMC,Wire_Type,Wire_Length,Dwg_Code,Cable_Descriptor,Up_stream_E
                nd,Color,Circ_Seg)
                  Values(Var_Connector2,Mating_Relation_Info3.To_Pin,
              Mating_Relation_Info3.Funct_Remarks,Connector_From,
              Mating_Relation_Info3.Fr_Pin,Mating_Relation_Info3.EMC,
              Mating_Relation_Info3.Type,Mating_Relation_Info3.Length,
              Mating_Relation_Info3.Dwg_Code,Mating_Relation_Info3.Cable,
              Var_UpStream_End,Mating_Relation_Info3.Color,
              Mating_Relation_Info3.Circ_Seg);
        End if;
         Exception when No_Data_Found then
          Null;
       when cannot_del_parent then
         Null;
      End;
   End Loop;
    Commit;
     Close c4;
   End;
End;
```