3D sensors

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3Dc

Outline

1. introduction
2. technology
3. calculations
4. first results
5. radiation damage
6. a puzzle (for now)
7. speed
8. TOTEM
9. active edges
10. yield
11. ATLAS pixels
12. FP420
13. molecular biology
14. conclusions

3Dc

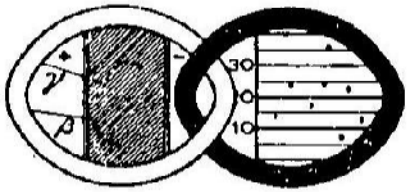
1. **Solid-state semiconductor diode radiation sensors were first made and used by Pieter Jacobus Van Heerden, a graduate student in the occupied Netherlands during World War II, and have been in use for over 50 years.**

2. **Planar technology was invented by Jean A. Hoerni of Fairchild Semiconductor in 1957- 8, around the time he, Robert Noyce and Gordon Moore left the original (and massively mismanaged) semiconductor company, Shockley Semiconductor, to help form the second one, Fairchild Semiconductor. Within 6 years, planar technology was used for silicon PIN diode sensors** (T. Madden, W. Gibson, *Rev. Sci. Instr*. 34 (1963) 50).

THE CRYSTALCOUNTER
A NEW INSTRUMENT IN NUCLEAR PHYSICS

Erik Heijne → Sherwood Parker
With compliments.

× 7.6 eV / e-h pair in AgCl



× Energy loss of electrons
fig 30 on p. 64

× drawing of AgCl detector crystal
fig 8 p. 23

P. J. VAN HEERDEN

THE CRYSTALCOUNTER
A NEW INSTRUMENT IN NUCLEAR PHYSICS

PROEFSCHRIFT

TER VERKRIJGING VAN DEN GRAAD VAN DOCTOR IN DE WIS- EN NATUURKUNDE AAN DE RIJKSUNIVERSITEIT TE UTRECHT, OP GEZAG VAN DEN RECTOR MAGNIFICUS, J. BOEKE, HOOGLEERAAR IN DE FACULTEIT DER GENEESKUNDE, VOLGENS BESLUIT VAN DEN SENAAT DER UNIVERSITEIT TEGEN DE BEDENKINGEN VAN DE FACULTEIT DER WIS- EN NATUURKUNDE TE VERDEDIGEN OP 30 JULI TE 3 UUR,

DOOR

PIETER JACOBUS VAN HEERDEN
GEBOREN TE UTRECHT

AMSTERDAM
N.V. NOORD-HOLLANDSCHE UITGEVERS MAATSCHAPPIJ
1945

1945

(but work done during WW2 in German occupied low-countries)

INTRODUCTION.

It is a fascinating idea, when using a GEIGER–MULLER-counter, that every kick of the instrument means that one submicroscopic particle has passed through it. The GEIGER–MULLER-counter however does not tell anything more about the particles thus observed. The tube shows a voltage-pulse of a fixed size, when one or more ions are formed in it, either by α-, β-, or γ-radiation, cosmic rays, ultraviolet light or by some unknown effect of the wall of the tube.

In the present work it was tried to develop a new instrument, the crystalcounter, which would informe us about the energy as well of every particle detected. It was found, that the ionization of the radioactive radiation in crystals like silverchloride is so large that the voltage-pulse of every single particle, if sufficiently amplified, can be observed and be measured.

This voltage pulse appeared to be proportional to the energy of the particle under suitable experimental conditions. So, in principle, the crystalcounter enables us to measure the energy-spectrum of every weak radioactive radiation that can be detected.

CONTENTS.

areas, which have a large heatresistance. When the diameter of the contactarea is a, and the heatresistance of one cm³ of the body is c, then the heat resistance of a contact is of the order of $\frac{c}{a}$. Apparently, the areas of real contact of two bodies, pressed against each other are very small. So, when the air is pumped away, the heatresistance becomes very large. We brought therefore paraffine-oil between all surfaces, which must make good thermal contact. In this way the cooling was much better and we could start the observations after cooling 40 minutes.

A thin steel wire, screened off by a metal tube, connected the crystal with the first valve. The table on which the β-ray spectrograph, the mercurypump and the first valve of the amplifier were mounted was placed on rubbercushions to keep away mechanical vibrations. The further apparatus was as described in chapter III.

§ 2. *Experimental results.*

In figure 30 the distribution curve is given for the deflections we got with homogeneous β-radiation of $Hp = 2500$. We see one peak, which goes down to zero at the side of the large deflections. At the

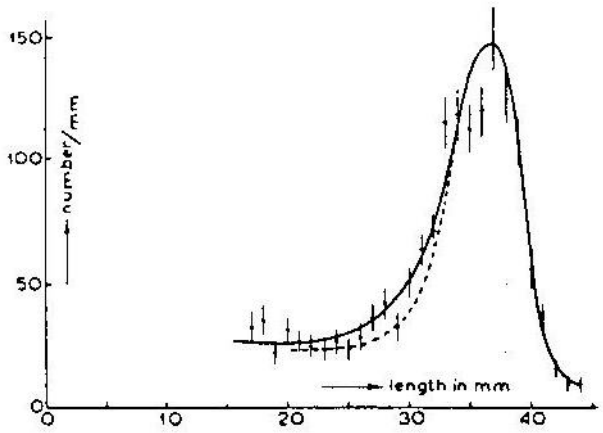


Fig. 30. The distribution curve of the deflections caused by homogeneous β-rays. $H\varrho = 2500$; $E = 0{,}4$ M.e.V. $V = 200$ volt; 1 mm = 1200 e.c.
Dotted: curve expected theoretically.

THE FOUR-LAYER DIODE IN THE CRADLE OF SILICON VALLEY

Kurt Hubner
CH - 3086 Zimmerwald, Switzerland

When William Shockley left Bell Laboratories to establish his own operation in California, he selected an exotic two-terminal switch, the bistable silicon *p-n-p-n* diode as his main commercial product. This business venture eventually failed, but gave birth to *Silicon Valley*. With silicon transistors at hand, why did Shockley jeopardize his business career with such a device ? Why did it function only with silicon ? How was the diode made, what were the applications and why did it fail ? Answers are attempted from personal experience in Shockley's company.

Jean Hoerni, one of Shockley's "8 traitors", may have invented the planar process during this time

HOW IT STARTED

William Shockley never really returned to Bell Laboratories after his leave of absence with the department of defense in Washington. Instead, backed by Beckman Instruments Inc., he set up the Shockley Semiconductor Laboratories in Mountain View, California.

DEVICE PROCESSING IN THE FIFTIES

This advanced, all diffused silicon device was successfully developped in an old fruit barn on gravel surfaced San Antonio Road in Mountain View. Today there is a shopping center, but still in 1959 the author jumped the fence at coffee break to pinch a fruit in the bordering orchard. Diffusion furnaces, fume hoods, machine shop and desks were all in the same open space. The high, old roof structure, and the few windows were impossible to clean and were full of dust and dirt. Seen in retrospective, it is a miracle, that such pertinent and good work could be accomplished under these working conditions. Apparently, gettering of unwanted impurities during processing made it possible, even if this phenomena was only understood later on (15). But Shockley and his crew realized, that production could only be done successfully in a reasonably clean environment. Beckman Instruments Inc. made space available in a new building of its Spinco Division in the Stanford Industrial Park in Palo Alto. There, what probably was the most modern integrated silicon device production facility at that time, was installed. When Clevite bought the Shockley operation, production and R+D were moved into a new building nearby at the corner of Junipero Serra and Page Mill Roads.

3Dc

Date: Sun, 16 Nov 2003 01:56:05 -0800 (PST)
From: Sherwood Parker <sher@slac.stanford.edu>
To: k.huebner@bluewin.ch
Cc: jbeaudouin@earthlink.net
Subject: the planar method

I have a question about the origin of the planar method that Jacques Beaudouin thinks you may be able to answer: how, and when did Jean Hoerni invent the planar method for oxide passivated diode junctions? He seems to think it may have been partly accidental, but didn't start at Shockley Semiconductor until after Hoerni and the others had left for Fairchild and so cannot be sure.

(In case you are wondering, this is what led to my curiosity:)

I started to learn about integrated circuit and silicon radiation detector fabrication technology in 1980. Before then I'd been working with gas filled tracking chambers for high energy physics research. Silicon PIN diode microstrip detectors had recently been introduced, but required large fanout boards and massive cable bundles to connect their many strips with their discrete-transistor readout electronics.

When three of us (Bernard Hyams of CERN who initiated the project, Terry Walker of Stanford and I) decided to try to make the world's first custom integrated circuit to read them out, I met Jacques Beaudouin who approved the project, and have kept in touch with him since.

Date: Sun, 16 Nov 2003 19:50:44 +0100
From: k.huebner <k.huebner@bluewin.ch>
To: sher@SLAC.Stanford.EDU
Cc: Jacques Beaudouin <jbeaudouin@earthlink.net>
Subject: planar method

Non selective oxide masking of one side of a silicon wafer against diffusion was already used for the manufacture of the Four Layer Diode at Shockley. The technology for this diode also was used for the mesa transistor, Fairchild's first product, by the 8 who left Shockley in 1958. A major problem of both products were the unstable surface leakage currents across the etched exposed junction surface. Jean Hoerni's idea was to diffuse the junction at the surface of the silicon under the oxide layer in order to obtain a low and stable leakage current. This required selective oxide masking. The planar all diffused reliable silicon transistor was born and was a great succes. Only afterwards were such transistors interconnected by evaporated aluminium over the planar surface to yield an integrated circuit, also a Fairchld first (if one neglects the Germanium hay wire construction of TI). The first Fairchild IC was four planar transistors on one chip, followed by simple gate circuits.

This is how I remember it. A literature and patent search would yield more precise information.

Greetings
Kurt Hubner

Silicon p-n particle detectors were described in a post-deadline paper at the recent meeting of the American Physical Society. These devices were reported to resolve easily the 122 kilovolt and 136 kilovolt γ rays of cobalt 57 with a 6.8 kilovolt resolution. They were 4 millimeters in diameter. Operating with a 300 volt reverse bias, they had a 0.8 millimeter depletion ratio and gave 1 millivolt per Mev with α-particles. These detectors measure quantitatively the ionization produced by charged particles and have circuit properties which are likely to lead to applications of considerable importance in many areas of nuclear physics and high energy physics research.

Attached is a recipe for these detectors. They don't seem very hard to make.

Herbert L. Anderson

May 2, 1960

(Herbert Anderson, a post-doc of Enrico Fermi, placed the last graphite blocks on the first reactor, the night before the first controlled chain reaction was achieved. We were working together on the μ □ e + γ experiment at the time he became interested in silicon detectors. Being rather slow, it took me 20 more years.)

3Dc

P. F. Donovan's

Recipe for Paint-on Particle Detectors

The silicon used has been obtained from Merck and is vacuum floating zone high resistivity p-type, in the range 250 to 10,000 ohm cm. Wafers have been cut with a diamond saw lapped with 600 mesh carborundum and then etched in 21 parts nitric and 4 parts hydrofluoric acid to a sufficient depth to remove the region of the surface damaged by the cutting and lapping operations. This means etching the order of a few mils.

The P_2O_5 solution is painted on one surface with a q-tip type applicator, allowed to dry, visually inspected for completeness of coverage and repainted if necessary. An oven with a thermal time constant the order of a couple of hours is heated to 950° C. The painted slice is introduced into the oven in a small quartz boat in air and the oven is turned off after sample reaches ~930°C. When the oven temperature has dropped to below 200°C, the sample is removed. The wafer is etched in HF to remove any glasses and oxides formed during the heat treatment. A region of the diffused surface is masked with apiezon wax applied as a thick solution in trichloethylene. This is heated moderately so that the wax adheres well to the surface. The wafer is then etched as described above, etching through the diffused layer into the base material. The device is washed and dried. The apiezon wax is removed with toluene, washed in alcohol, then water and dried. At this point one should have a rectifier, measuring between the diffused layer, which was protected by the apiezon wax, and the base p material. A large area silver paint contact can be made on the bottom and a wire, perhaps aided by a dot of silver paint, contacts the diffused layer. The diode may be a very poor counter because of noise resulting from surface leakage. It can often be made good by a soak in HF followed, without exposure to air, by wash in water.

Silicon Dioxide Passivation of p-n Junction Particle Detectors

T. C. Madden and W. M. Gibson
Bell Telephone Laboratories, Inc., Murray Hill, New Jersey
(Received 24 September 1962; and in final form, 31 October 1962)

1962

Silicon p-n junction particle detectors present unusual passivation problems because of the shallow diffusions and large exposed junction areas involved. The use of silicon dioxide films for reducing the ambient sensitivity of junction detectors has been investigated, and grown-oxide films produced with high pressure steam have been studied in detail. The dependence of ambient sensitivity on such parameters as bulk silicon resistivity, diffusant, and diffusion temperature has been investigated. Methods of fabrication of ambient insensitive diodes and more complicated guard-ring structures are also discussed.

INTRODUCTION

A SERIOUS problem in the use of semiconductor particle detectors is the sensitivity of the reverse leakage current and breakdown voltage to ambient effects. Windowless operation is necessary when making precise energy or short-range particle measurements, and this precludes encapsulation of the detector in the manner used for transistors.

That portion of a p-n junction which principally controls the reverse characteristics is at the edge where the high electric field comes to the surface.[1] In this work, passivation of phosphorus-diffused p-n junction particle detectors by covering the junction edge with a silicon dioxide film was investigated.

Silicon dioxide films can be formed by pyrolytic decomposition of volatile organic silane compounds,[2] reactive sputtering of silicon,[3] anodic deposition,[4] thermal oxidation in dry or wet oxygen at atmospheric pressure,[5] and oxidation in high pressure steam.[6] After considering the known properties of films produced by these processes, we concluded that those grown in high pressure steam showed the most promise for the present application. In addition to the favorable passivation properties of this type of oxide, the closed system used offers convenience in maintaining cleanliness and control and the low oxidation temperature ($\leq 650°C$) minimizes lifetime degradation effects. Considerable information on the mechanism, kinetics, and properties of steam grown oxides is available from the work of Ligenza[6,7] and Ligenza and Spitzer.[8,9]

Two configurations for oxide protected particle detectors are shown in Fig. 1.[10] Figure 1(a) shows a deep diffusion of phosphorus (≈ 2–$3\ \mu$) into p-type silicon, followed by oxidation. The oxide film must be thinner than the diffused layer so that removal of a window in the oxide will leave a portion of the junction surface exposed. The junction edges remain under the oxide. Detectors have been fabricated in this fashion with $>1\ \mu$ diffused layers, but it is difficult to control the diffusion and oxidation rates with sufficient precision to achieve the thin diffused layers ($\approx 0.1\ \mu$) often desired. In addition, removal of the outer layer of the diffused silicon by the oxidation process results in a low surface concentration, which necessitates evaporation of a thin metal film to reduce the high sheet resistance of the front surface. This method does not require heating the sample after the oxidation, which can cause changes in the oxide film, as will be shown later. If a window thickness of the order of $1\ \mu$ is acceptable, this is probably the preferred fabrication technique.

The structure illustrated in Fig. 1(b) involves growth of an oxide film, removal of a "window" in the oxide, and diffusion of phosphorus through the window. The silicon dioxide film, being relatively impervious to the phosphorus, acts as a mask to define the junction area. This method, which allows both thin diffusions and high surface concentrations, is the one investigated in this work.

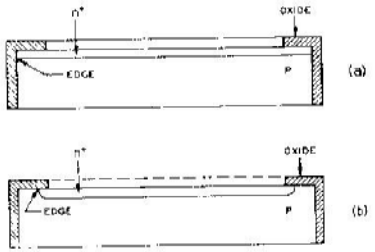
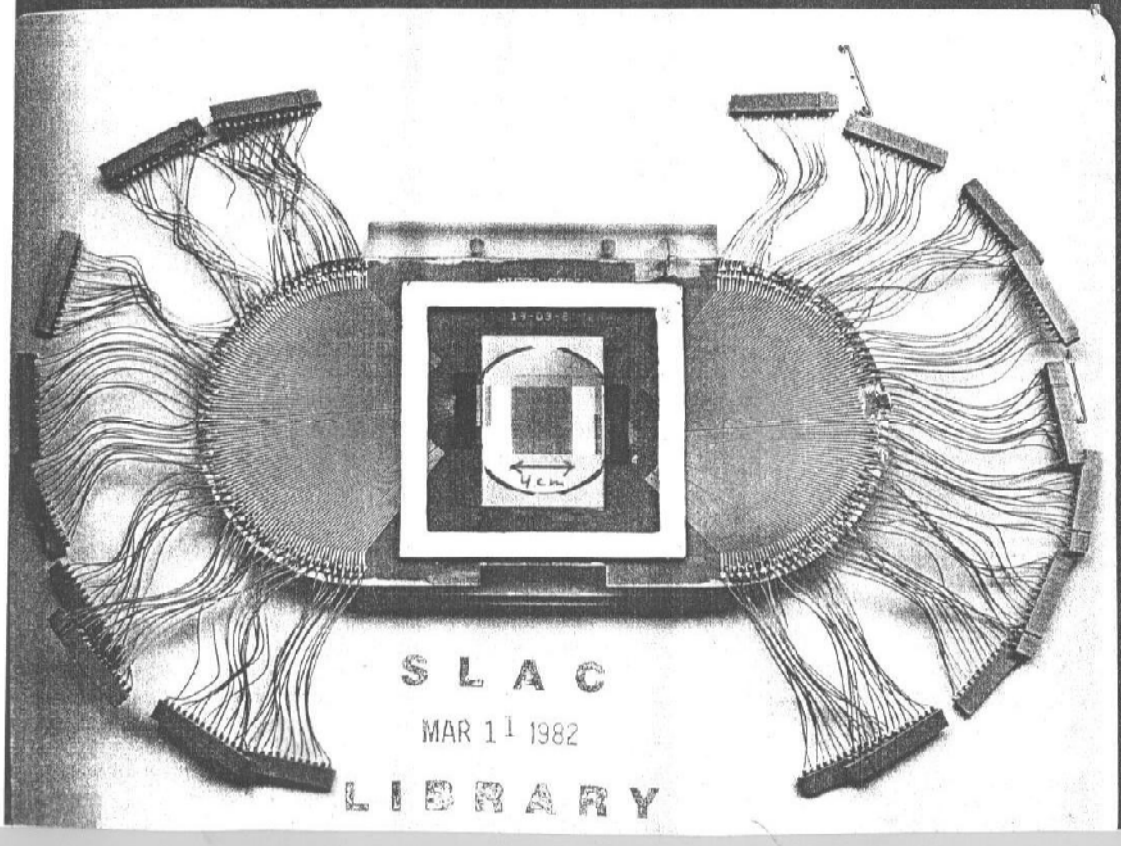


FIG. 1. Possible oxide protected diode structures. The structure used in this work is shown in (b).

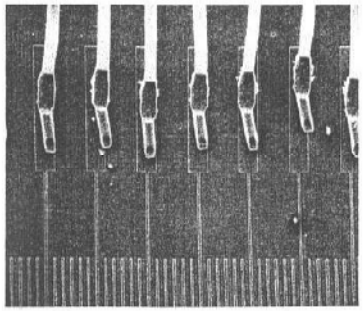
[1] L. M. Lark, "Semiconductor Nuclear Particle Detectors," Proceedings of the Ashville Conference, Report NAS-NS-32, Publ. 871 (1961), p. 131.
[2] E. Jordan, J. Electrochem. Soc. 108, 478 (1961).
[3] W. R. Sinclair and F. G. Peters, J. Am. Ceramic Soc. (to be published).
[4] R. J. Archer, J. Opt. Soc. Am. 52, 970 (1962).
[5] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, Bell System Tech. J. 38, 749 (1959).
[6] J. R. Ligenza, J. Electrochem. Soc. 109, 73 (1962).
[7] J. R. Ligenza, J. Phys. Chem. 65, 2011 (1961).
[8] J. R. Ligenza and W. G. Spitzer, J. Phys. Chem. Solids 14, 131 (1960).
[9] W. G. Spitzer and J. R. Ligenza, J. Phys. Chem. Solids 17, 196 (1961).
[10] W. M. Gibson, "Semiconductor Nuclear Particle Detectors," Proceedings of the Ashville Conference, Report NAS-NS-32, Publ. 871 (1961), p. 232.

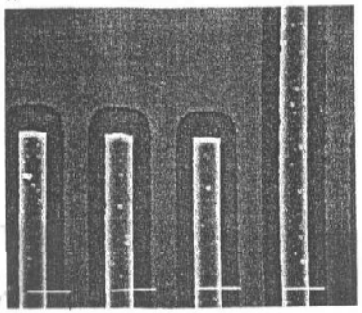
3Dc

CERN COURIER



Photographs taken with an electron microscope at CERN showing details of the intricate connections which have to be made on the silicon wafer in the semiconductor detector. 1 — wires, about 120 microns apart, are bonded onto the wafer. 2 — an enlarged view of the strip pattern on the wafer. The strips are 20 microns apart.





2.

The silicon sensor is the dark rectangle in the center. The width of the fanout if every strip were read out: 1 meter

3Dc

Paul Karchin in front of a silicon telescope (the rest of the photograph: fanouts and cables).
(Fermilab; 1985, 9 planes, 5 cm x 5 cm)

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NUCLEAR INSTRUMENTS AND METHODS 169 (1980) 499-502. © NORTH-HOLLAND PUBLISHING CO

FABRICATION OF LOW NOISE SILICON RADIATION DETECTORS BY THE PLANAR PROCESS

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1979

Received 30 July 1979 and in revised form 22 October 1979

Dedicated to Prof. Dr. H.-J. Born on the occasion of his 70th birthday

By applying the well known techniques of the planar process: oxide passivation, photo engraving and ion implantation, Si pn-junction detectors were fabricated with leakage currents of less than 1 nA/cm^2/100 μm at room temperature. Best values for the energy resolution were 10.0 keV for the 5.486 MeV alphas of ^{241}Am at 22 °C using 5 × 5 mm^2 detector chips.

1. Introduction

For many years Si-surface barrier detectors have been used for the spectroscopy and detection of charged particles. As the dead layer of these detectors can be reduced to less than 1000 Å they are especially useful for experiments with heavy ions. In contrast to the technology for the fabrication of diffused or ion implanted pn-junction detectors the techniques for the preparation of surface barriers avoids any high temperature treatment. As a consequence the lifetimes of the charge carriers are not reduced during the fabrication steps, leading to very small generation currents. As the generation current I_G can be expressed by the intrinsic concentration n_i, the volume V and the lifetime τ according to $I_G = n_i V/(2\tau)e$V, ($e = 1.6 \times 10^{-19}$ As, $n_i = 1.5 \times 10^{10}$ cm^{-3}) the generation currents for surface barriers are about 12 nA/cm^2/100 μm using silicon slices with lifetimes of 1000 μs. Though the generation current is very low, surface barrier detectors show a much higher reverse current which must be attributed to a surface leakage current component. In addition, the fabrication cycle is very time consuming, as every single detector must be fabricated and tested individually. These drawbacks can be overcome by fabricating pn-junction detectors applying the so-called planar process. Combining the techniques of oxide passivation, photo engraving and ion implantation, it is possible to get a large number of detector chips with only small tolerances in their geometrical and electrical properties. Oxide passivation of the surface is a useful method for the reduction of leakage currents, whereas ion implantation allows the tailoring of asymmetric nearly abrupt pn-junctions with thin dead layers. The photo engraving technique not only enables precise geometrical configurations of the chips but also allows a change of the geometry just by using another mask.

Though the planar process is a well known and useful technique for the production of electronic devices, up to now, only little effort was made to apply it to the fabrication of radiation detectors[1].

References

1) G. Keil and E. Lindner, Nucl. Instr. and Meth. **101** (1972) 43.

Nuclear Instruments and Methods in Physics Research 226 (1984) 89–93
North-Holland, Amsterdam

Section III. Detector technology

IMPROVEMENT OF DETECTOR FABRICATION BY THE PLANAR PROCESS

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A planar process is described, which enables the fabrication of low noise high quality Si radiation detectors, by using ion implantation for doping and oxide passivation for reduction of the leakage current. Several technological problems are discussed associated with detector fabrication. Finally, the technical possibilities and economical limits are considered.

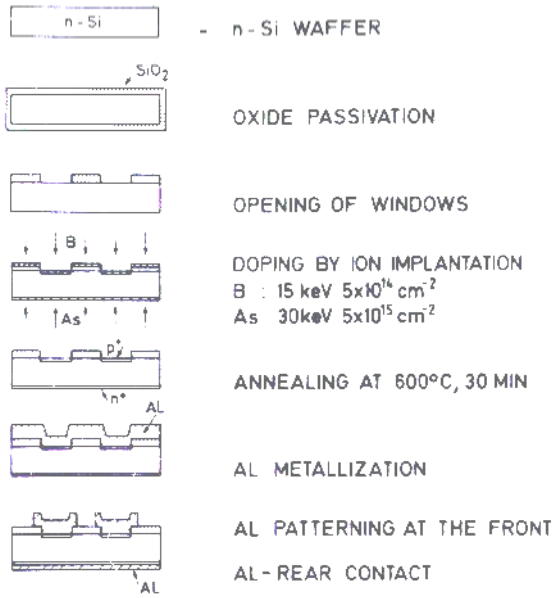

Fig. 2. The planar process for detector fabrication.

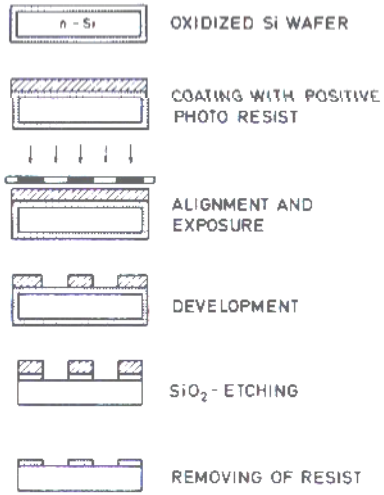

Fig. 4. The photolithographic process.

Nuclear Instruments and Methods in Physics Research 226 (1984) 200–203
North-Holland, Amsterdam

DEVELOPMENT OF HIGH DENSITY READOUT FOR SILICON STRIP DETECTORS

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A compact readout for silicon strip detectors is being developed. It employs an nMOS circuit with 128 channels of charge sensitive amplifiers and multiplexed output.

Silicon strip detectors may have channel-to-channel spacings that are two to three orders of magnitude smaller than that of the electronics to which they have been connected [1]. Telescopes for fixed target experiments usually have used fan-out boards that have dwarfed their detectors to make the necessary match. Fan-outs of this sort will not be practical around the intersection points of colliding beam machines such as SLC and LEP where 25 to 50 thousand channels might be packed within a radius of a few cm. In addition, significant problems arise in setting and monitoring that many thresholds. This article describes an integrated circuit under development that will amplify, integrate and store 128 detector signals and, on command, output the multiplexed information on a single line. Pulse height information is preserved. Thus spatial resolution can be improved with weighted center-finding. dE/dx data is provided, noise and detector problems can be more easily recognized and thresholds can be set by the computer in the form of a decision to pass or not pass a given pulse. The input spacing is 47.5 μm. With amplifiers at each end, one-to-one readout is possible for detectors with strip pitch of less than 25 μm. Calibration pulses can be applied to each input.

Fig. 1 shows a schematic diagram of the system. Two inputs are provided to each channel: one from the strip detector and one capacitively coupled from a calibration line. Input protection is provided by a diode which shorts negative signals to the substrate and two normally-off transistors, which short large positive signals. The amplifier is designed to have an open loop gain, A, of 500, a delay time of about 10 ns and a rise time of about 20 ns. In the off state, the reset and store switches are closed and the output switches are open. Just before data collection starts, the reset is opened. A charge, q, coming from the detector is then stored on C_{int} producing an output voltage of q/C_{int} which is also impressed on C_{store}. Since the effective amplifier input capacitance, $(A+1)\times C_{int}$ is much larger than the capacitance of typical detector strips, most of the generated charge will be collected. At the end of data collection, the store switch is opened and then the reset switch is closed. During readout, the switches controlled by the shift register are closed sequentially, one channel at a time, as a low-voltage level makes its way along the read-bit path of the two phase shift register. The voltage

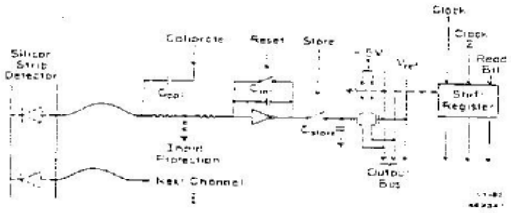

Fig. 1. Schematic view of readout method.

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(North-Holland Physics Publishing Division)

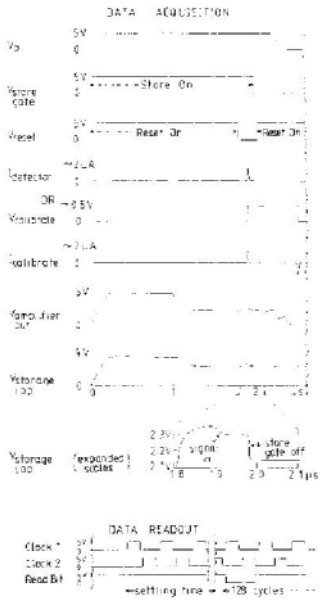


Fig. 2. Sequence of signals. The amplifier supply voltage, V_p, is turned on only during data collection. The output signals are from a computer simulation.

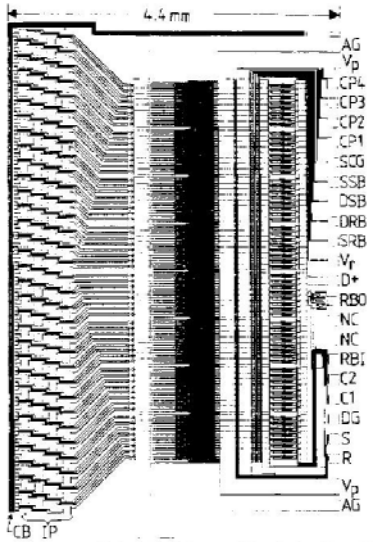


Fig. 3. Enlarged view of chip layout: AG = Analog Ground; D + = Digital + 5; V_p = Analog + 5 (Pulsed); RBO = Read Bit Out; CP4 = Calibrate Pulse 4; NC = No Connection; CP3 = Calibrate Pulse 3; RBI = Read Bit In; CP2-Calibrate Pulse 2; C2 = Clock 2; CP1-Calibrate Pulse 1; C1 = Clock 1; SCG = Storage Cap Ground; DG = Digital Ground; SSB = Source, Signal Bus; S = Store; DSB = Drain Signal Bus; R = Reset; DRB = Drain, Ref Bus; IP = Input Pads; SRB = Source, Ref Bus; CB = Calibrate Buses; $V_r = V_{ref}$.

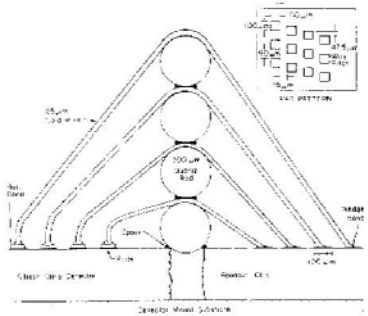


Fig. 4. Method for connecting detector with amplifier.

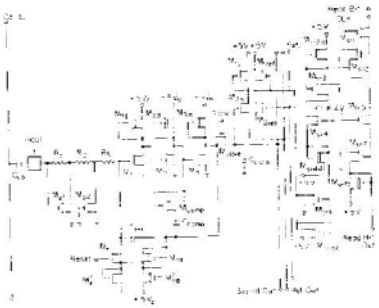


Fig. 5. Circuit diagram of one channel.

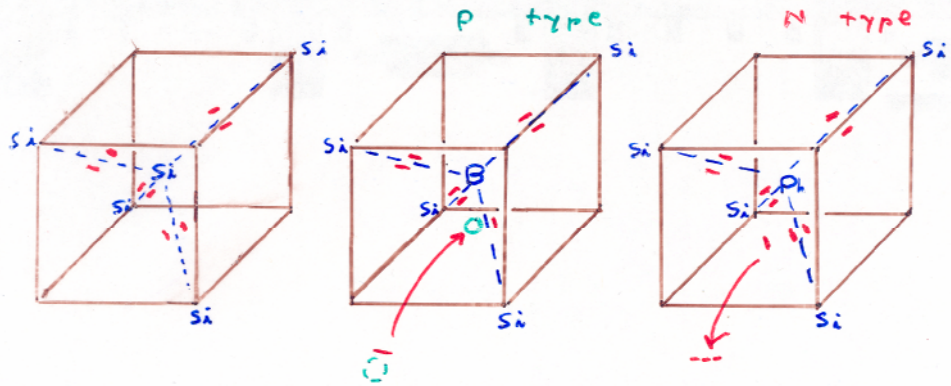
3. With planar technology, all fabricated elements are located on or very close to the wafer surfaces, and oxide passivation layers tie up otherwise loosely bound surface charges, except along the saw-cut edges which must be separated from the sensitive volume.

4. With the development of microstrips (England, Hyams, Hubbeling, Vermeulen, Weilhammer), and in 1982 - 4, the Microplex chip (Walker, Parker, Hyams) – the first custom VLSI readout chip (which also used planar technology), silicon detectors started their wide use as particle trackers in high-energy collider experiments.

5. Now, for experiments at the Large Hadron Collider and for structural molecular biology, we are building a new kind of silicon sensor: 3D.

3Dc

Holes and Electrons in Silicon



Hole motion $B^{(-)}$ $Ph^{(+)}$

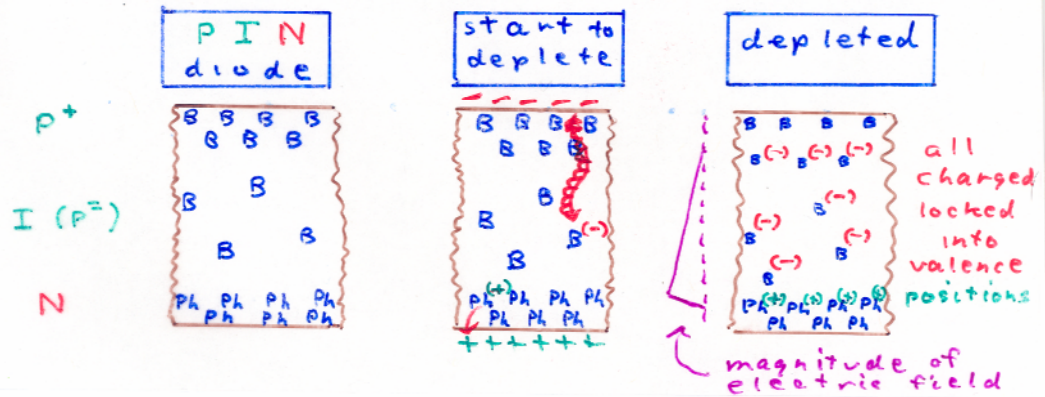
[P (positive) mobile charge]

[by nearby electron jumping into old hole and leaving new one behind]

[N (negative) mobile charge]

[electron just moves - same one all the way]

[note : both P and N type mostly Si, few B or Ph] 5.0×10^{22}/cc



3Dc

Why do we use the PIN structure? A semiconductor conducts, and at room temperature (except in 217 where I froze yesterday)

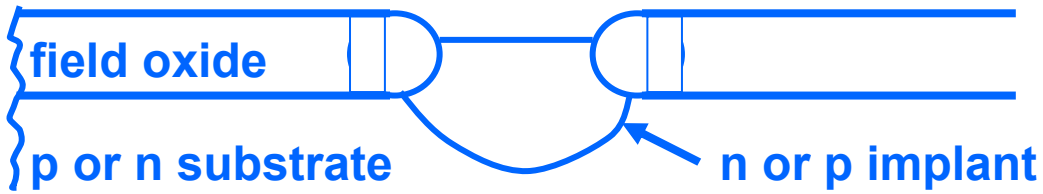
KT ≈ 0.026 eV

and in semiconductors with ~ 1eV band gaps, thermal leakage currents will dominate the signals.

Some types of PIN radiation sensors

- surface barrier – thin layers of metal with different work functions on top and bottom surfaces (thin entrance window but delicate and temperamental)

- planar technology – diode junction (with its high fields) ends at an oxide layer – the current standard for high energy physics



- monolithic – very high signal-to-noise and so very high spatial resolution – but you have to make the readout circuit yourself.

3Dc

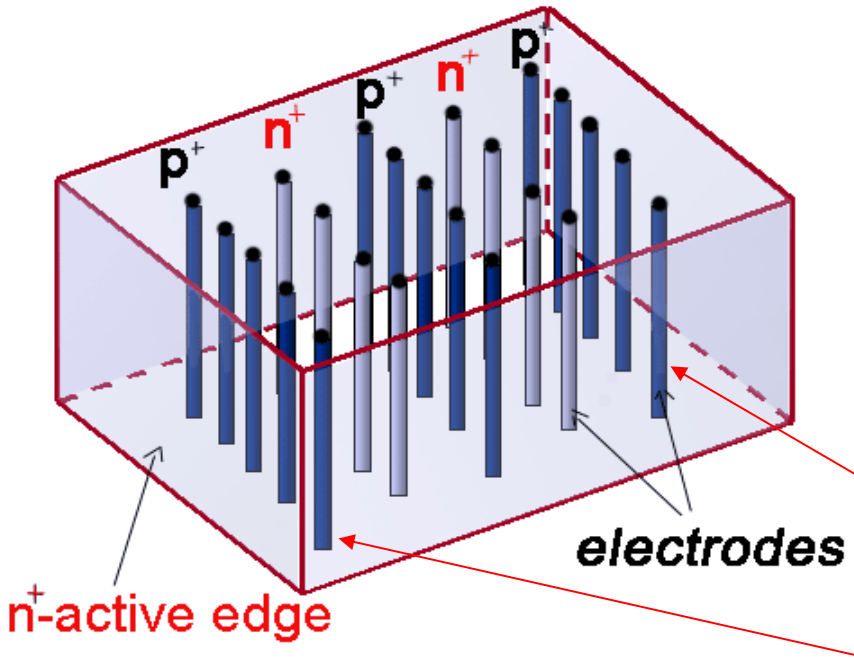
- **MAPS: epi layer (from commercial CMOS) as the sensor:**
  - **++ MUCH easier to order than make, no bump bonding, small pixels possible, low input capacitance, thin (low scattering, may help lower x-ray backgrounds)**
  - **– over most of the area charge carriers have to diffuse to collection electrode so slow – and slow means extreme radiation hardness out of reach, thin means small signals or low x-ray detection efficiency**

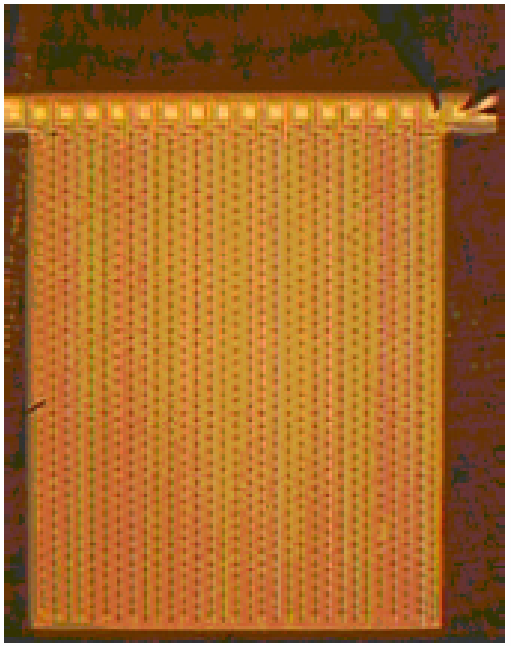
- **planar / 3D active edge:**
  - **standard (0.1 – 1 mm dead edge) drops to about ~1μm**
  - **allows making large area detector from small units without dead bands crossing the image plane**
  - **small units means high yield**

- **full 3D, active edge:**
  - **fast**
  - **extreme radiation hardness**
  - **1μm dead edge**

3Dc

INTRODUCTION





3D silicon detectors were proposed in 1995 by S. Parker, and active edges in 1997 by C. Kenney.

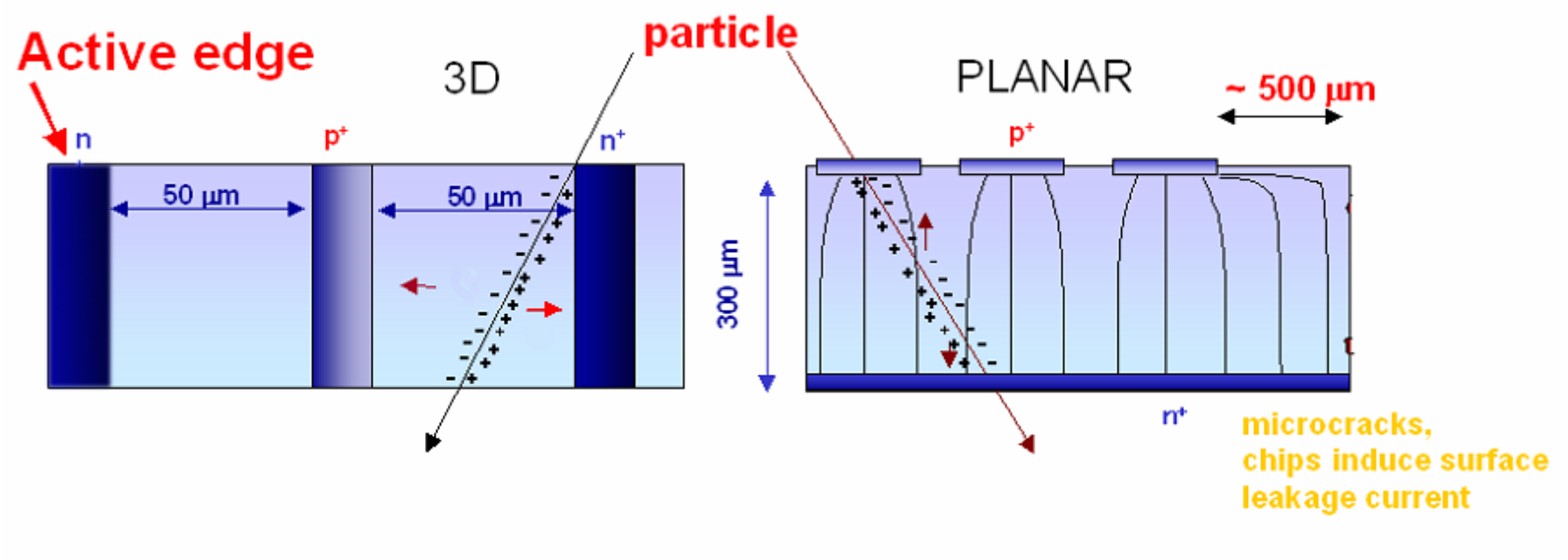
Combine traditional **VLSI** processing and **MEMS** (Micro Electro Mechanical Systems) technology.

Electrodes are processed inside the detector bulk instead of being implanted on the Wafer's surface.

The edge is an electrode! Dead volume at the Edge < 2 microns! Essential for
-Large area coverage
-Forward physics

3Dc

1. NIMA 395 (1997) 328
2. IEEE Trans Nucl Sci 46 (1999) 1224
3. IEEE Trans Nucl Sci 48 (2001) 189
4. IEEE Trans Nucl Sci 48 (2001) 1629
5. IEEE Trans Nucl Sci 48 (2001) 2405
6. CERN Courier, Vol 43, Jan 2003, pp 23-26
7. NIMA 509 (2003)86-91
8. NIMA 524 (2004) 236-244


Active edge
3D
particle
PLANAR
~ 500 µm
n
p+
n+
50 µm
50 µm
300 µm
p+
n+
microcracks,
chips induce surface
leakage current

3Dc

Some properties of 3D radiation sensors:

1 Long tracks can have short drift distances.

2 They have a lower ratio of peak to drift electric fields and so are less likely to have voltage breakdowns.

3 They can be depleted, and have full sensitivity, at lower bias voltages.

4 The geometric nature of this means there will be a low increase of depletion voltage with radiation damage.

3Dc

5. They have rapid charge collection, and charges in perpendicular tracks come in simultaneously, rather than one at a time from the track ends, so they can make order-of-magnitude shorter pulses.

This speed is maintained, as expected, in heavily irradiated sensors, and is useful in reducing capture losses regardless of amplifier speeds.

6. With fields directed away from, rather than along pixel or strip boundaries, they have reduced charge-sharing.

Charge-sharing may be used to improve spatial resolution, but may also take tracks below threshold in radiation damaged silicon, particularly with planar sensors.

7. Active edges provide full sensitivity to within a few microns of the physical edges, in contrast with the large dead regions of standard planar technology (1.1 mm in the Atlas and CMS pixel sensors which must allow for many concentric guard rings).

8. Bias voltages can be made to vary across 3D sensors. (useful if radiation damage and so depletion voltages are much higher at, for example, edges)

BUT

they require more fabrication work.

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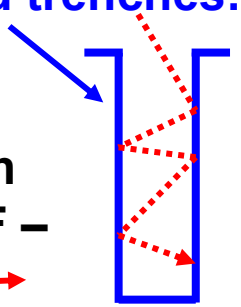
3Dc

Keys to the technology

1. Plasma etchers can now make deep, near-vertical holes and trenches:
   a. SF6 in plasma → F, F – → driven onto wafer by E field
   b. Si + 4F → SiF4 (gas)
   c. SF6 replaced with C4F8 → CF2 + other fragments which
   d. form teflon-like wall coat protecting against off-axis F, F –
   e. repeat (a – d) every 10 – 15 seconds



2. At ~620ºC, ~0.46 Torr, SiH4 gas molecules bounce off the walls many times before they stick, mostly entering and leaving the hole. When they stick, it can be anywhere, so they form a conformal polysilicon coat as the H leaves and the silicon migrates to a lattice site.

3. Gasses such as B2O3, B2H6 (diborane), P2O5, and PH3 (phosphine) can also be deposited in a conformal layer, and make p+ and n+ doped polysilicon.

4. Heating drives the dopants into the single crystal silicon, forming p–n junctions and ohmic contacts there. Large E drift fields can end before the poly, removing that source of large leakage currents.

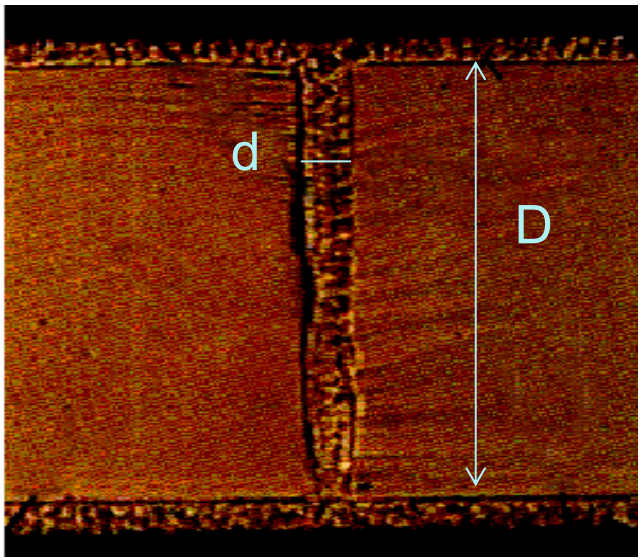
5. Active edges are made from trench electrodes, capped with an oxide coat. Plasma dicing up to the oxide etch stop makes precise edges.

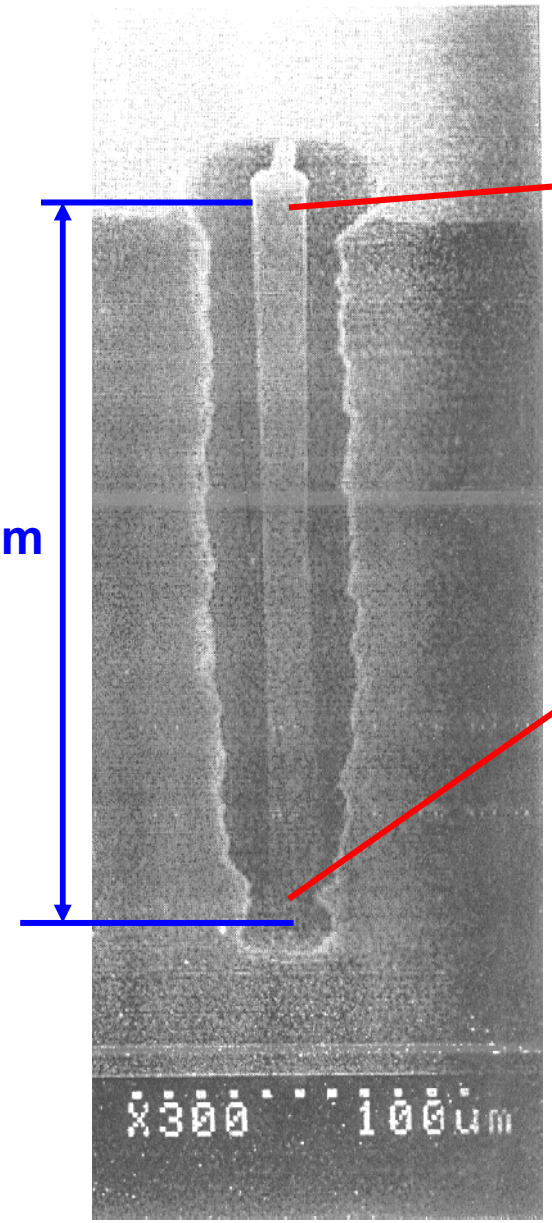
3Dc

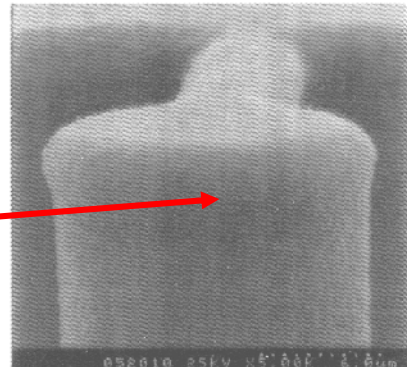
Examples of etching and coating with polysilicon.

An early test structure by Julie Segal, etched and coated (middle, right), showing conformal nature of poly coat.

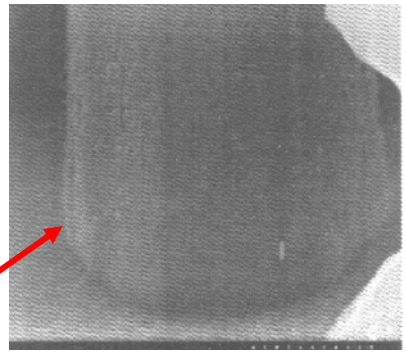
An electrode hole, filled, broken (accidentally) in a plane through the axis, showing grain structure (below). The surface poly is later etched off.



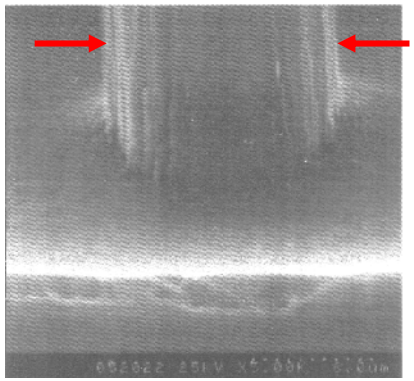




coated, top



coated, bottom



uncoated

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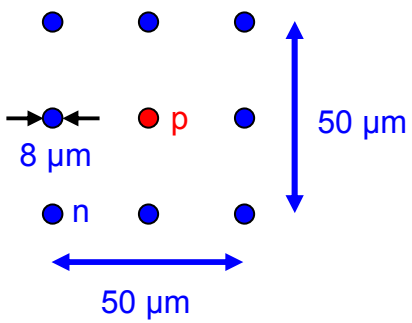
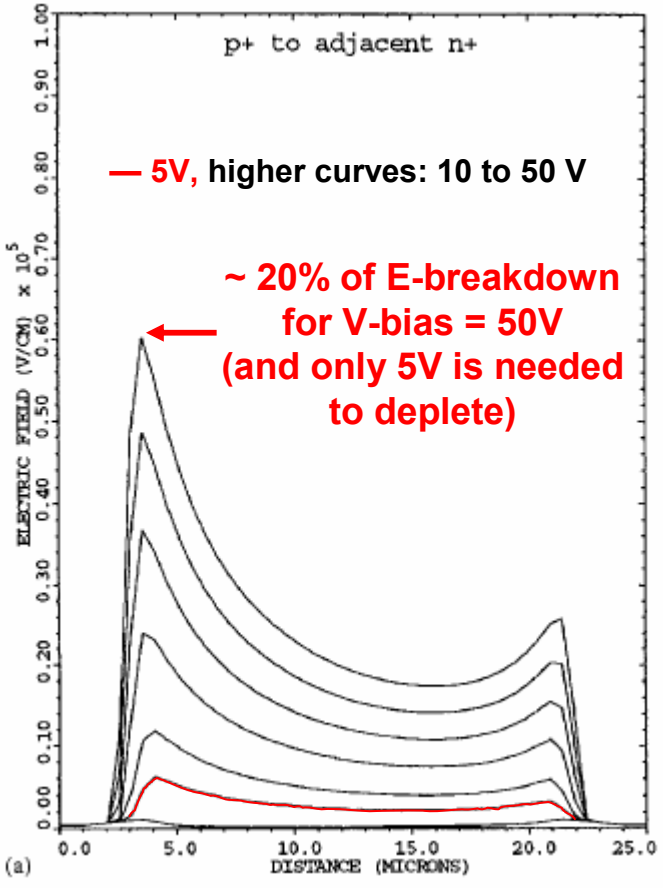
Potential 3D features from preliminary calculations:

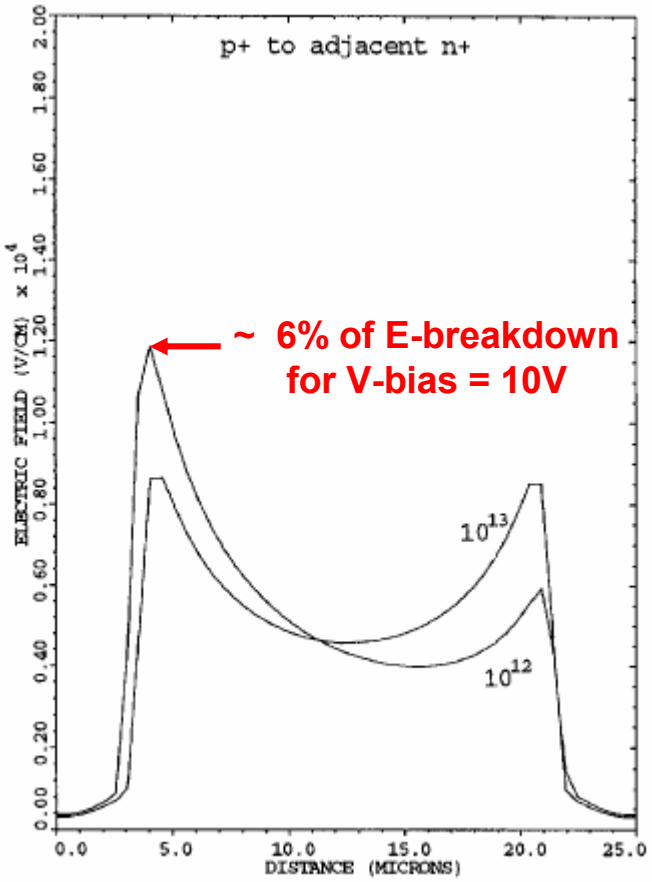


Structure used in calculations.

Fabricated ones have electrode diameters ~50% larger; cell sizes ~2× larger, and have rows of alternate n and p electrodes.



1. Low depletion voltages and peak fields.



2. Peak fields do not become excessive with large radiation-induced bulk damage.

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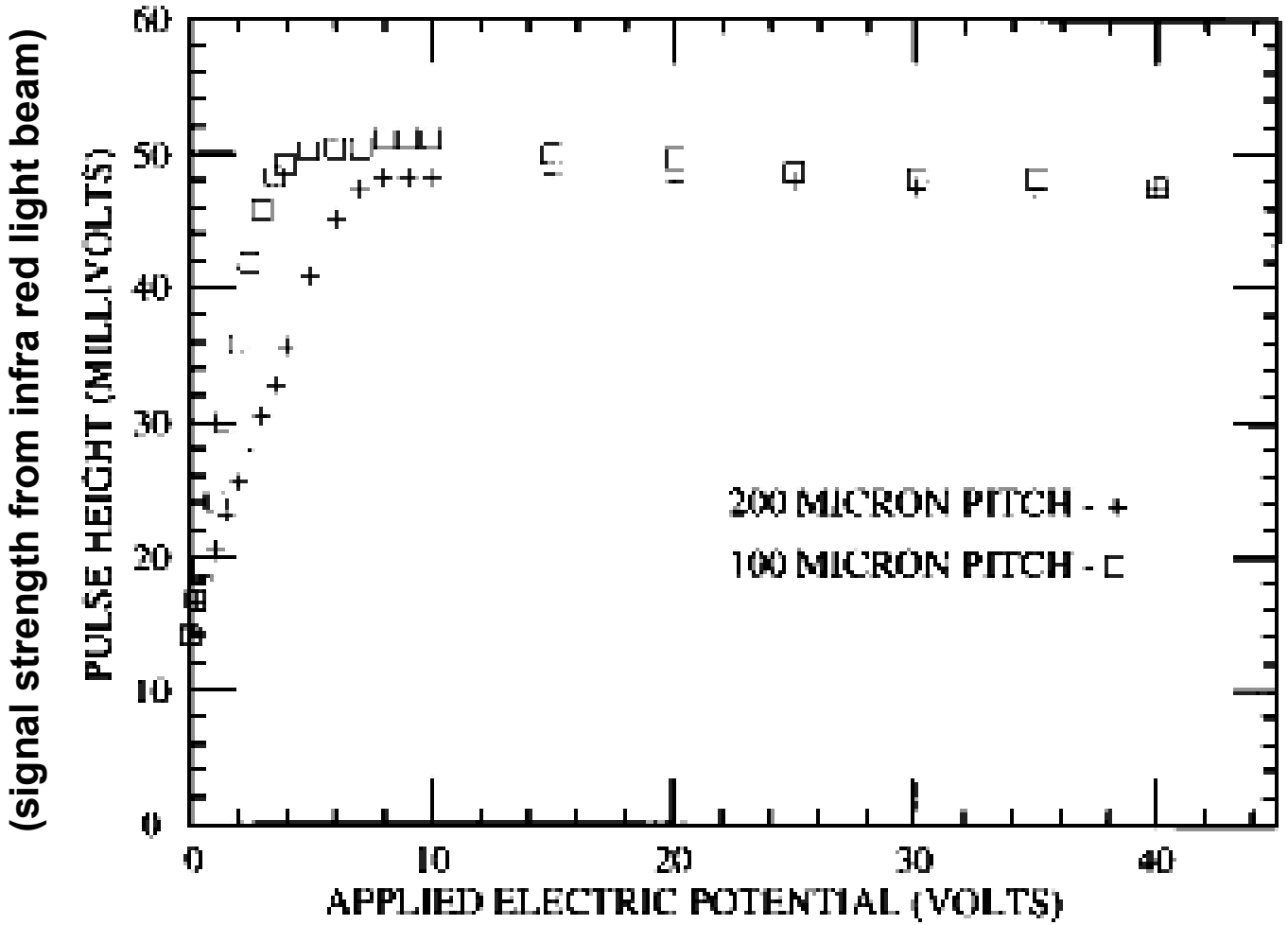
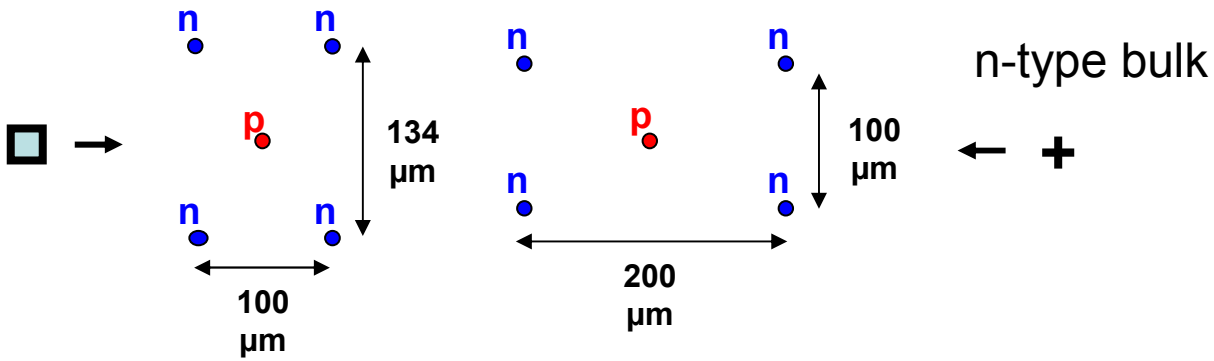

(signal strength from infra red light beam)
PULSE HEIGHT (MILLIVOLTS)
APPLIED ELECTRIC POTENTIAL (VOLTS)
200 MICRON PITCH - +
100 MICRON PITCH - □
0
10
20
30
40
50
60


n
p
134 µm
100 µm
200 µm
100 µm
n-type bulk
+

3Dc

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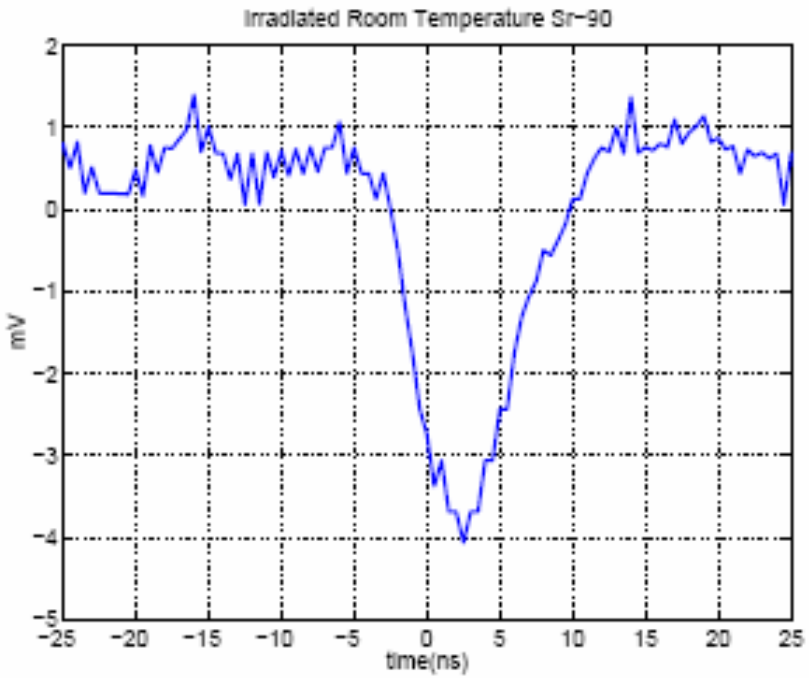
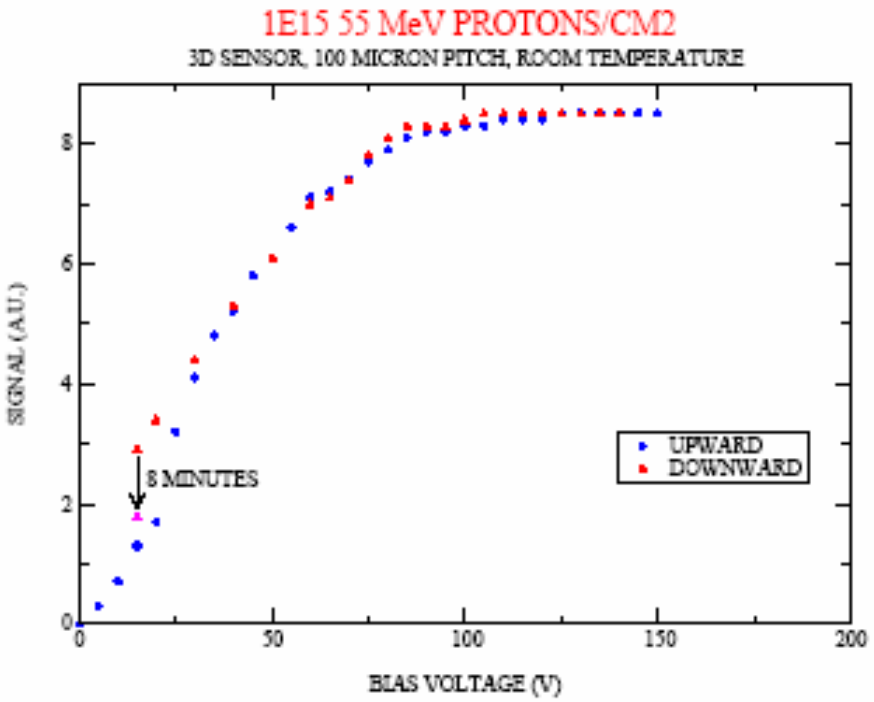
3D performance after irradiation



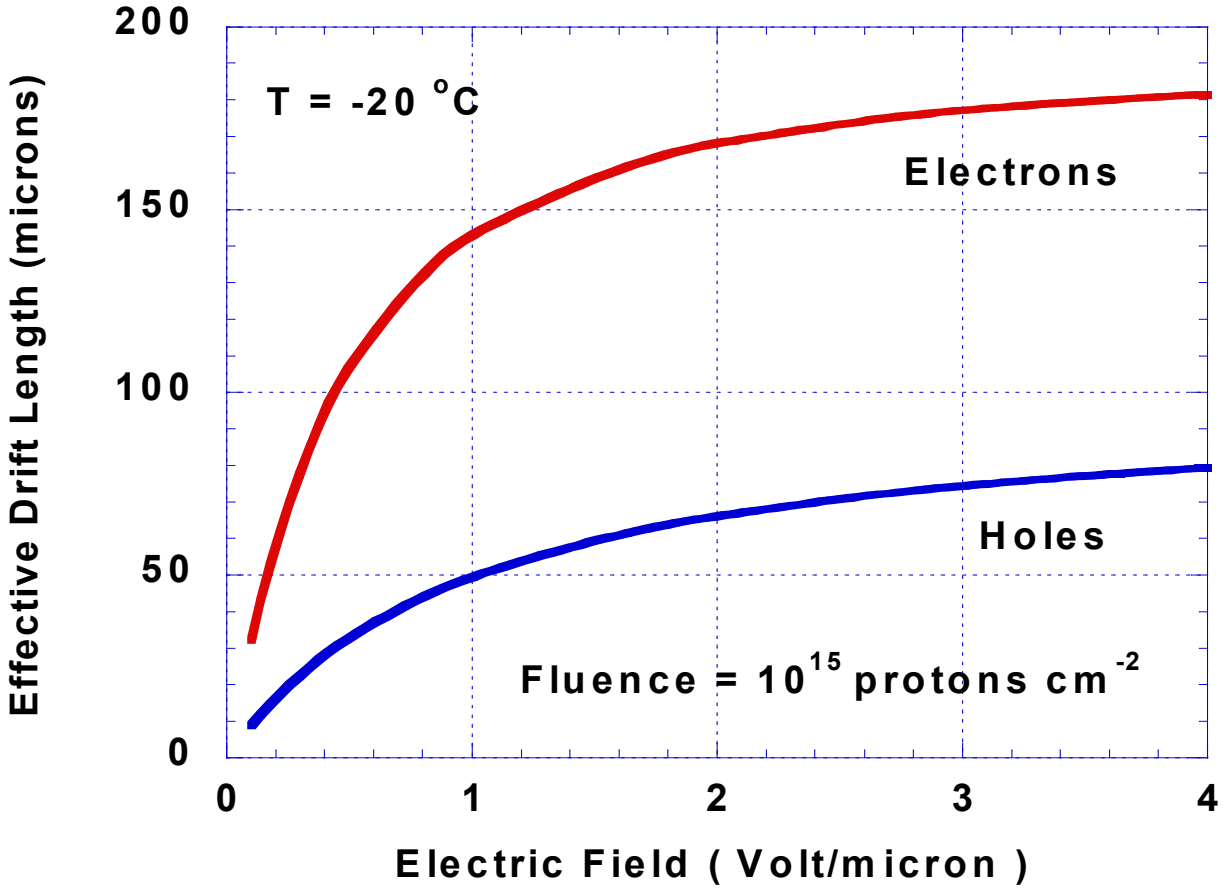
90-Sr β signal in 3D sensor irradiated by 10e15 SPS protons / sq cm, fully reverse annealed, no implanted oxygen, room temperature.

Both sensors 181 μm thick, 100 μm × 134 μm cells, joined in rows for readout.



IR μbeam signal vs. V-bias, 3D sensor 10e15 55 MeV protons / sq. cm ≈ 1.8 10e15 1 MeV neutrons. Measured at room temp. Stored at low temp. No beneficial or reverse annealing, no oxygen.

3Dc



(Nucl. Instr. and Meth. A 509 (2003) 86 – 91)

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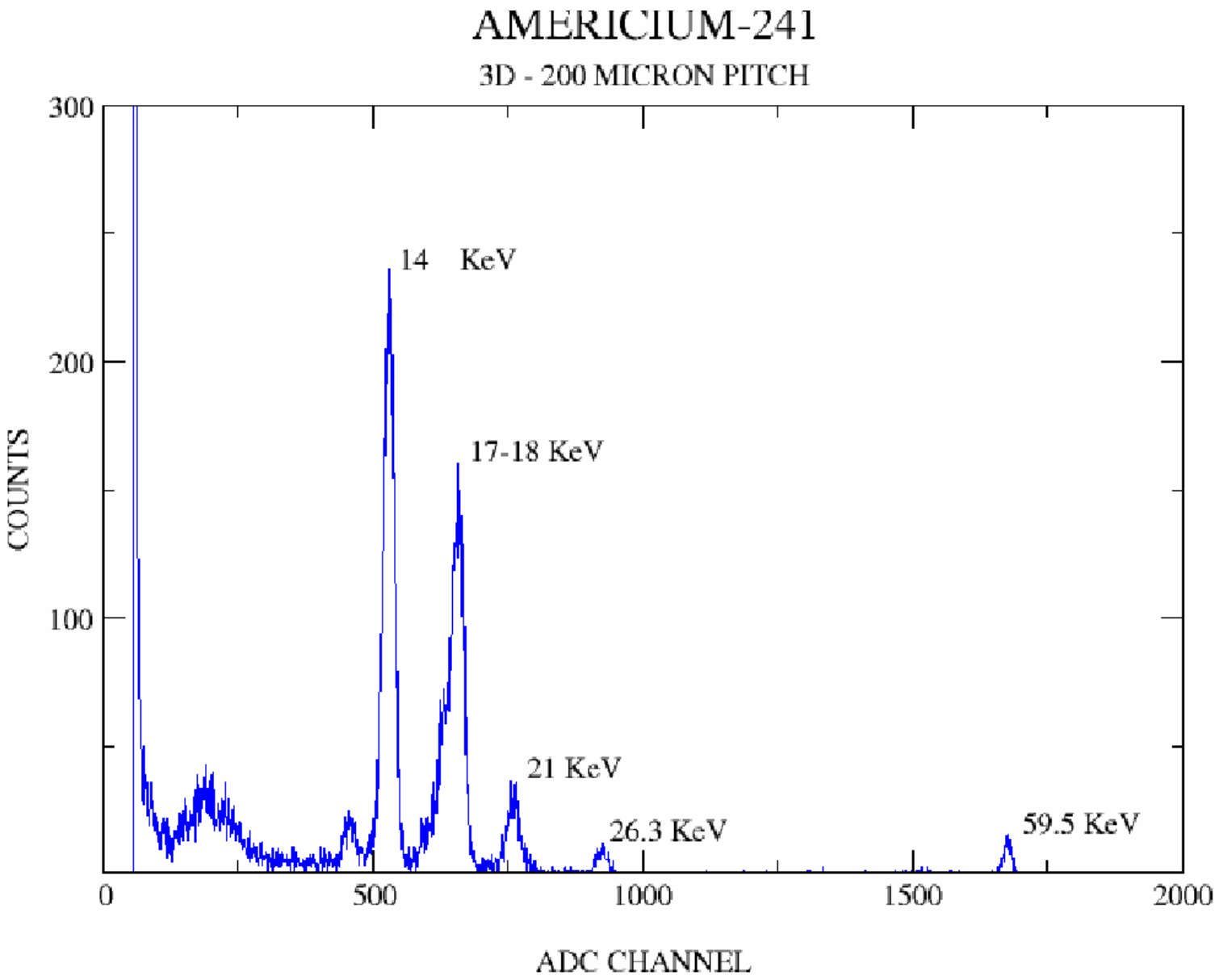
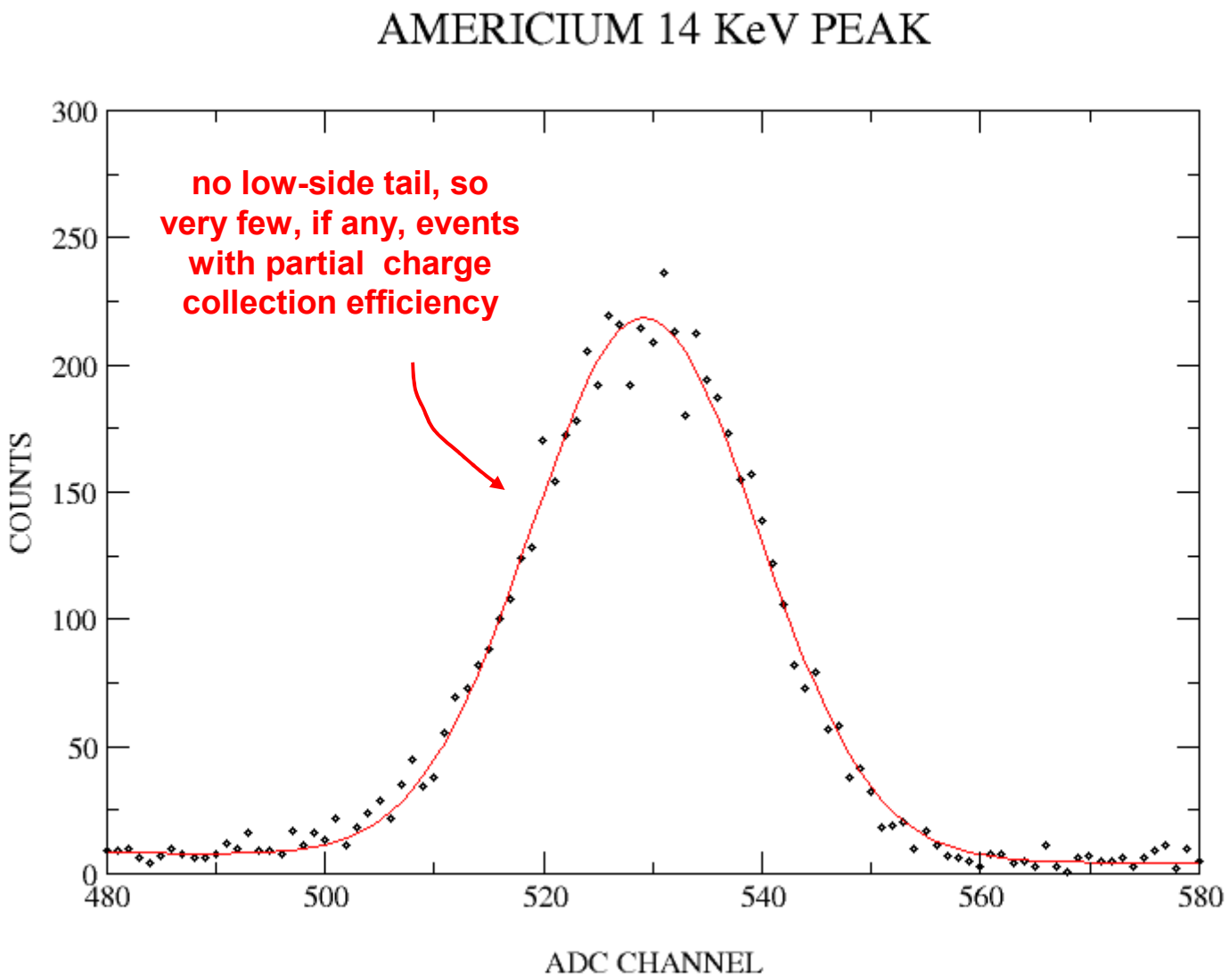
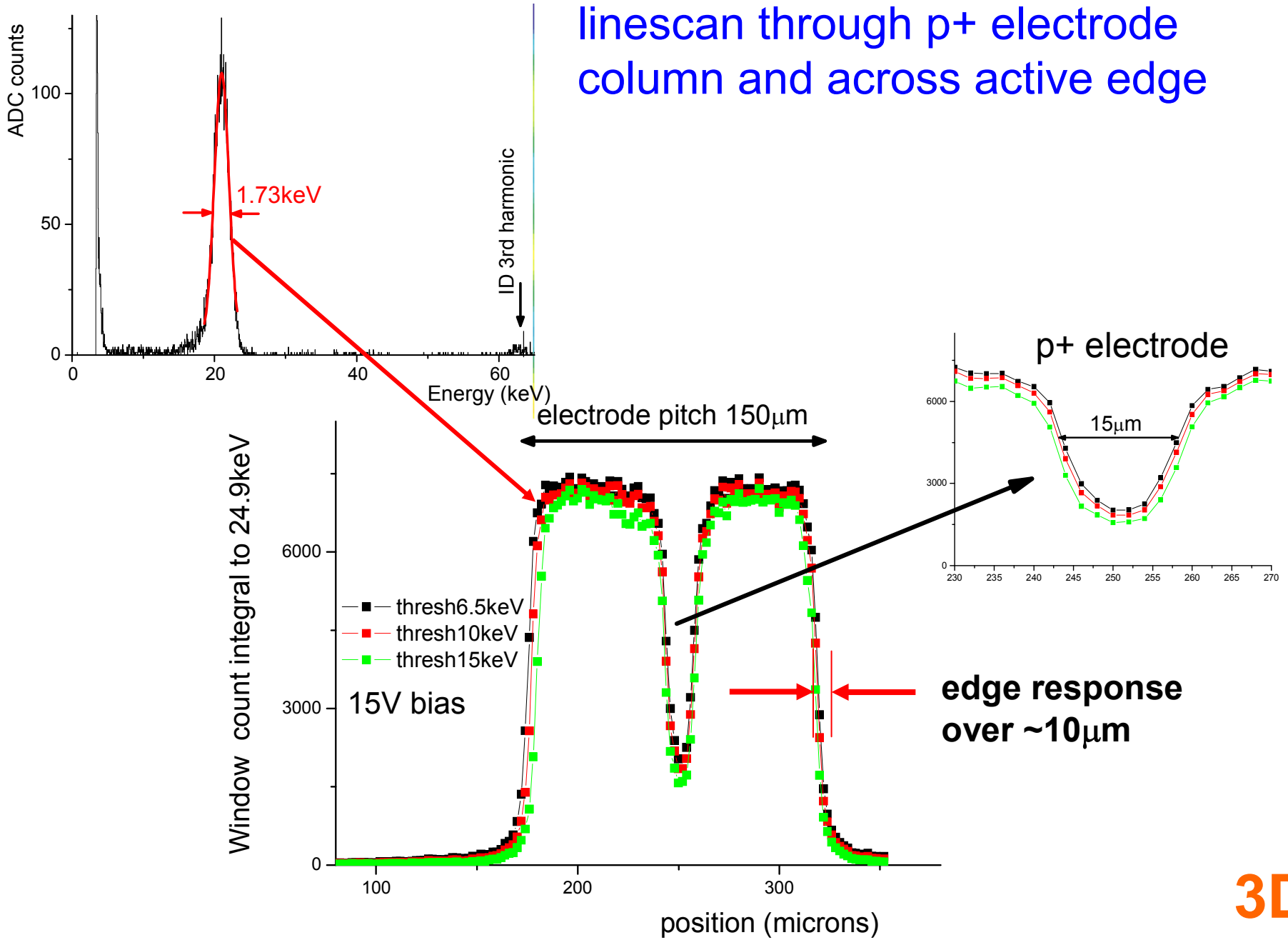

AMERICIUM-241
3D - 200 MICRON PITCH
300
200
100
COUNTS
14 KeV
17-18 KeV
21 KeV
26.3 KeV
59.5 KeV
0
500
1000
1500
2000
ADC CHANNEL

3Dc


AMERICIUM 14 KeV PEAK
no low-side tail, so
very few, if any, events
with partial charge
collection efficiency
COUNTS
ADC CHANNEL
0
50
100
150
200
250
300
480
500
520
540
560
580

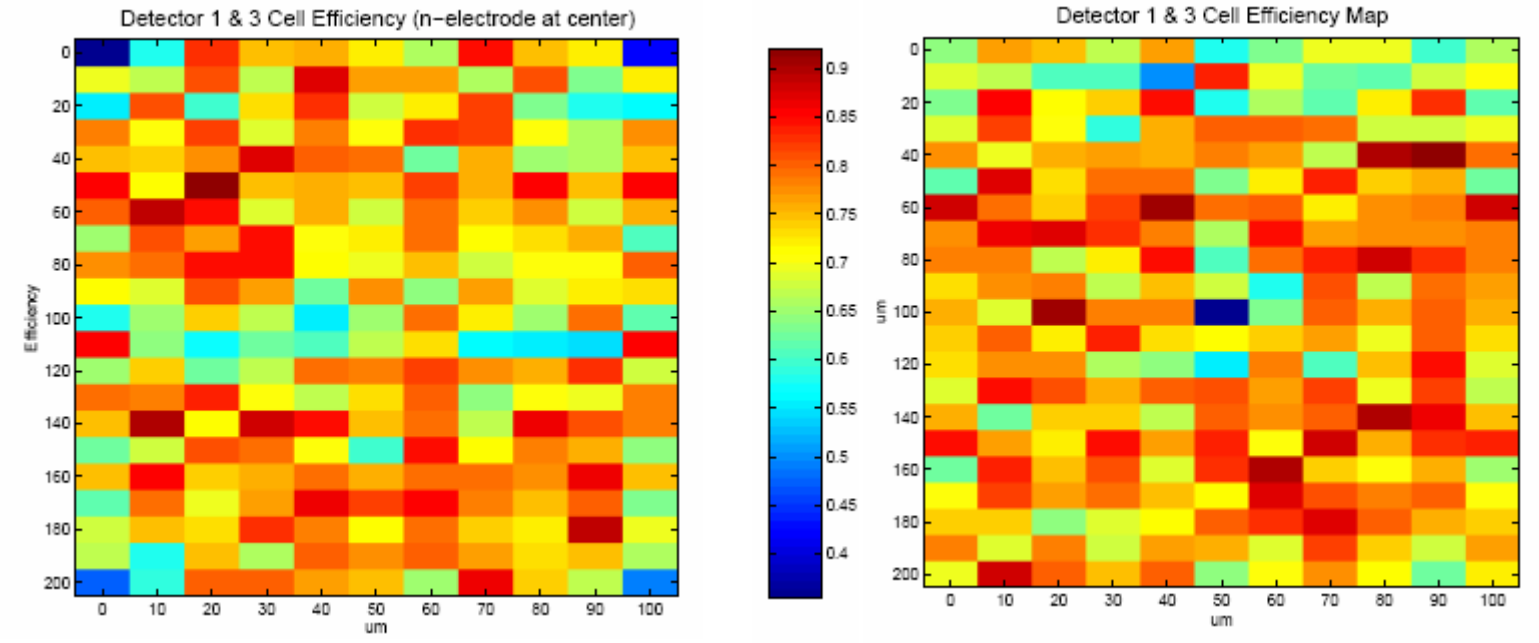
3Dc

linescan through p+ electrode column and across active edge



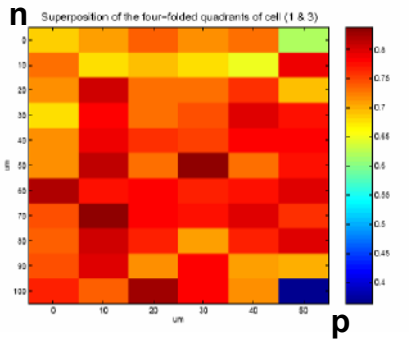
3Dc

X5 (Totem) beam test – cell uniformity measurements



Observed 3D hits / predicted telescope hits as a function of position within the 100 µm x 200 µm non-edge cells. To improve statistics, the hits for all cells are superimposed.
(Note: 3D discriminator thresholds can magnify the true collection efficiency differences.)

Left above: grid with p electrodes on corners.



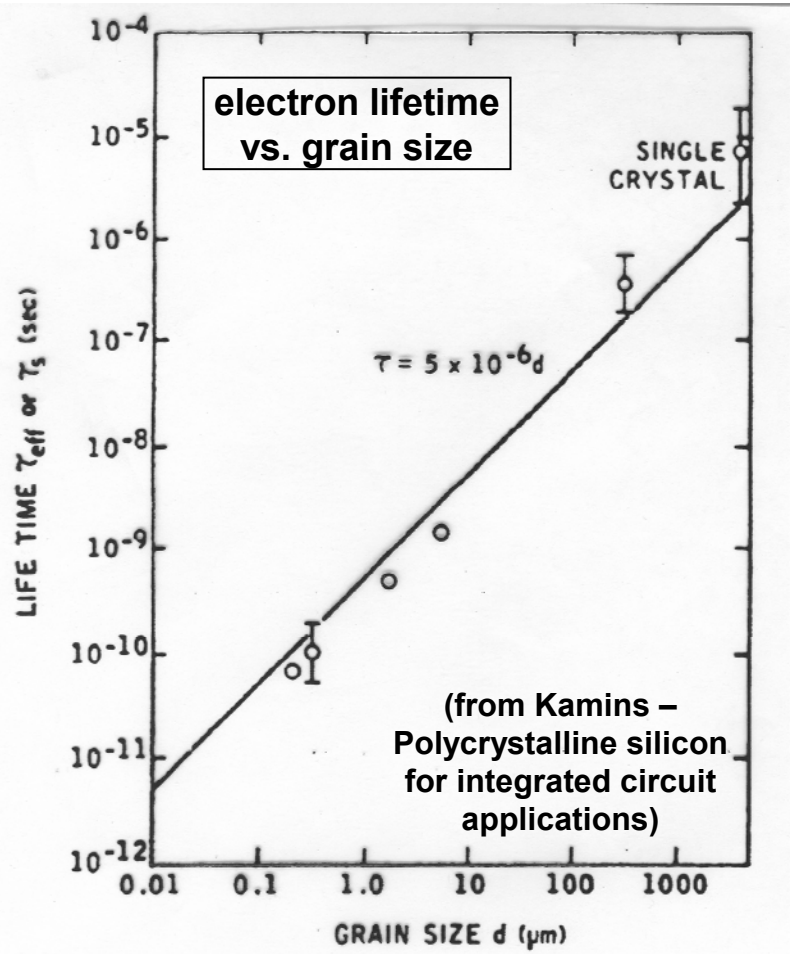
Right above: grid with p electrodes in center.

Center: data is further projected onto one quadrant. Null-field points are at upper right and lower left. n^{--} bulk and n^{+} active edges.

3Dc

Some possible sources of the observed differences in collection efficiencies seen from n and p electrodes:

1. Differences in electrode diameters and thermal history (increased Dt increases dopant diffusion distances and radius of built-in fields, and can increase grain sizes – the N electrodes were done first).
2. The dopant gasses available at SNF produce an oxide layer on the hole surface which remains after the hole is filled; they may differ in radii and effectiveness as barriers.
3. Electrons and holes have different diffusion rates and lifetimes in the poly electrodes.
4. Note: The CERN -- X5 beam test data shows counts, not signal heights, and discrimination levels will affect the results.



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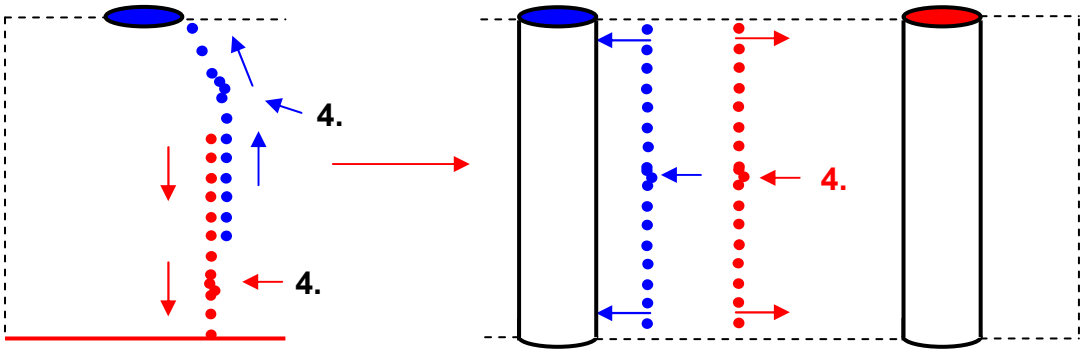
Speed: planar → 3D



1. 3D lateral cell size can be smaller than wafer thickness, so → 1. shorter collection distance

2. in 3D, field lines end on cylinders rather than on circles, so → 2. higher average fields for any given maximum field (price: larger electrode capacitance)

3. most of the signal is induced when the charge is close to the electrode, where the electrode solid angle is large, so planar signals are spread out in time as the charge arrives, and → 3. 3D signals are concentrated in time as the track arrives

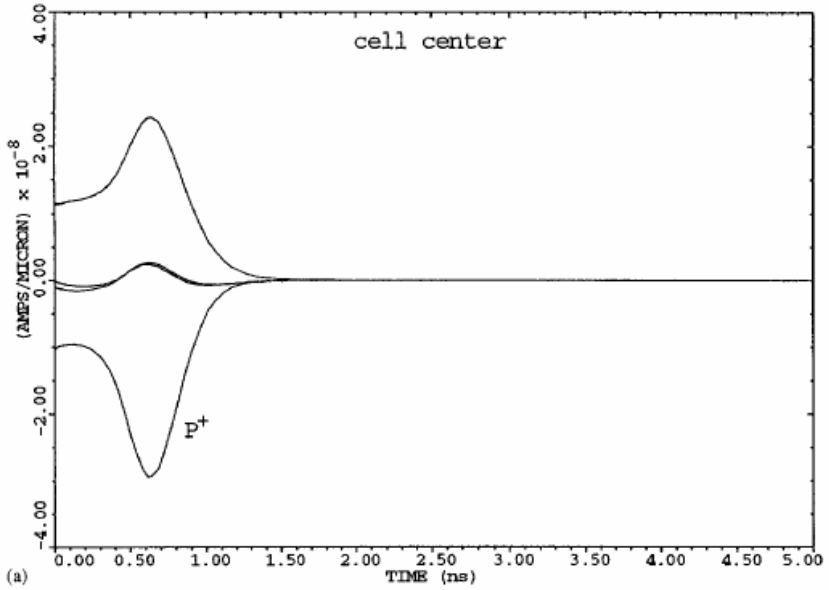
4. Landau fluctuations along track arrive sequentially and may cause secondary peaks (see next slide) → 4. Landau fluctuations arrive nearly simultaneously

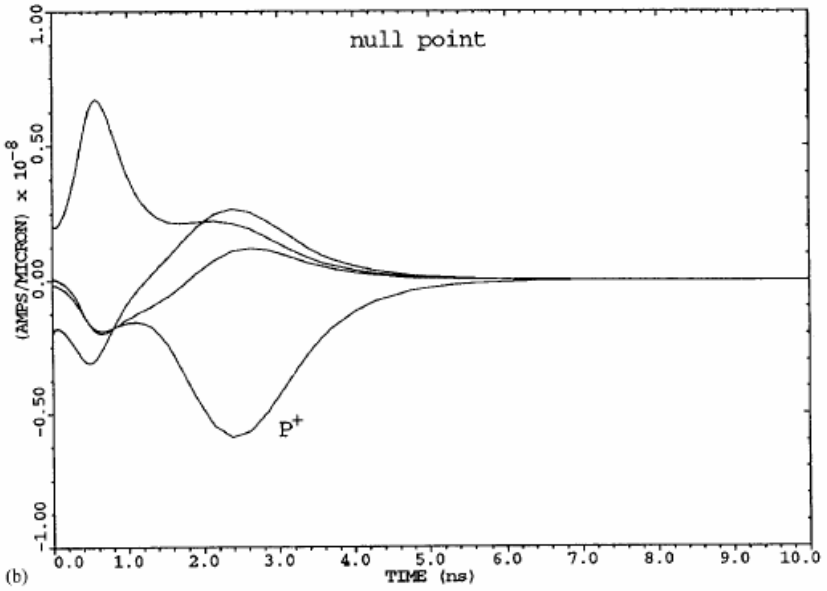
5. if readout has inputs from both n+ and p+ electrodes, → 5. drift time corrections can be made

6. for long, narrow pixels and fast electronics, → 6. track locations within the pixel can be found

3Dc

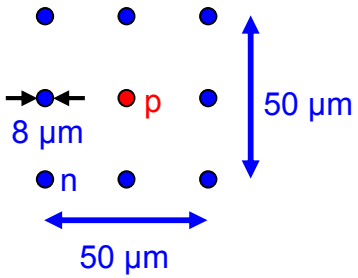
Potential 3D features from preliminary calculations:





1 ns

3 ns



3. Fast pulses. Current to the p electrode and the other 3 n electrodes.

(The track is parallel to the electrodes through a cell center and a null point. V – bias = 10V. Cell centers are in center of any quadrant. Null points are located between pairs of n electrodes.)

3Dc

0.13 µm chips now fabricated – rise, fall times expected to be ≈ 1.5 ns

A high-speed low-noise transimpedance amplifier in a 0.25 µm CMOS technology

Giovanni Anelli[a,*], Kurt Borer[b], Luca Casagrande[a], Matthieu Despeisse[a], Pierre Jarron[a], Nicolas Pelloux[a], Shahyar Saramad[a,c]

rise times ≈ 3.5 ns **fall times ≈ 3.5 ns**

[a] *CERN, EP Division, CH-1211 Geneva 23, Switzerland*

[b] *University of Bern, Laboratory for High Energy Physics, Sidlerstr. 5, CH-3012 Bern, Switzerland*

[c] *Institute for Studies in Theoretical Physics and Mathematics (IPM), Tehran, Iran, P.O. Box 19395-5531*

Elsevier use only: Received date here; revised date here; accepted date here

Abstract

Resistive (transistor channel) feedback, and so a current amplifier.

We present the simulated and measured performance of a transimpedance amplifier designed in a quarter micron CMOS process. Containing only NMOS and PMOS devices, this amplifier can be integrated in any submicron CMOS process. The main feature of this design is that a transistor in the feedback path substitutes the transresistance. The circuit has been optimized for reading signals coming from silicon strip detectors with few pF input capacitance. For an input charge of 4 fC, an input capacitance of 4 pF and a transresistance of 135 kΩ, we have measured an output pulse fall time of 3 ns and an Equivalent Noise Charge (ENC) of around 350 electrons rms. In view of a utilization of the chip at cryogenic temperatures, measurements at 130 K have also been carried out, showing an overall improvement in the performance of the chip. Fall times down to 1.5 ns have been measured. An integrated circuit containing 32 channels has been designed and wire-bonded to a silicon strip detector and successfully used for the construction of a high-intensity proton beam hodoscope for the NA60 experiment. The chip has been laid out using special techniques to improve its radiation tolerance, and it has been irradiated up to 10 Mrd (SiO_2) without showing any degradation in the performance.

Keywords: Deep submicron; CMOS; Transimpedance amplifier; Radiation tolerance; Low temperature CMOS

3Dc

planar sensor pulse shape

Nuclear Instruments and Methods in Physics Research A310 (1991) 189–191
North-Holland

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

Electrostatic simulations for the design of silicon strip detectors and front-end electronics

R. Sonnenblick, N. Cartiglia, B. Hubbard, J. Leslie, H.F.-W. Sadrozinski and T. Schalk
Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA 95064, USA

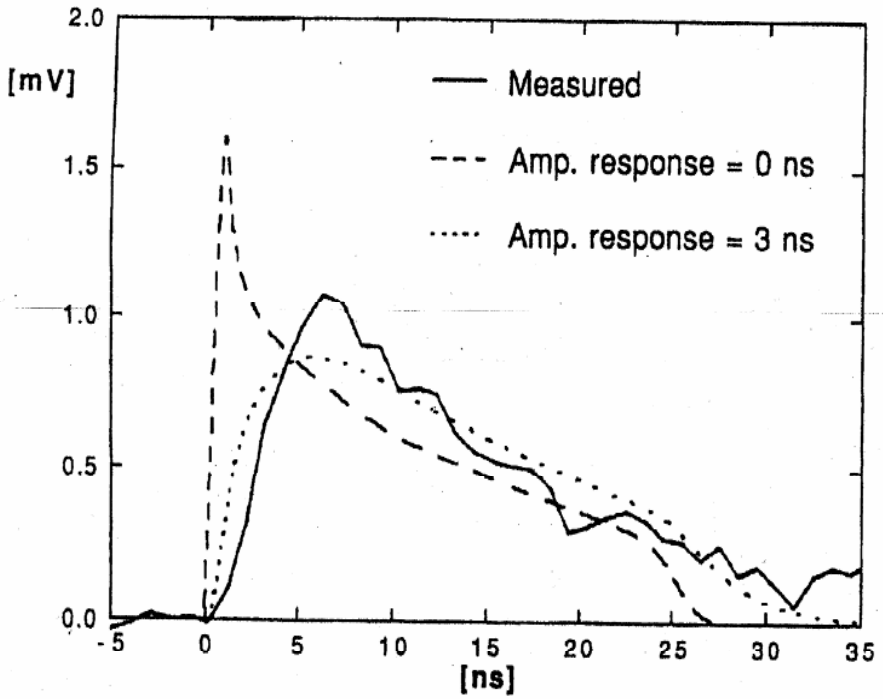
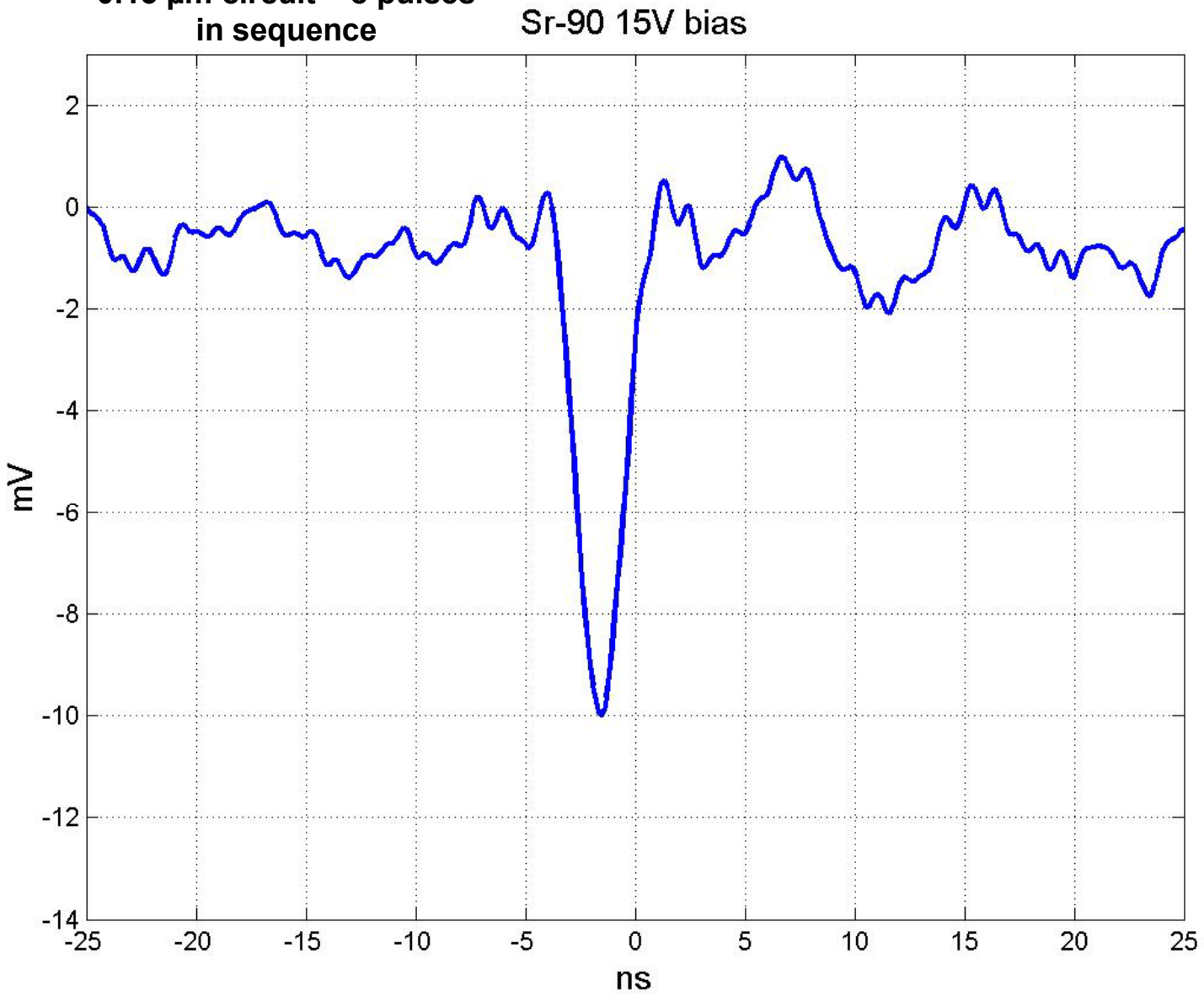


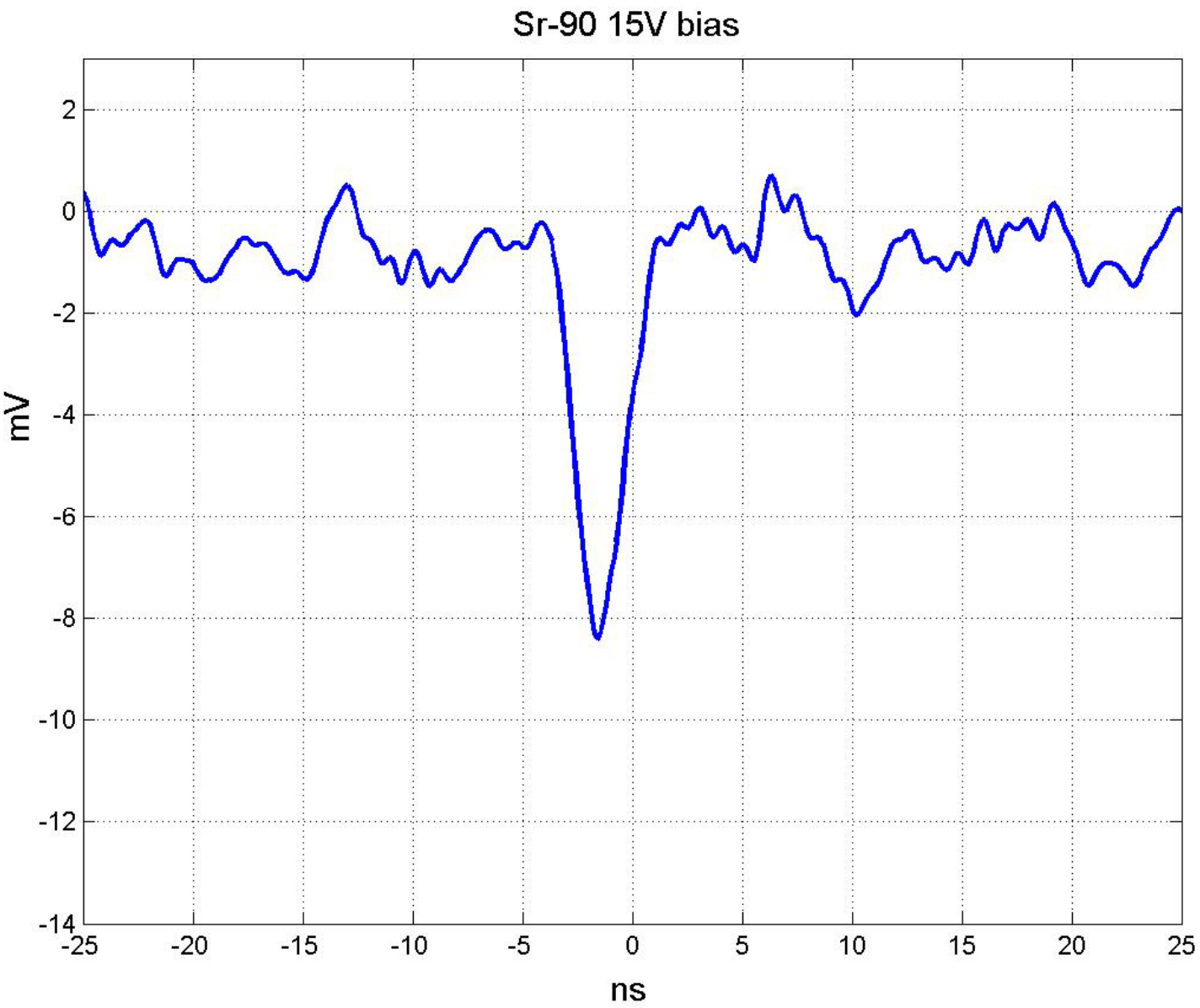
Fig. 3. Pulse shape at the junction side from a minimum ionizing particle. The three curves are the simulated current (with initial diffusion), the simulated current convoluted with the preamplifier response, and a typical observed pulse, respectively.

3Dc

0.13 µm circuit – 8 pulses in sequence



3Dc



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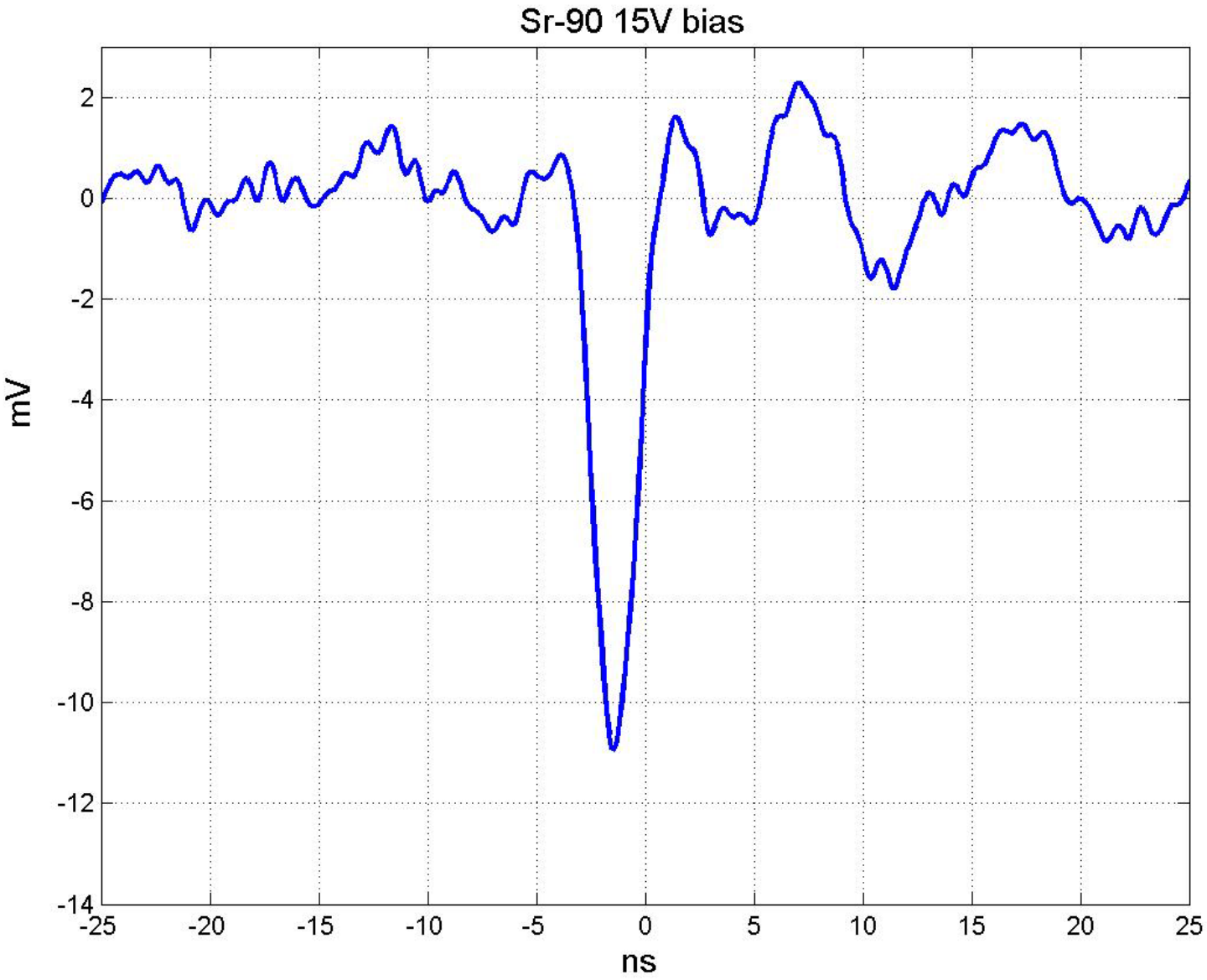
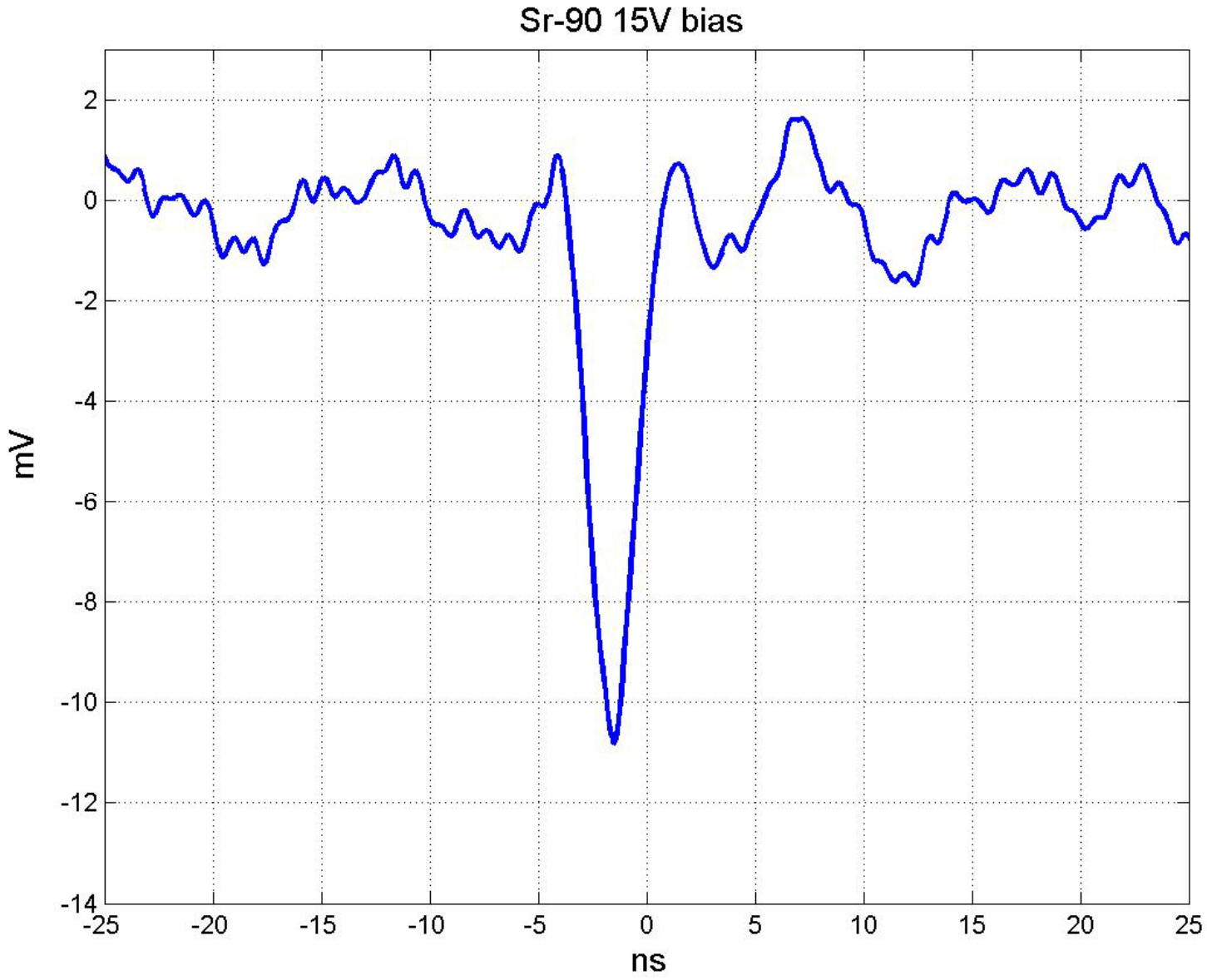
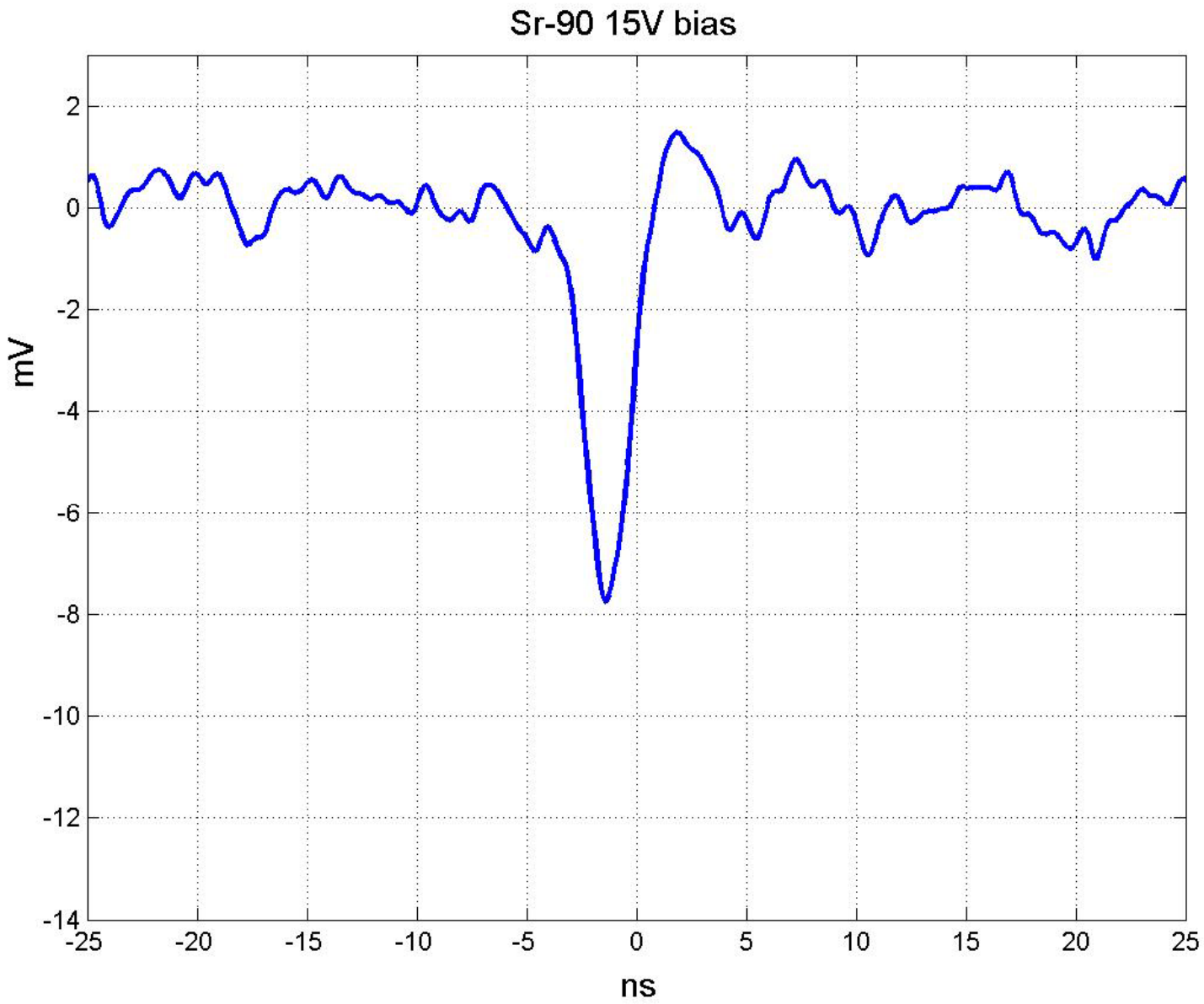


3Dc



3Dc



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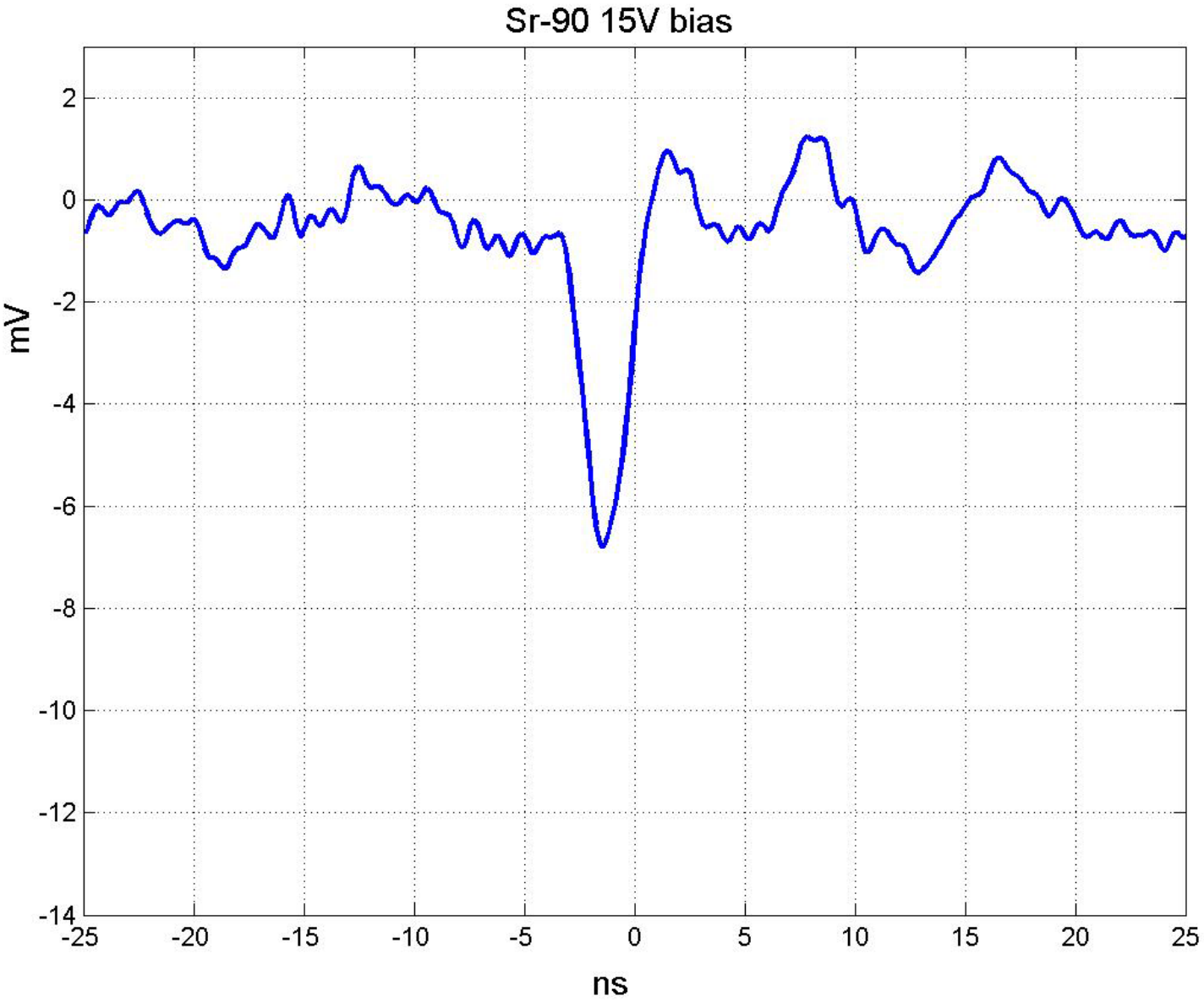

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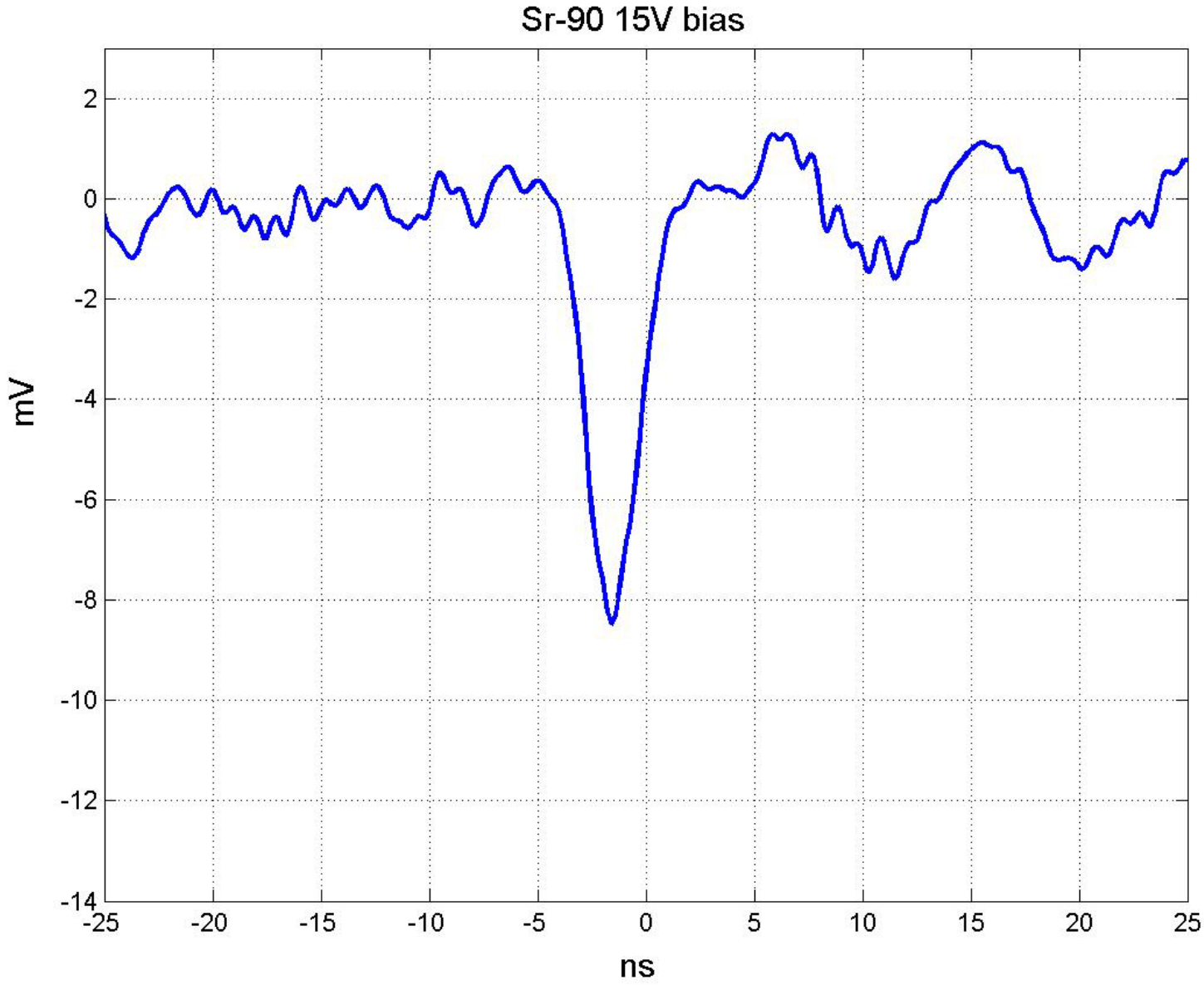

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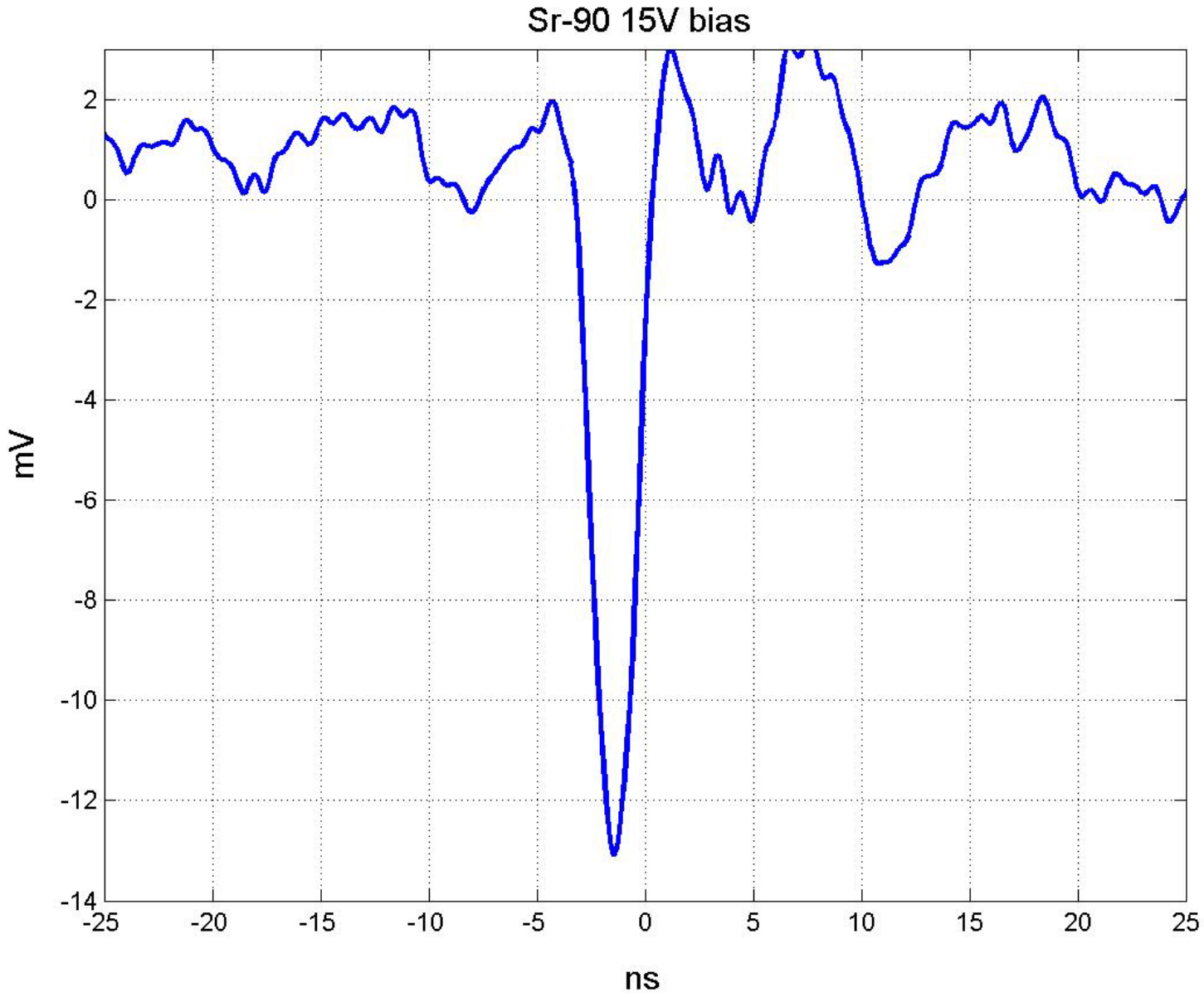
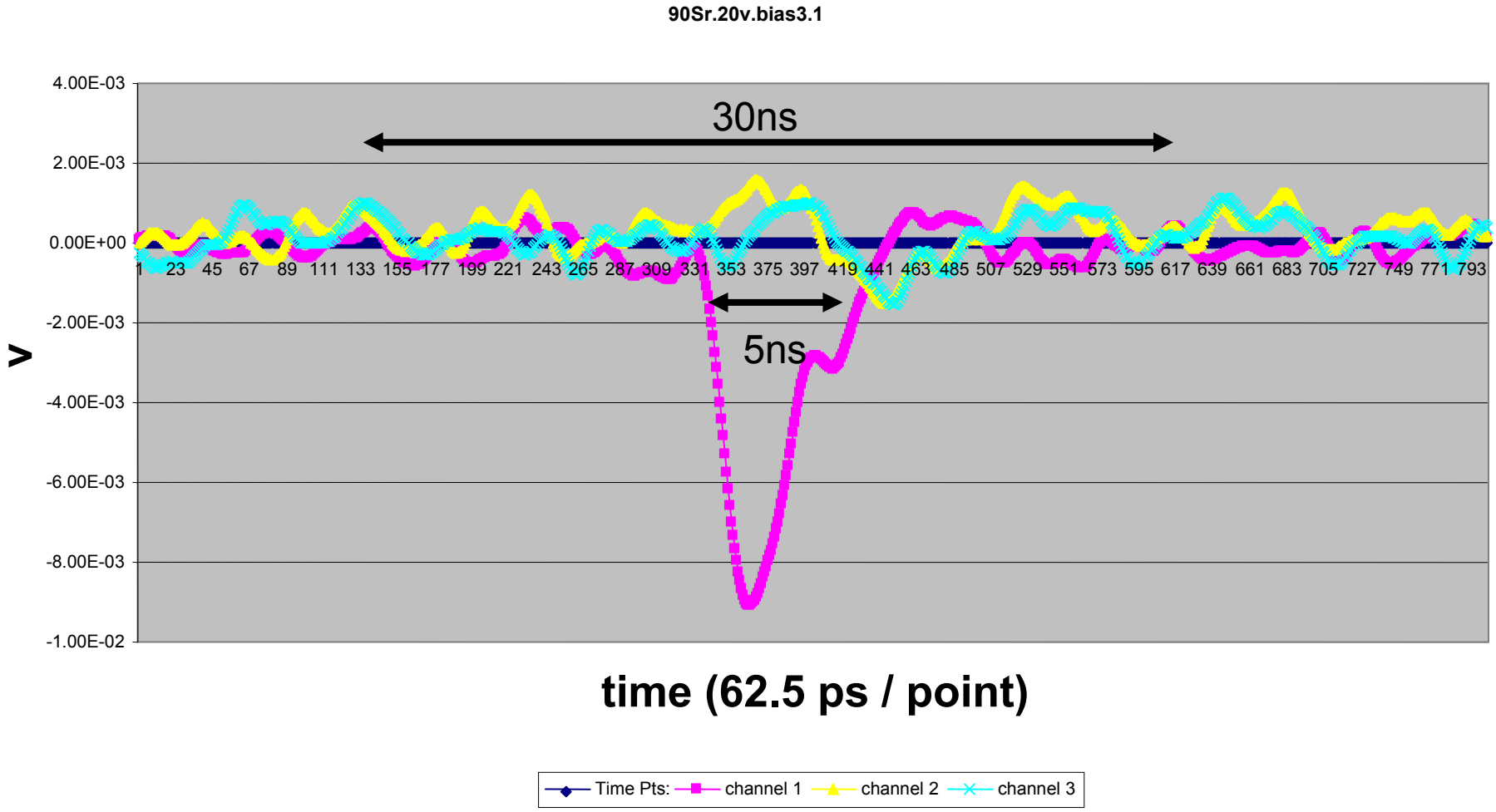


3Dc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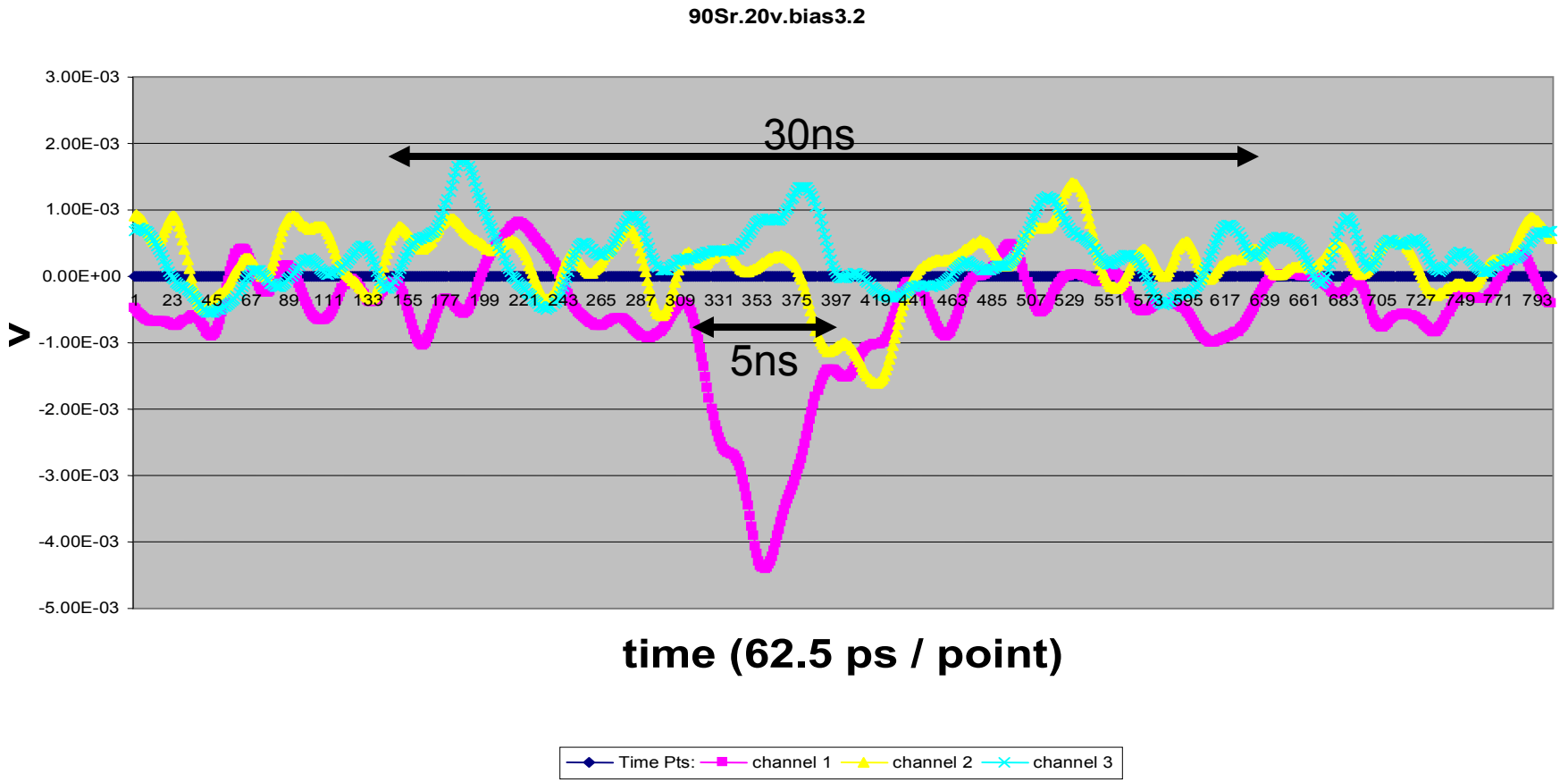
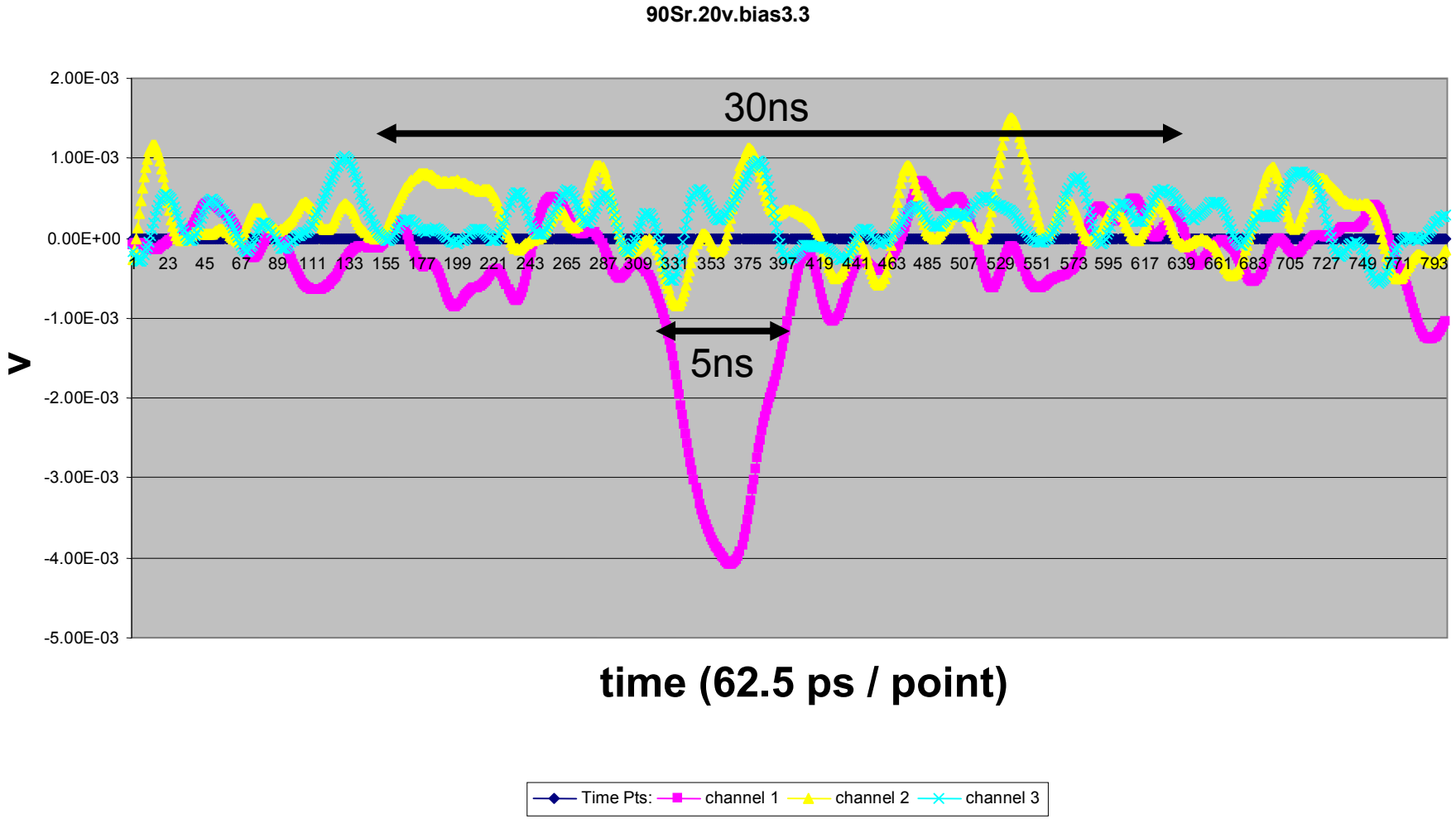
2.00E-03
0.00E+00
-2.00E-03
-4.00E-03
-6.00E-03
-8.00E-03
-1.00E-02
V
30ns
5ns
1 23 45 67 89 111 133 155 177 199 221 243 265 287 309 331 353 375 397 419 441 463 485 507 529 551 573 595 617 639 661 683 705 727 749 771 793
time (62.5 ps / point)
Time Pts:
channel 1
channel 2
channel 3

3Dc


90Sr.20v.bias3.2
3.00E-03
2.00E-03
1.00E-03
0.00E+00
-1.00E-03
-2.00E-03
-3.00E-03
-4.00E-03
-5.00E-03
V
30ns
5ns
1 23 45 67 89 111 133 155 177 199 221 243 265 287 309 331 353 375 397 419 441 463 485 507 529 551 573 595 617 639 661 683 705 727 749 771 793
time (62.5 ps / point)
Time Pts:
channel 1
channel 2
channel 3

3Dc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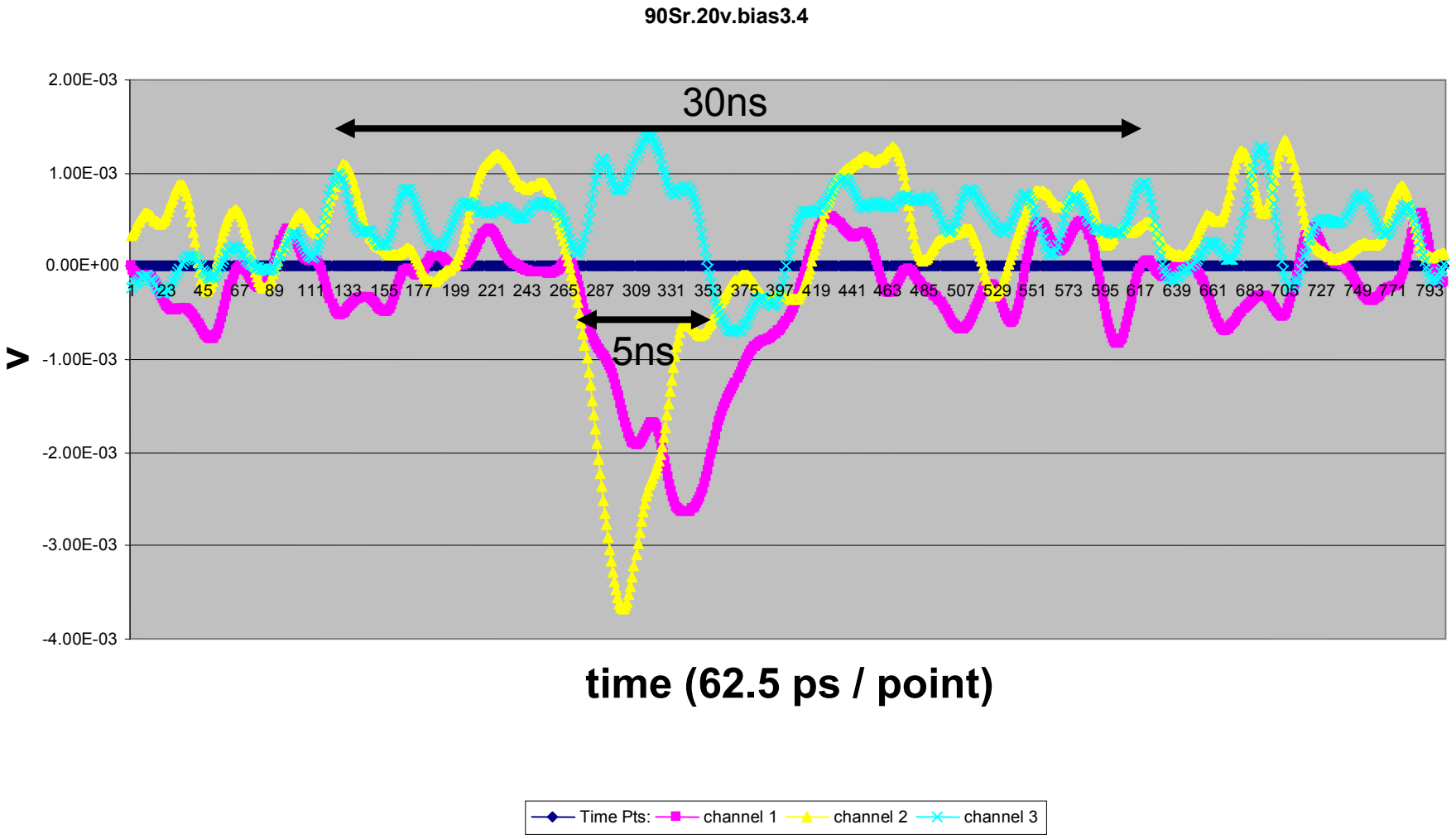
1.00E-03
0.00E+00
-1.00E-03
-2.00E-03
-3.00E-03
-4.00E-03
-5.00E-03
V
30ns
5ns
1 23 45 67 89 111 133 155 177 199 221 243 265 287 309 331 353 375 397 419 441 463 485 507 529 551 573 595 617 639 661 683 705 727 749 771 793
time (62.5 ps / point)
Time Pts:
channel 1
channel 2
channel 3

3Dc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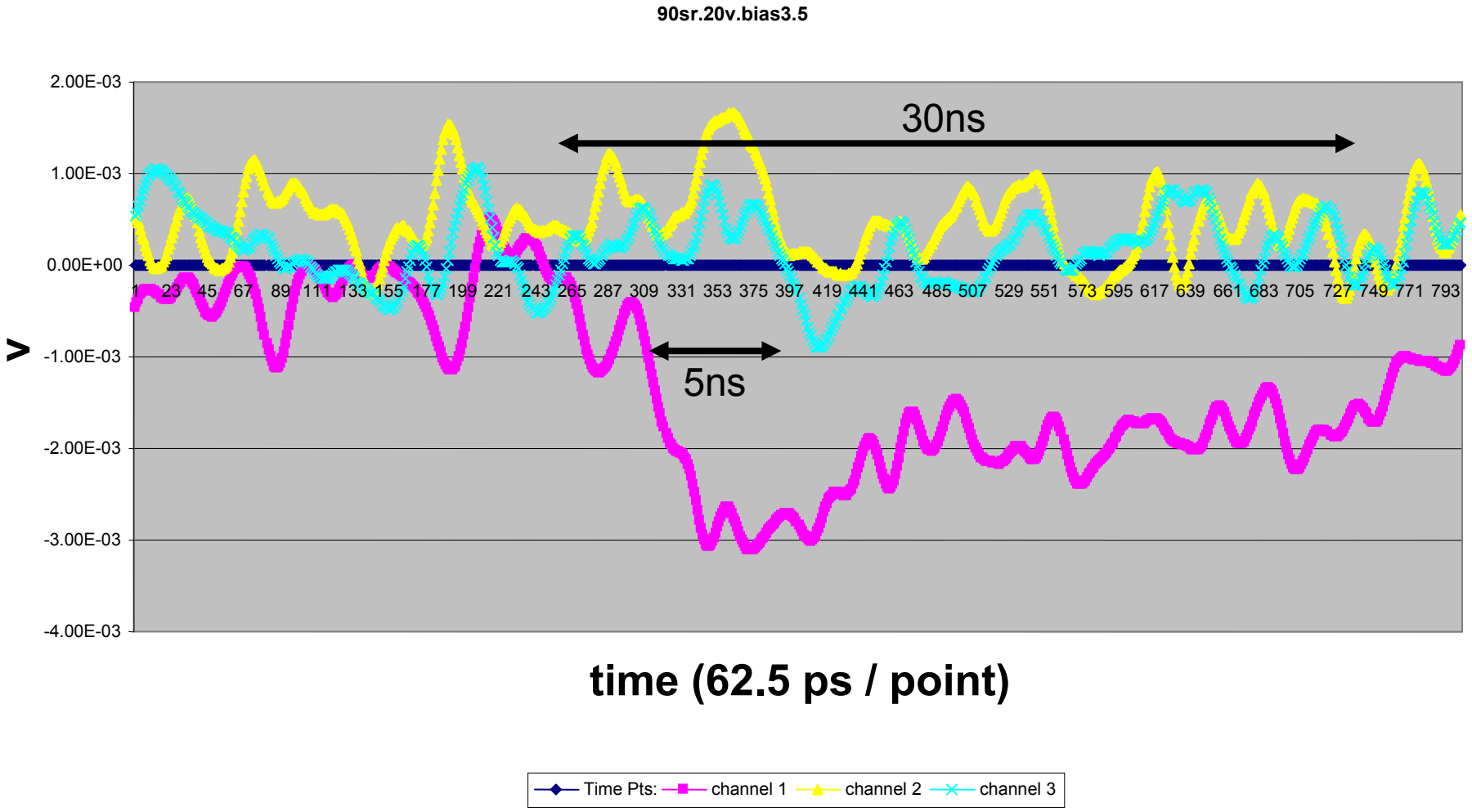
1.00E-03
0.00E+00
-1.00E-03
-2.00E-03
-3.00E-03
-4.00E-03
V
30ns
5ns
1 23 45 67 89 111 133 155 177 199 221 243 265 287 309 331 353 375 397 419 441 463 485 507 529 551 573 595 617 639 661 683 705 727 749 771 793
time (62.5 ps / point)
Time Pts:
channel 1
channel 2
channel 3

3Dc


90sr.20v.bias3.5
2.00E-03
1.00E-03
0.00E+00
-1.00E-03
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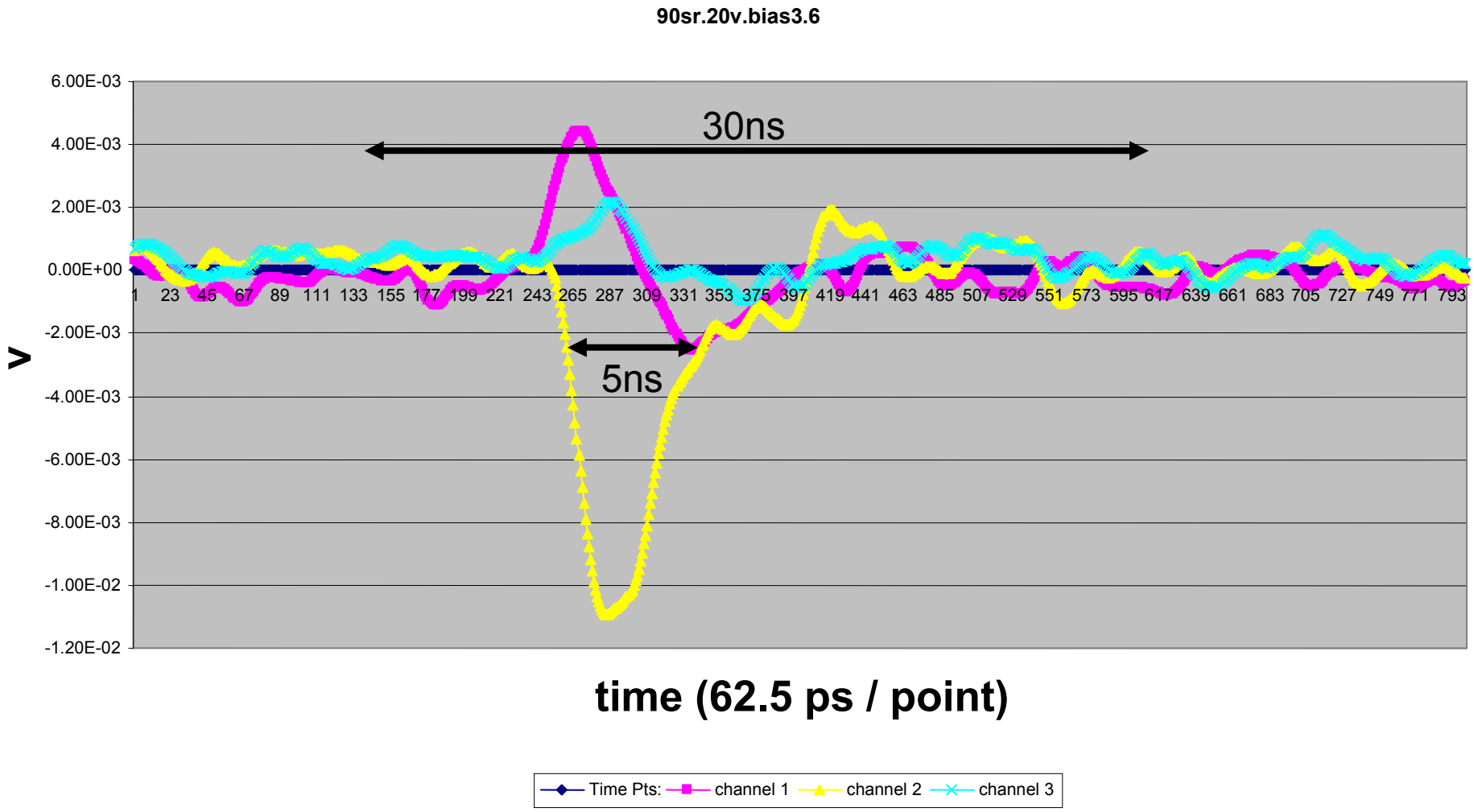
-3.00E-03
-4.00E-03
V
30ns
5ns
1 23 45 67 89 111 133 155 177 199 221 243 265 287 309 331 353 375 397 419 441 463 485 507 529 551 573 595 617 639 661 683 705 727 749 771 793
time (62.5 ps / point)
Time Pts:
channel 1
channel 2
channel 3

3Dc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6.00E-03
4.00E-03
2.00E-03
0.00E+00
-2.00E-03
-4.00E-03
-6.00E-03
-8.00E-03
-1.00E-02
-1.20E-02
V
1 23 45 67 89 111 133 155 177 199 221 243 265 287 309 331 353 375 397 419 441 463 485 507 529 551 573 595 617 639 661 683 705 727 749 771 793
30ns
5ns
time (62.5 ps / point)
Time Pts:
channel 1
channel 2
channel 3

3Dc

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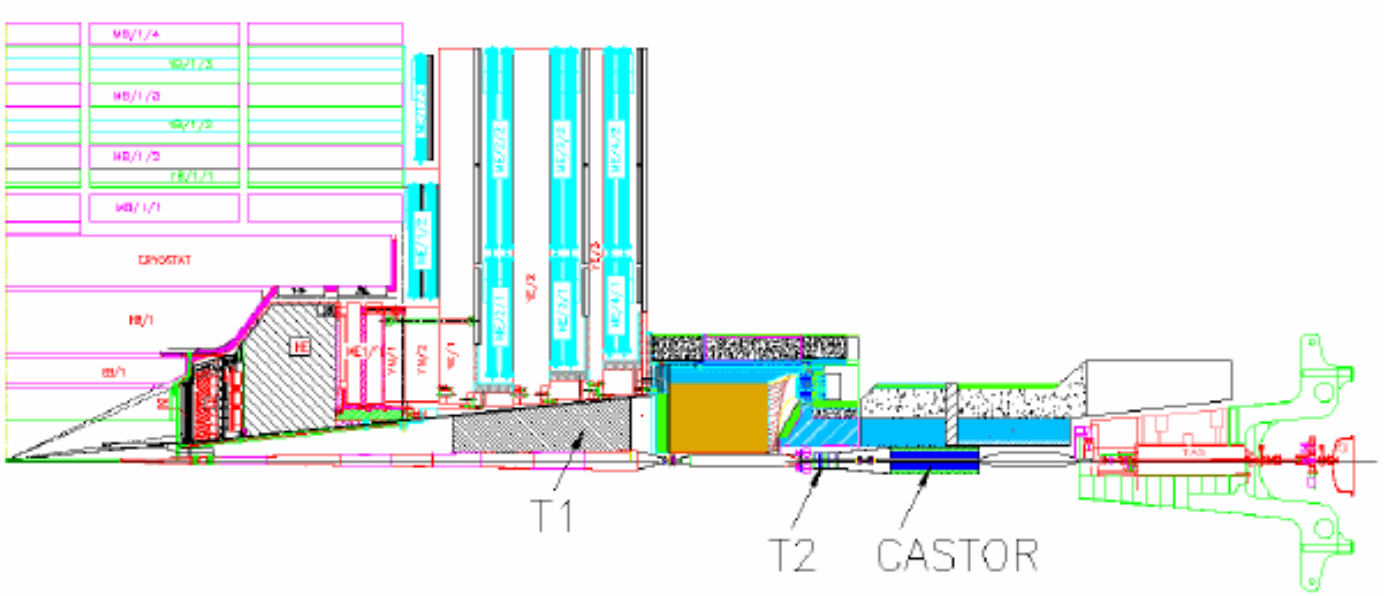


Figure 1.1: The TOTEM detectors are installed in the CMS forward region

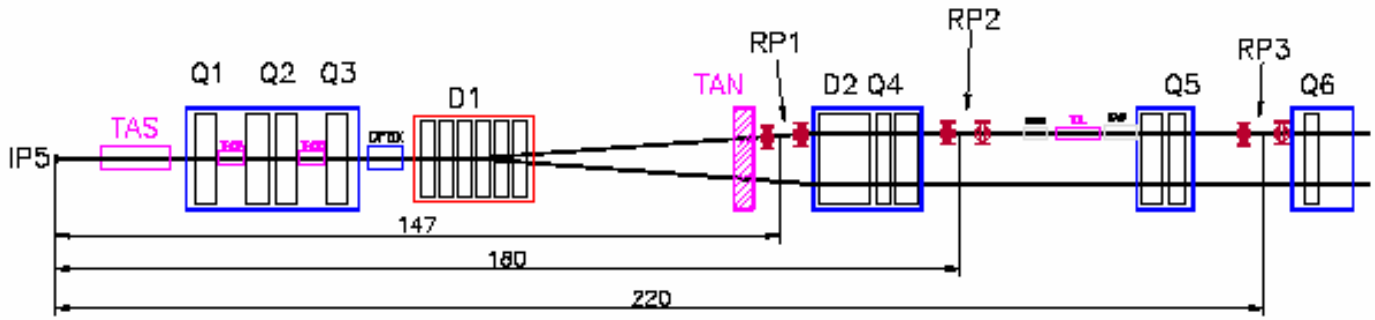
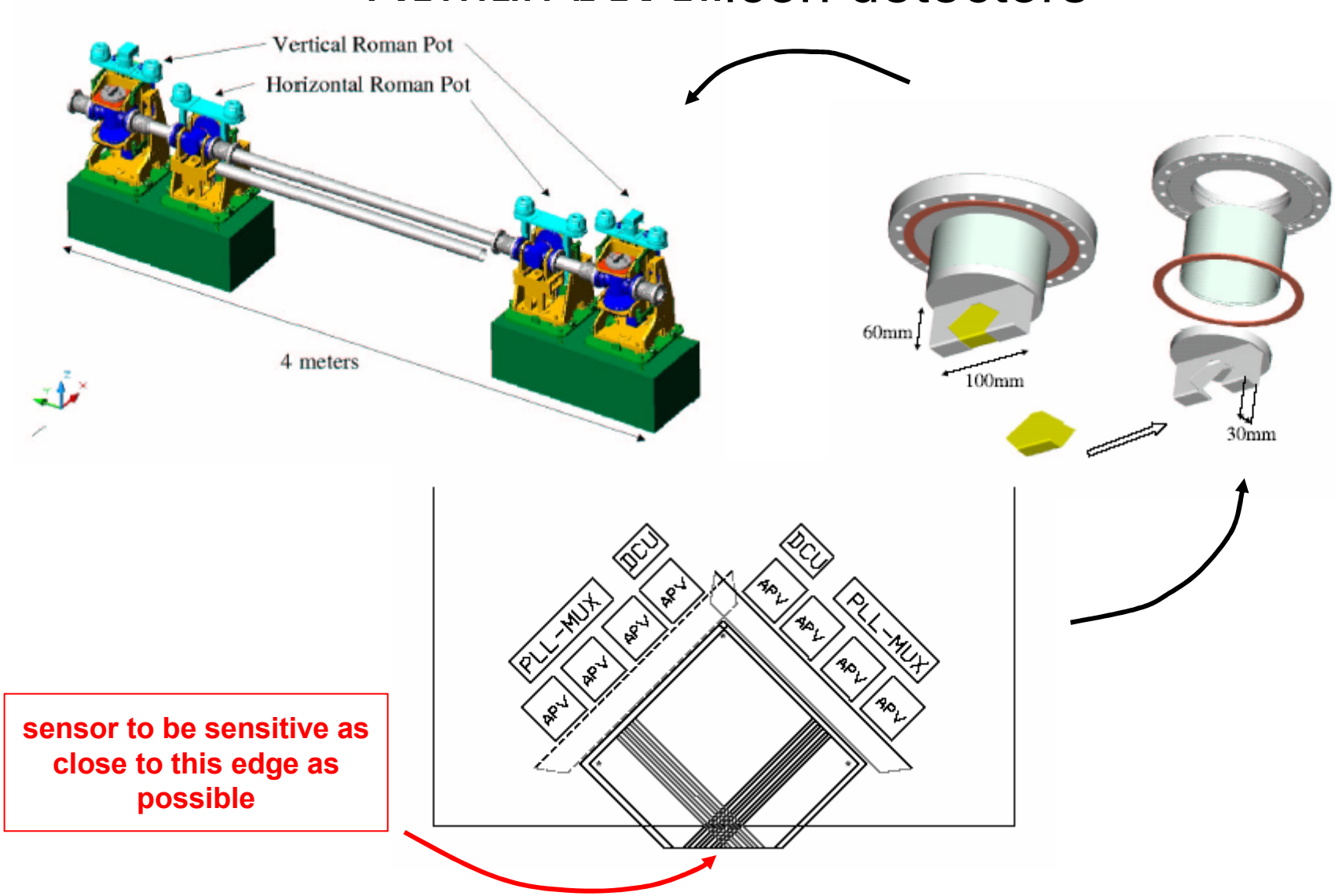


Figure 1.2: The LHC beam line and the Roman pots at 147 m and 220 m

Totem – total cross section, elastic scattering, diffraction dissociation at the LHC – forward, Roman pot silicon detectors



sensor to be sensitive as close to this edge as possible

3Dc

CERN-LHCC-2004-002
TOTEM-TDR-001
7 January 2004

Technical Design Report

The TOTEM experiment will measure the total pp cross section and study elastic scattering and diffractive dissociation at the LHC. More specifically, TOTEM will measure:

*** the total cross-section with an absolute error of 1mb by using the luminosity independent method. This requires the simultaneous measurement of the elastic pp scattering down to the four-momentum transfer of -t ≈ 10-3 GeV2 and of the inelastic pp interaction rate with an adequate acceptance in the forward region;**

*** elastic proton scattering over a wide range in momentum transfer up to -t ≈ 10 GeV2;**

•diffractive dissociation, including single, double and central diffraction topologies using the forward inelastic detectors in combination with one of the large LHC detectors.

From the minutes of the TOTEM Collaboration Board, Feb. 16, 2005:

* * * *

The suggestion I to keep two technologies: 3D strips and planar with CTS. 3Dstrips have a better edge behavior while the Russian CTS are less expensive. This choice does not require extra financing and manpower resources from the experiment. SW says that in the present situation it will be difficult for Brunel to contribute, but agrees that it is a good policy to have two vendor. Everybody agrees.

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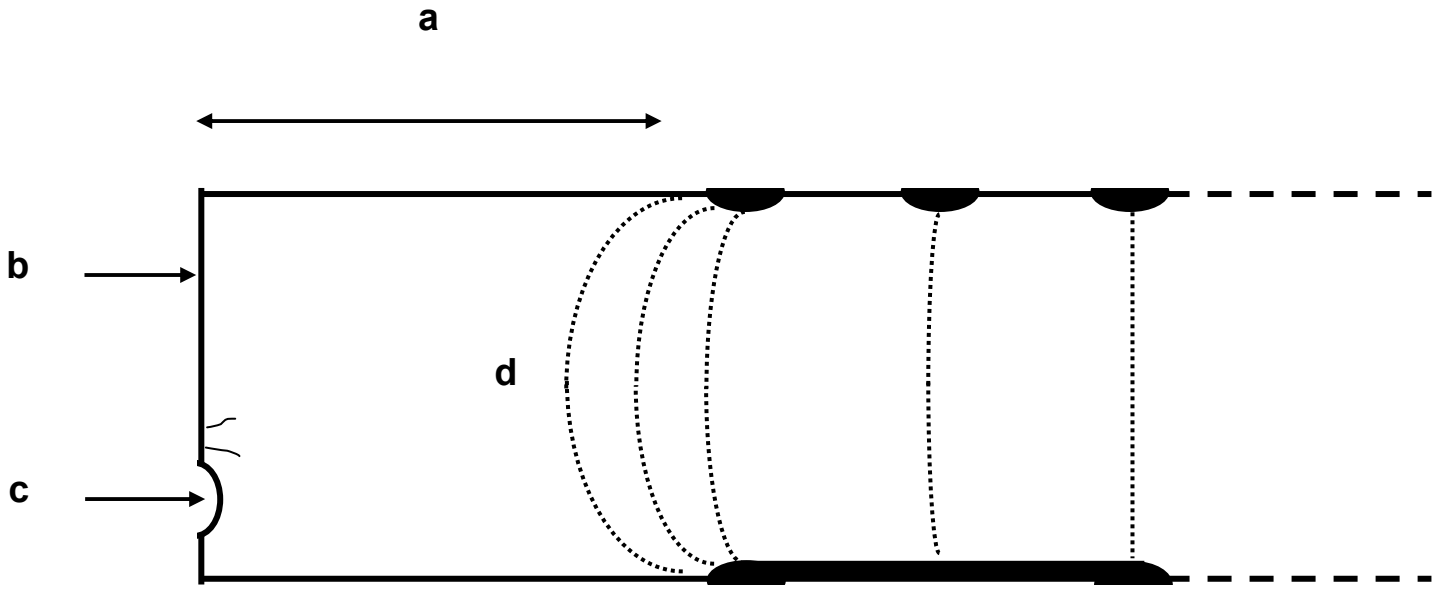
3Dc

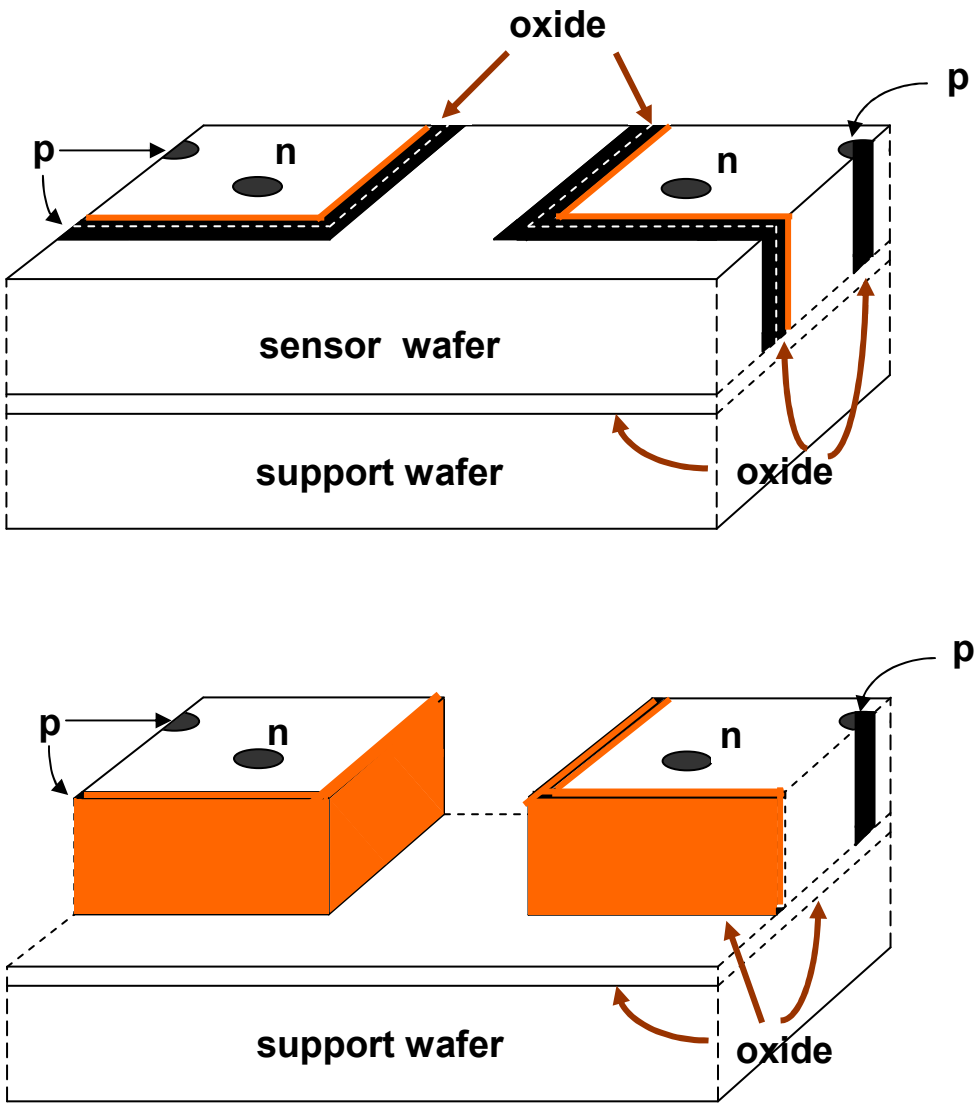
Reasons for dead borders on standard planar technology sensors



a. space for guard rings
b. sawed edges connecting top and bottom are conductors
c. chips and cracks are also conducting and can reach inside the edges
d. the field lines bulge out, and should be kept away from b and cs

3Dc

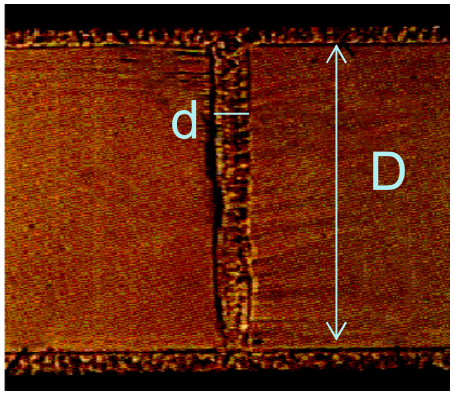
Active Edges



1. etch border trenches
2. diffuse in dopant
3. grow protective oxide cover
4. fill trench with poly
5. vertical, directed etch (to dotted lines)
6. turn off sidewall protection step
7. isotropic etch to oxide stop
8. additional steps are not included on this slide (and note, bonding oxide to support wafer not colored)
9. n and p electrodes can be reversed

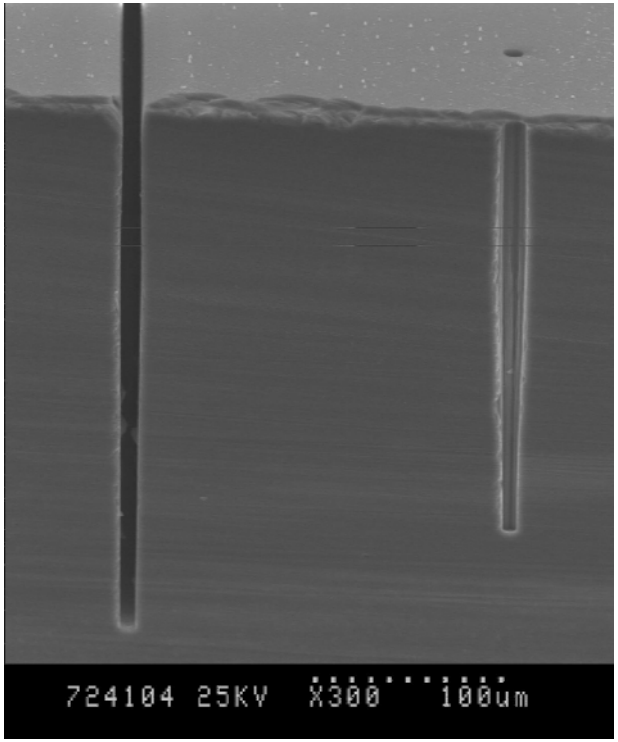
3Dc

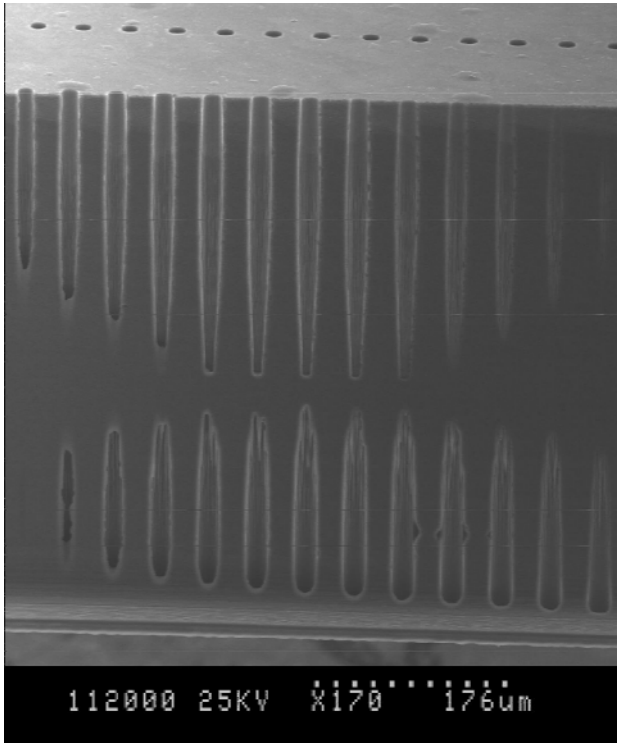
Some work on deep etching:



0. An old hole (filled).

D/d = 121 μm /11μm.

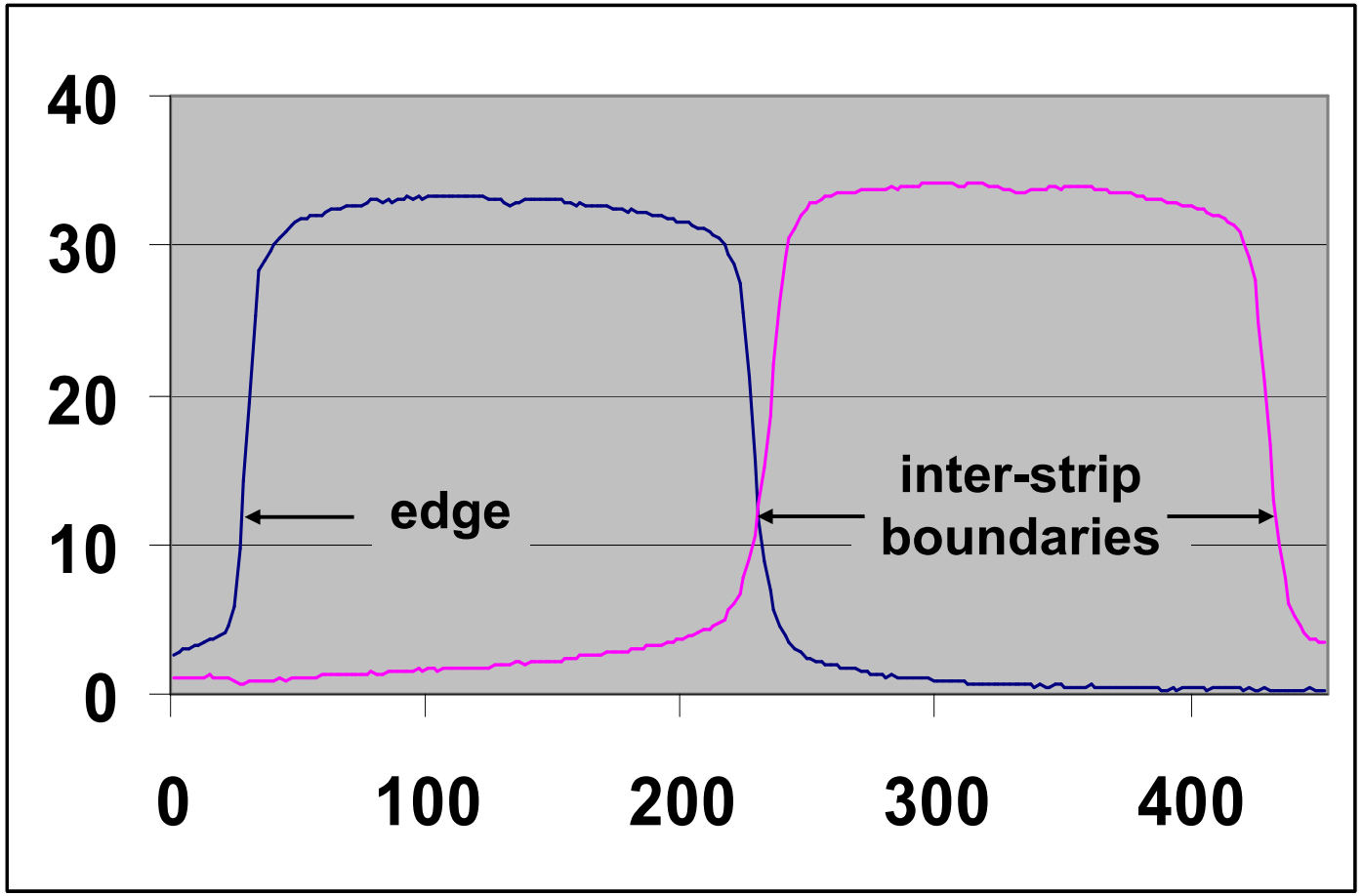




1. Process steps to improve depth / diameter ratios, and to make holes and trenches at the same time (middle). Note: $s(\updownarrow) = s(\leftrightarrow) \times \cos 20^{o}$.
2. True diameter from an angled saw cut: (right). D/d, top holes ≈ 18 / 1.
3. A second, newer STS etcher has just been installed at Stanford. It is faster and should make somewhat narrower holes and trenches.
4. The old etcher will become a "dirty" one, allowing us to make trench "dicing" etches on wafers with indium bumps.

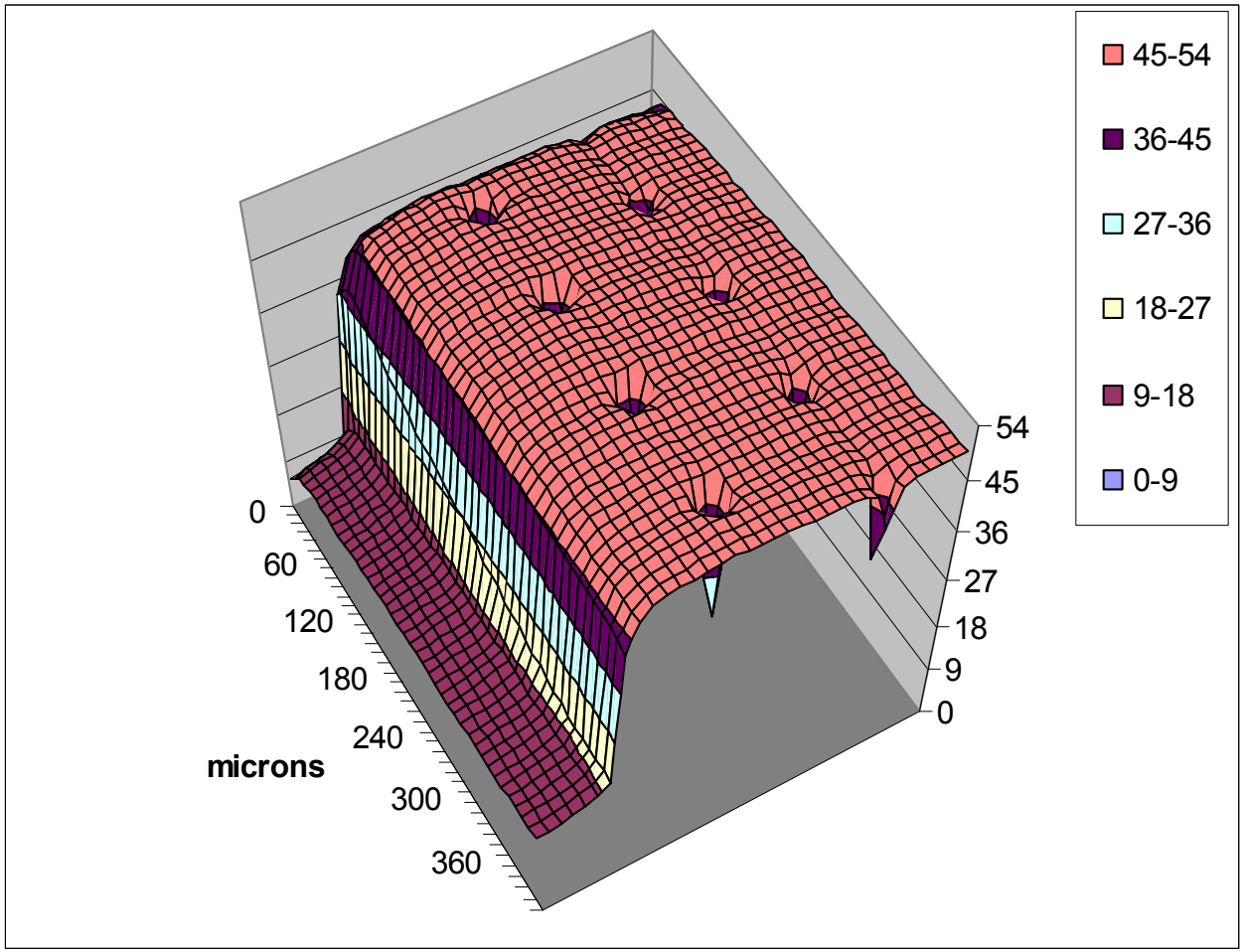
3Dc

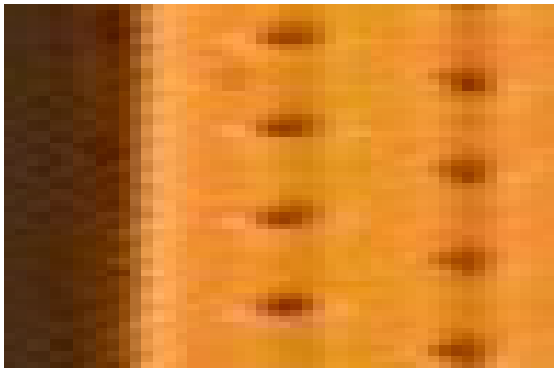
X-ray microbeam results for a 3D sensor



X-ray micro-beam scan, in 2 μm steps, of a 3D, n bulk and edges, 181 μm thick sensor. The left curve is for the edge p channel. The horizontal scale is in μm; the vertical is arbitrary. The small dip in each center is from nearby 3D electrodes. The left edge tail is from reflected gold x-rays and from leakage current.

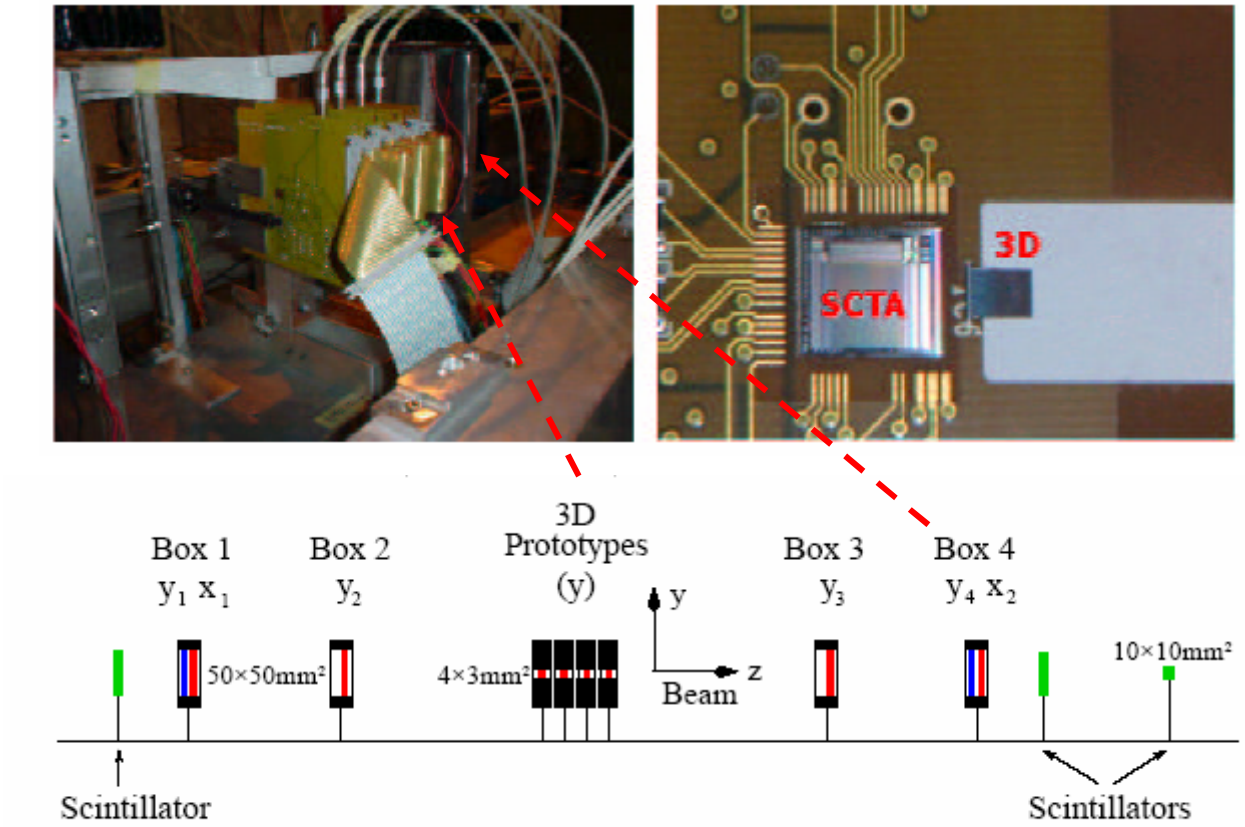
3Dc





Current from scan in an x-ray microbeam, of another 3D sensor with a photomicrograph of the corresponding part on the right. Grid lines are spaced 10µm apart.

3Dc

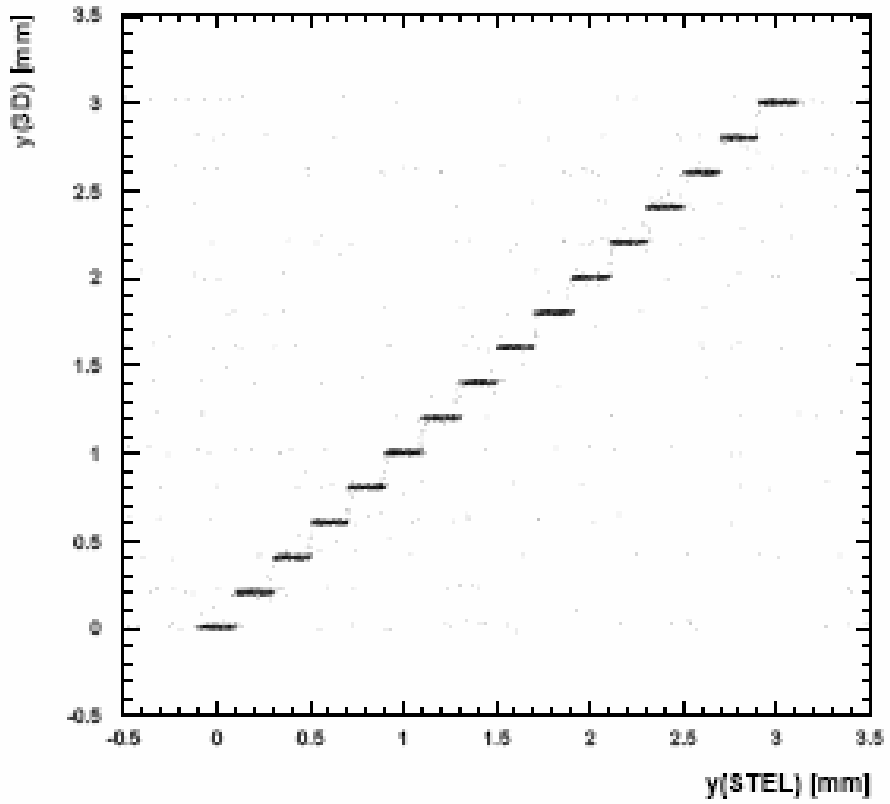


Totem X5 test beam at CERN.

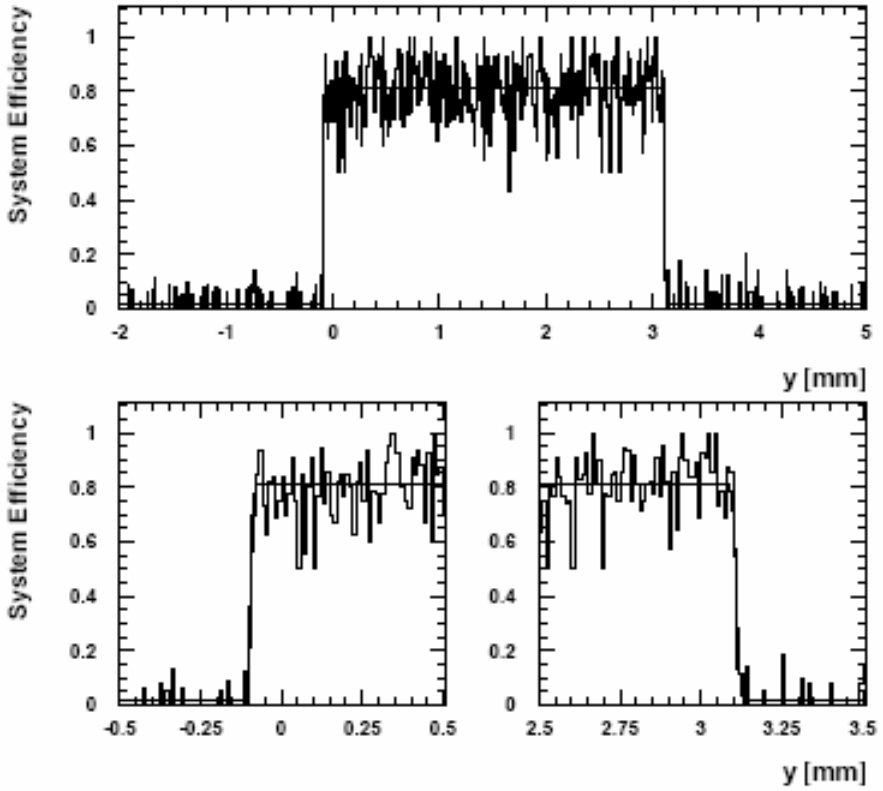
1. **The 3D planes: 16 -- 200 µm (y) by 40 -- 100 µm (x) cells, n bulk and edges.**
2. **They are tied together in x-rows for a y readout using SCTA integrated circuits and a scintillator trigger.**
3. **The 3D planes are centered between a 4-plane silicon strip telescope with 4 y planes and 2 x ones. σy = ± 4 µm.**
4. **The beam was set for 100 GeV muons.**

3Dc

Some results from the CERN X5 beam test (100 GeV muons)



Measured hit position in 3D sensor plane #3 vs. predicted position from beam telescope.



Fitted 3D sensor width = 3,203 ±4 µm. Drawn width = 3,195 µm. Sensor efficiency = 98%. System efficiency less due to DAQ, triggering electronics.

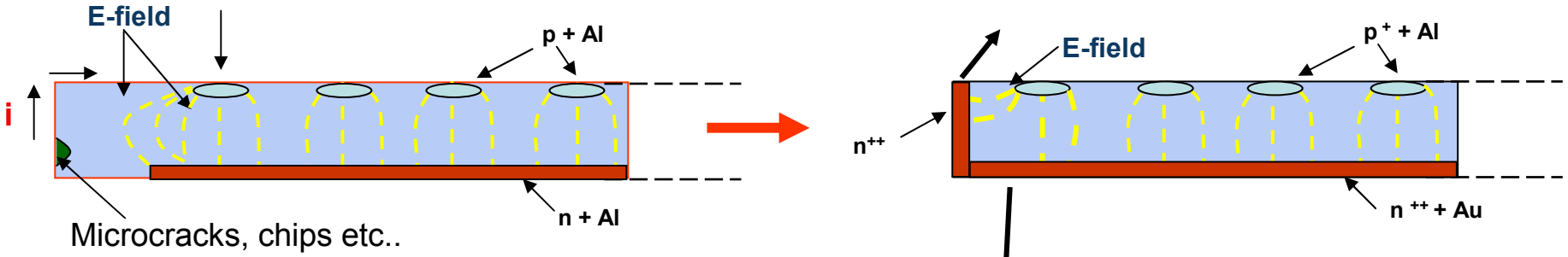
3Dc

PLANAR DEVICES WITH 3D ACTIVE EDGES

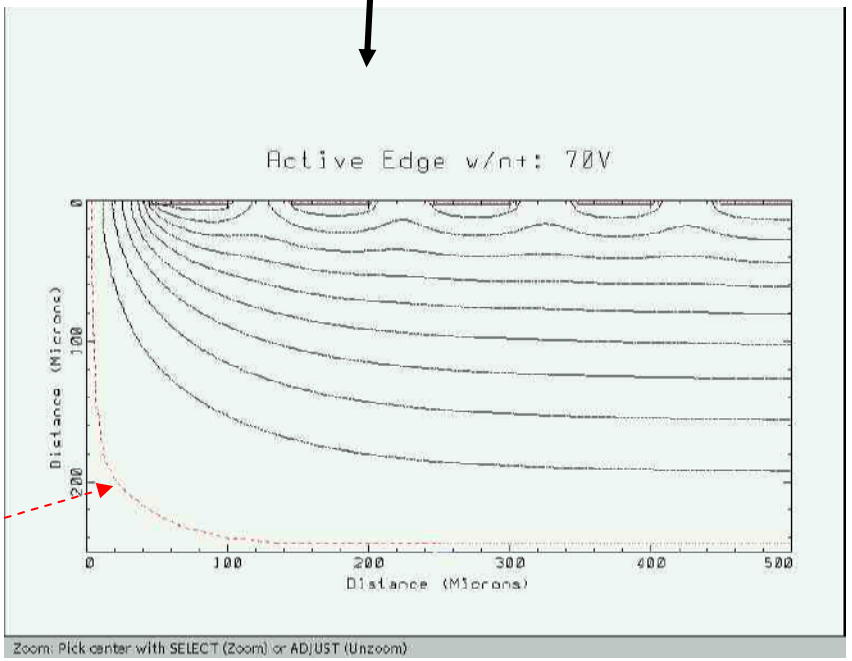
PLANAR

PLANAR / 3D =

PLANAR DETECTOR + DOPANT DIFFUSED IN FROM DEEP ETCHED EDGE, CAPPED WITH OXIDE, FILLED WITH POLYSILICON, POLY FINALLY ETCHED AWAY



MEDICI Simulation of the equipotential lines for a 70 V bias 300 μm device (J. Segal MBC)



Depletion boundary

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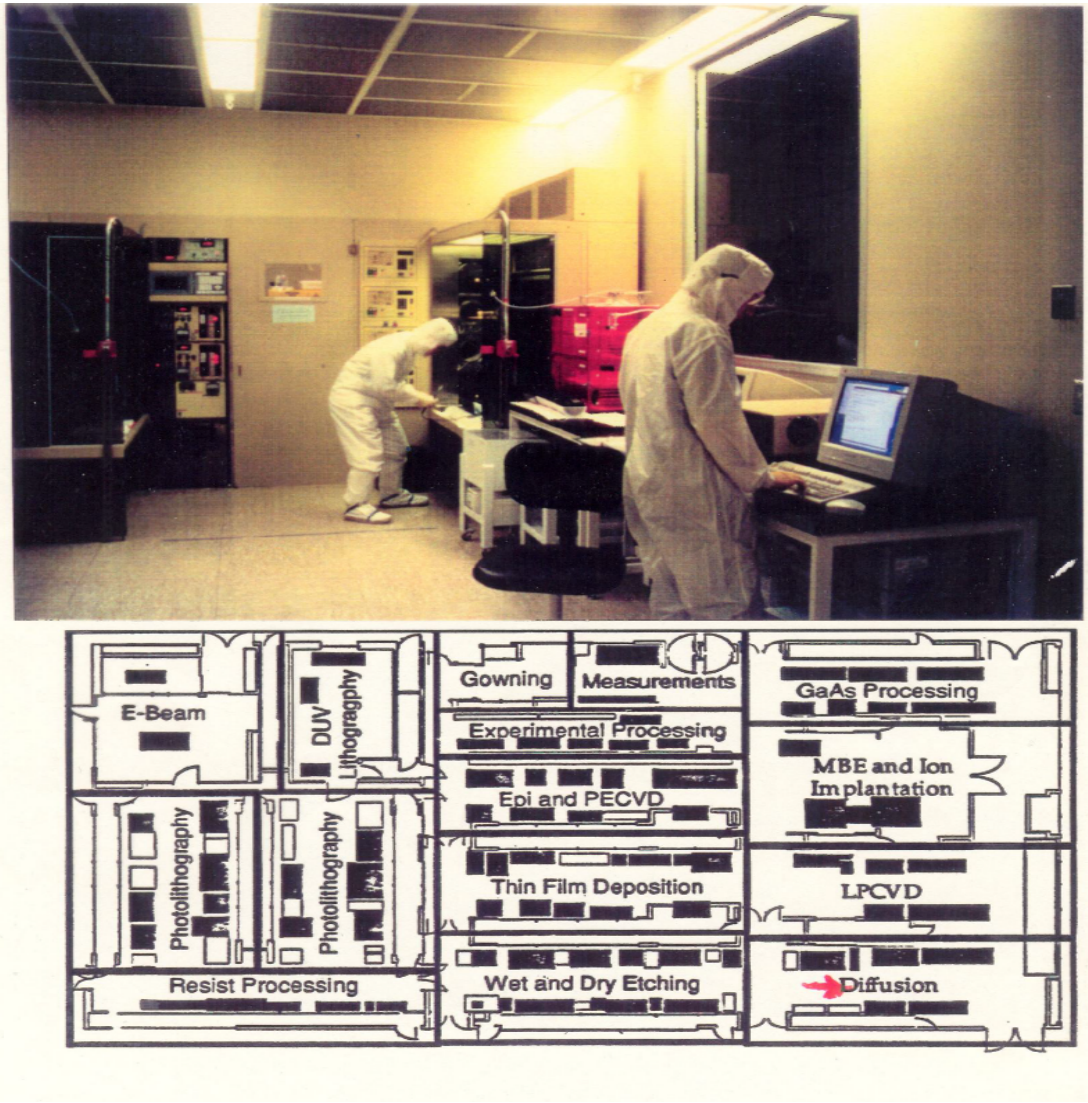

Figure 6. Stanford clean room near diffusion furnaces, looking in the direction of the red arrow.

3Dc

Pictures of clean rooms like the one preceding are familiar, but many other things are needed for high yield, for example: specific, careful checking of the results of each of the 37 main steps and of the many sub-steps, cleanliness not just of the room and air, but of everything used – tools, chemicals, cassettes, etc.

The deep etching may leave an uneven surface that makes it difficult to spin on a uniform layer of photoresist for a following lithography step. If this step is a deep etch, a thick resist is needed. They seem to have a higher level of particulates and clumps of resist.

Active edge fabrication requires support wafers, which must be oxide-bonded to the sensor wafer under extremely clean conditions.

The following specific steps were added to the fabrication procedure for the two-order-of-magnitude larger, 9 cm^2 planar / 3D active edge Totem sensors:

1. The wafers were carefully inspected after every litho step. If defects were seen, the resist was removed, new resist was applied, and the wafers were re-spun and re-exposed.

2. Defects in the thick resist used for the trench etch were covered with polyimide.

3. The surface planarity in the region of the dips at the centers of the poly-filled electrodes was improved by etching the poly off the top surface, and then repeating the fill and etch procedure.

4. The plasma dice lane was widened from 50 microns to 120 microns. The more open trench prevented the formation of silicon chips along the trench edges. This seems to have eliminated this defect class, which caused a 25% loss for the first batch.

5. Evaporated aluminum instead of sputtered gold was used for the backside contact.

In the first Totem fabrication run of full-size sensors, only 1 of 28 sensors had 99% or more good strips. After the 5 yield enhancement steps were added,13 of 20 sensors from the next run had at least 99% good strips:

RESULTS: full-sized, 512-strip, planar / 3D active-edge sensors, 60V

	sensor	leakage current (μA)	strips with defects	% good strips	comments
1	t4 – 4c	0.7	0	100	
2	t4 – 5c	0.8	0	100	
3	t4 – 7c	0.7	0	100	
4	t4 – 4a	0.7	1	99.8	100% at 30V
5	t4 – 5b	0.8	1	99.8	defect is on back
6	t4 – 6c	0.6	1	99.8	
7	t4 – 8b	0.9	1	99.8	
8	t4 – 7a	1.1	2	99.6	
9	t4 – 7b	0.7	2	99.6	
10	t4 – 4b	0.8	3	99.4	100% at 30V
11	t4 – 8a	1.2	3	99.4	
12	t4 – 8c	1.6	3	99.4	
13	t4 – 8d	1.9	3	99.4	
14	t4 – 5d	1.3	>5	~ 99.0	
15	t4 – 7d	0.7	8	98.4	
16	t4 – 4d	1	>10	<98.0	testing stopped at 255
17	t4 – 5a	-	-	-	hole etched through chip
18	t4 – 6a	-	-	-	hole etched through chip
19	t4 – 6b	-	-	-	not tested
20	t4 – 6d	-	-	-	not tested

Now we must produce similar results for full 3D sensors.

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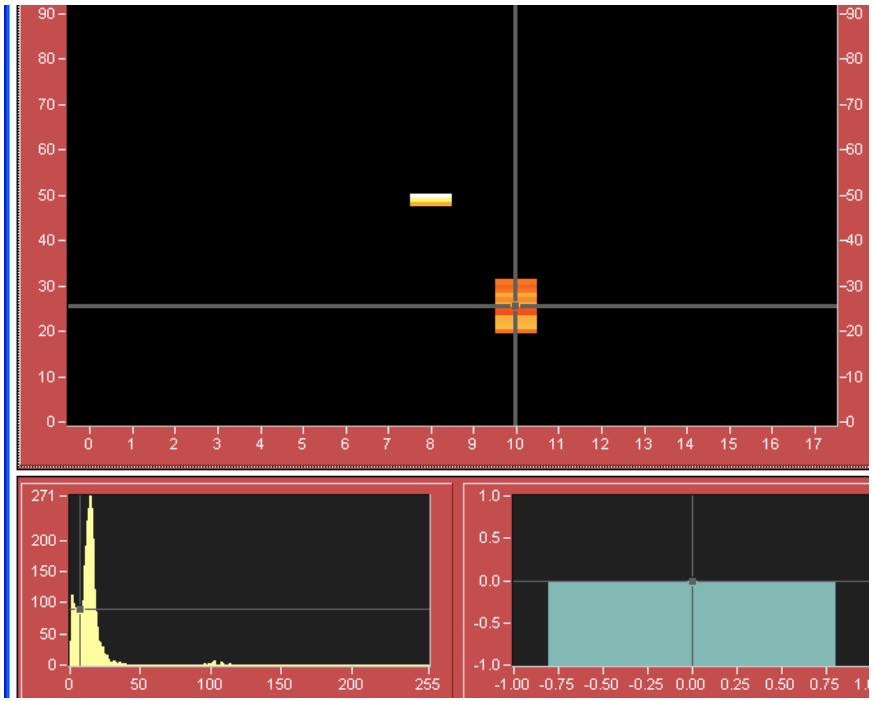
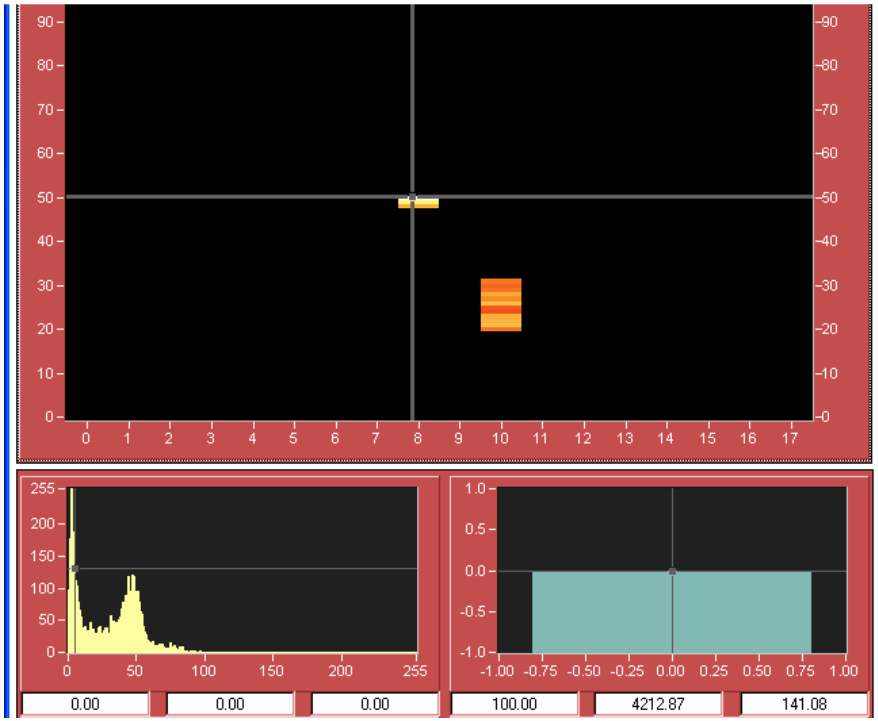


More typical spectrum



TOT spectrum for the best looking pixel

Possible steps for improvement of fabrication yields:

- Improvement of fabrication steps (as was done for planar / 3D active edge sensors).
- Use solder bumps at wafer scale.
- 2-3 month fabrication run rather than 5 week run.
- Use of P- type bulk so diode junctions always at signal electrodes so one bad junction does not short bias supply.
- Probably won't need to reduce signal electrode capacitance using poly-resistor isolation of bias electrodes, but it remains a possibility.

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Fabrication

1. It would be best to have commercial fabricators. Some discussions have been held with companies making sensors.
2. However the companies currently having the specialized plasma etchers used for 3D fabrication tend to be micromachining companies, not sensor ones.
3. Second sources, as some LHC collaborations can confirm, can be important.
4. It is difficult to get even a first source, in the absence of the prospect of an order.
5. We can make the needed sensors at Stanford, if necessary. At the minimum, that will supply a second source. We now discuss fabrication at Stanford:

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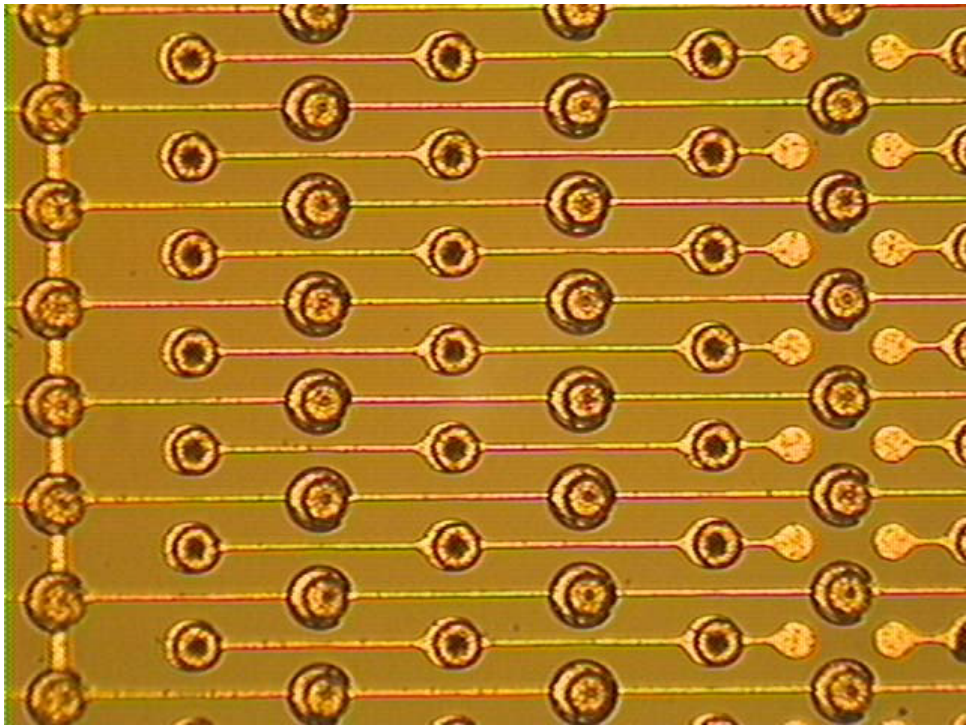
Module Production

10 Modules per Wafer

150 mm Wafers

230 Wafers Divided by Yield

or (next slide) make readout-chip size units:



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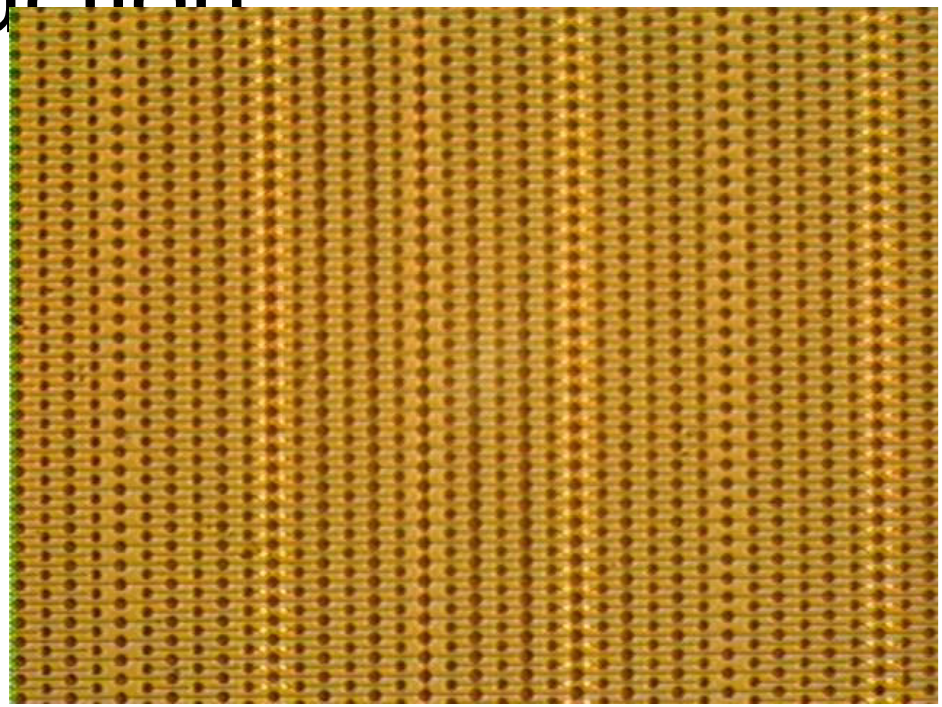
Chip Production

- 209 Chips per Wafer
- (i.e. one active edge sensor chip for each readout chip)
- 150 mm Wafers



- 170 Wafers Divided by Yield
- Chip Yield is Probably Much Higher then Module Yield

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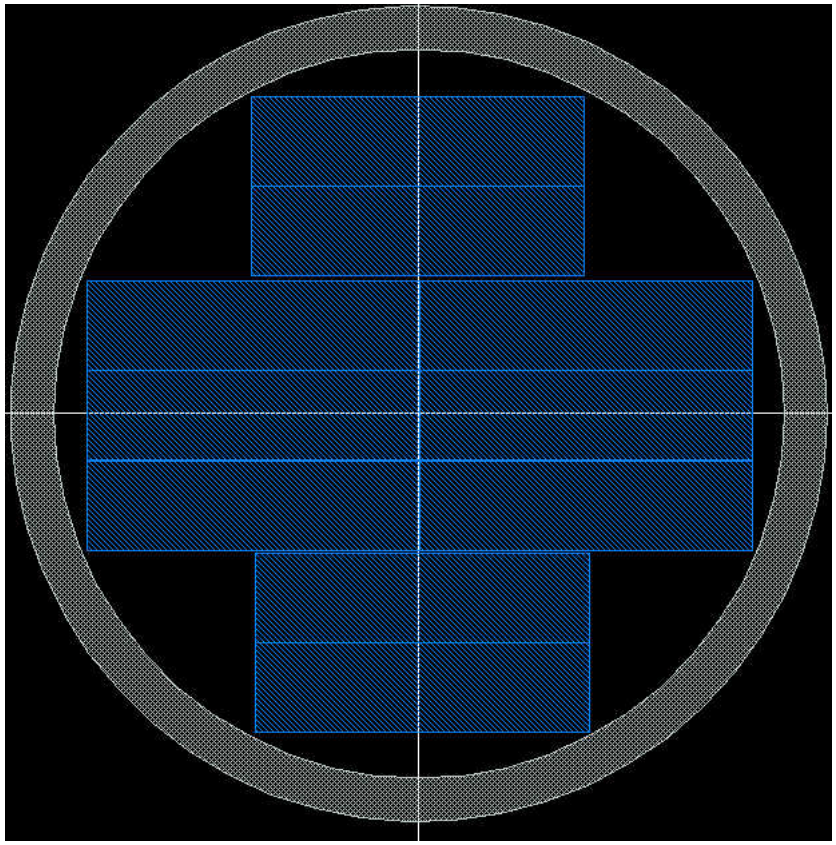
Module Layout

Dimensions:

61mm by 16.4 mm

10 Modules Per 150 mm Wafer



Area Used:
10,000 mm^2 – 10 Modules

80 Percent of Chip Area

3Dc

Chip Layout

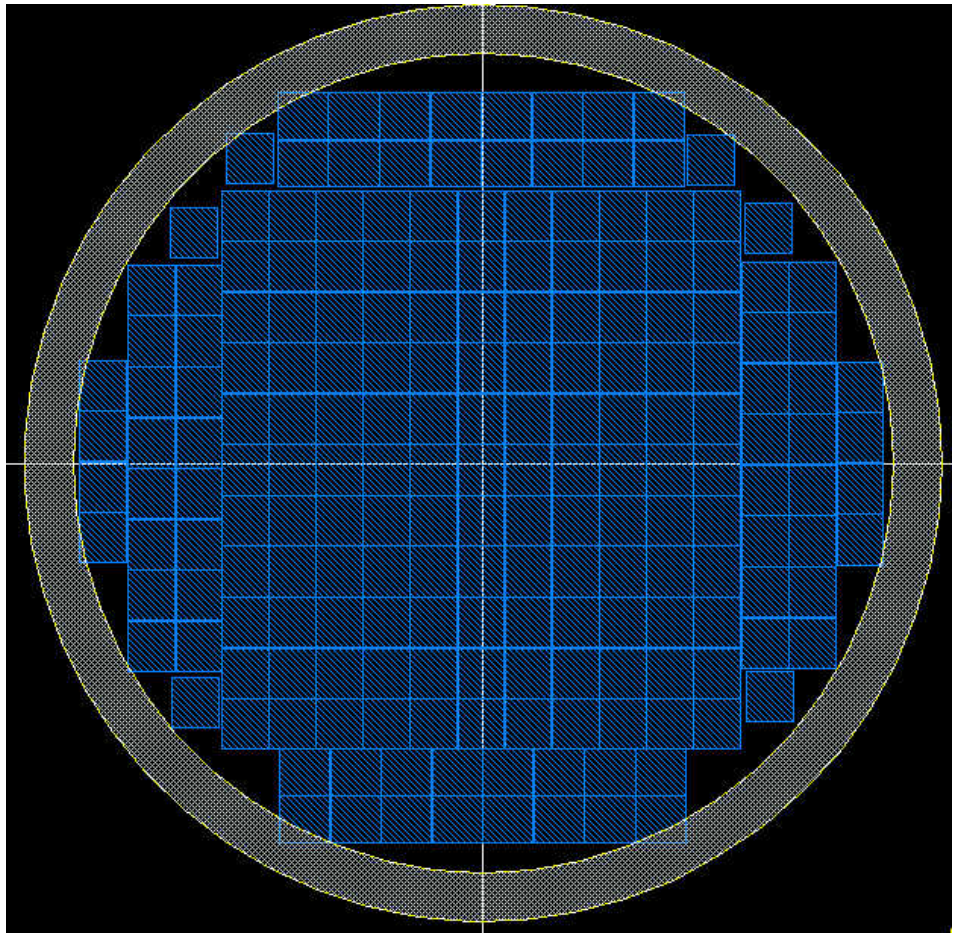
Dimensions:

7.6 mm by 8.2 mm

209 Chips Per 150 mm Wafer

Area Used:

13,025 mm^2



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Budget

Item	Modules NO/DRIE	Modules w/DRIE	Chips w/DRIE
Fab Usage	$200,000	$100,000	$80,000
Thinning	$20,000	$20,000	$20,000
Float Zone Wafers	$23,000	$23,000	$17,710
Test & Fusion Wafers	$10,000	$10,000	$7,700
Supplies	$20,000	$20,000	$20,000
DRIE Etcher	$0	$350,000	$350,000
Masks	$30,000	$30,000	$30,000
Personnel	$800,000	$400,000	$320,000
TOTAL	**$1,103,000**	**$953,000**	**$845,410**
Time (Months)	**24**	**12**	**9.2**

Divide by Device Yield (Range 40 to 75 Percent)

Add overhead and Contingency

So at least Double these Amounts

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CERN-LHCC-2005-025
LHCC-I-015

FP420 (L.O.I.)

An R&D Proposal to Investigate the Feasibility of Installing Proton Tagging Detectors in the 420m Region at LHC

M. G. Albrow[1], T. Anthonis[2], M. Arneodo[3], R. Barlow[2,4], W. Beaumont[5], A. Brandt[6], P. Bussey[7], C. Buttar[7], M. Capua[8], J. E. Cole[9], B. E. Cox[2,*], C. DaVià[10], A. DeRoeck[11,*], E. A. De Wolf[5], J. R. Forshaw[2], J. Freeman[1], P. Grafstrom[11,+], J. Gronberg[12], M. Grothe[13] , J. Hasi[10], G. P. Heath[9], V. Hedberg[14,+], B. W. Kennedy[15], C. Kenney[16], V. A. Khoze[17], H. Kowalski[18], J. Lamsa[19], D. Lange[12], V. Lemaitre[20], F. K. Loebinger[2], A. Mastroberardino[8], O. Militaru[20], D. M. Newbold[9,15], R. Orava[19], V. O'Shea[7], K. Osterberg[19], S. Parker[21], P. Petroff[22], J. Pinfold[23], K. Piotrzkowski[20], M. Rijssenbeek[24], J. Rohlf[25], L. Rurua[5], M. Ruspa[3], M. G. Ryskin[17], D. H. Saxon[7], P. Schlein[26], G. Snow[27], A. Sobol[27], A. Solano[13], W. J. Stirling[17], M. Tasevsky[28], E. Tassi[8], P. Van Mechelen[5], S. J. Watts[10], T. Wengler[2], S. White[29], D. Wright[12]

1. Executive Summary

The physics potential of forward proton tagging in the 420m region at the LHC has only been fully appreciated within the last few years. By detecting protons that have lost less than 1% of their longitudinal momentum, a rich QCD, electroweak, Higgs and BSM program becomes accessible, with the potential to make measurements which are unique at LHC, and difficult even at a future linear collider.

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Structural Molecular Biology

1. The human genome project has given us a first draft for the order of the base pairs in our DNA, specifying the order in which amino acids (one for each three base pairs) are assembled to make proteins.

2. It does NOT tell us what the proteins look like or what they do.

3. Understanding that—the keys to their biological activity – requires knowledge of their three dimensional shape and charge distribution.

4. Even though they are made in a linear fashion as the RNA is read out, they fold – or are folded – into highly complex shapes. The sequence may also be altered.

5. They are far too small to be seen in an optical microscope, have too much internal detail for scanning tunneling microscopes, and are too delicate for the vacuum and electrical conditions of an electron microscope.

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6. Their structure can be determined by illuminating them with collimated, mono-energetic x-rays, and measuring the scattering intensity over a range of angles. Each outgoing angle gives information from a different view of the molecule.

7. Extra intensity measurements with sulfur replaced by selenium, or of anomalous scattering near an absorption edge, are used to give phase information.

8. To get enough counts, many molecules must be used. To keep the patterns coherent, they must be aligned in a crystalline form.

9. We plan to use an array of shingled, active-edge, 3D silicon sensors to measure those patterns.

Crystallography area detectors

Now use phosphor screen / multi-fibreoptic bundle /CCD mosaic readout.
Up to 300 x 300mm2 square and with PSF ~100μm FWHM

Limitations:

•intense diffraction spots in image spoil the usable dynamic range (which for a CCD is always < “16 bits”)

• Long tails associated with the ‘Lorentzian’ spatial response of the phosphor screen+optics. This *limits the precision of flat field corrections* and measurement of close-spaced diffraction peaks…

•*Protein Samples rapidly degrade in the X-ray beam (synchrotron IDs -->10^{13} photons/sec).*
CCD systems require *a few seconds* to readout, while strongly diffracting crystals can saturate the CCD full well capacity in *~0.1sec*

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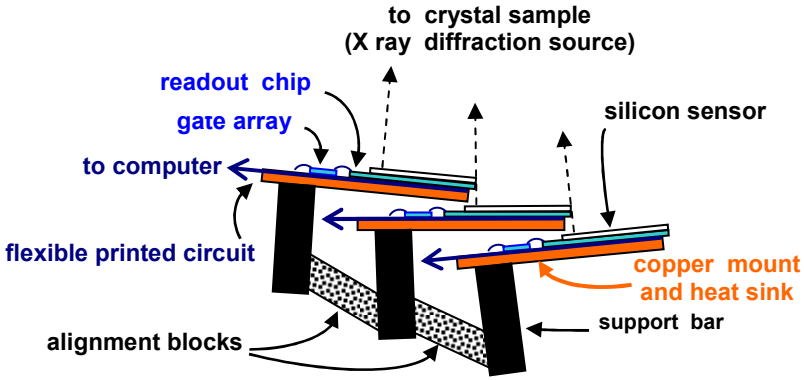
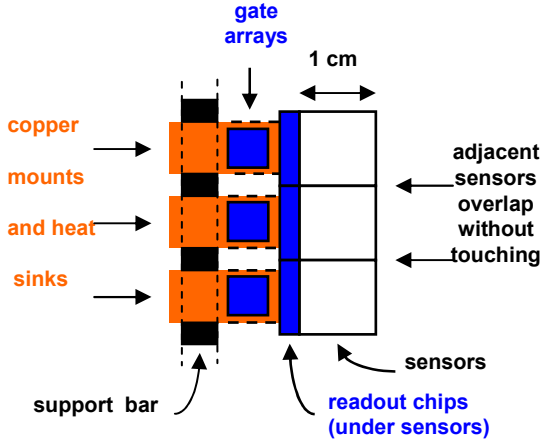
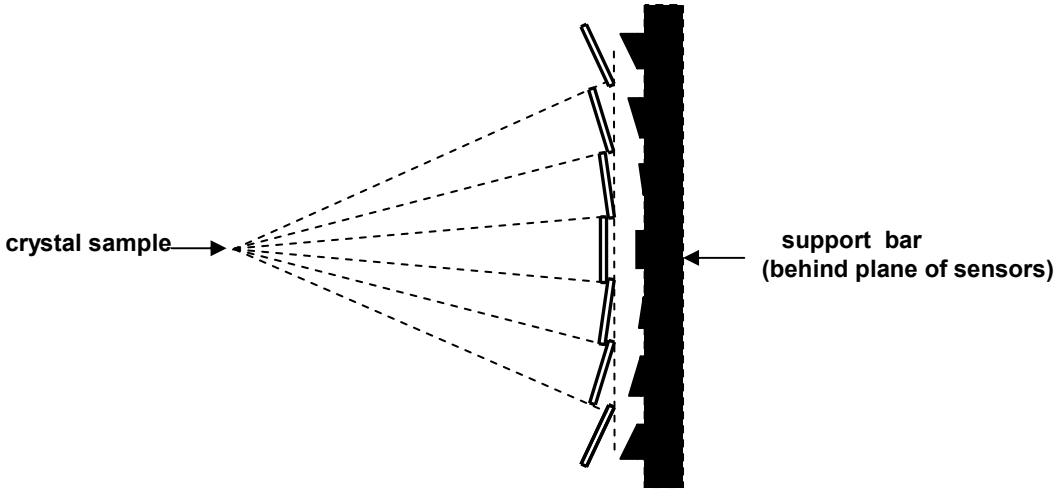
3DX x-ray detector array for structural molecular biology



a: top view of 3 modules (in central plane)



b: front (x-ray) view of 1 column



c: side view of one column

(all sensors normal to diffracted x-rays)

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Pixel Design

1. 64 x 64 pixels, each 150 µm x 150 µm.
2. Readout pixels are only 144 µm x 150 µm, keeping the readout chip fully under the sensor.
3. Each pixel has an integrating amplifier.
4. 2 rows are read out together, using 128 lines.
5. Integration resumes after 1 µs.
6. Pulse heights are digitized in a Wilkinson ADC.
7. Readout moves to next two rows after an additional µs.
8. Data is output to the computer from alternate buffers. The full sensor is readout every 64 µs.
9. Charge-shared signals can be recombined in the computer.
10. Small replaceable units for efficiency (PILATUS dead area = 8.1% (pixels) + 4.4% (gaps) = 1 / 8)

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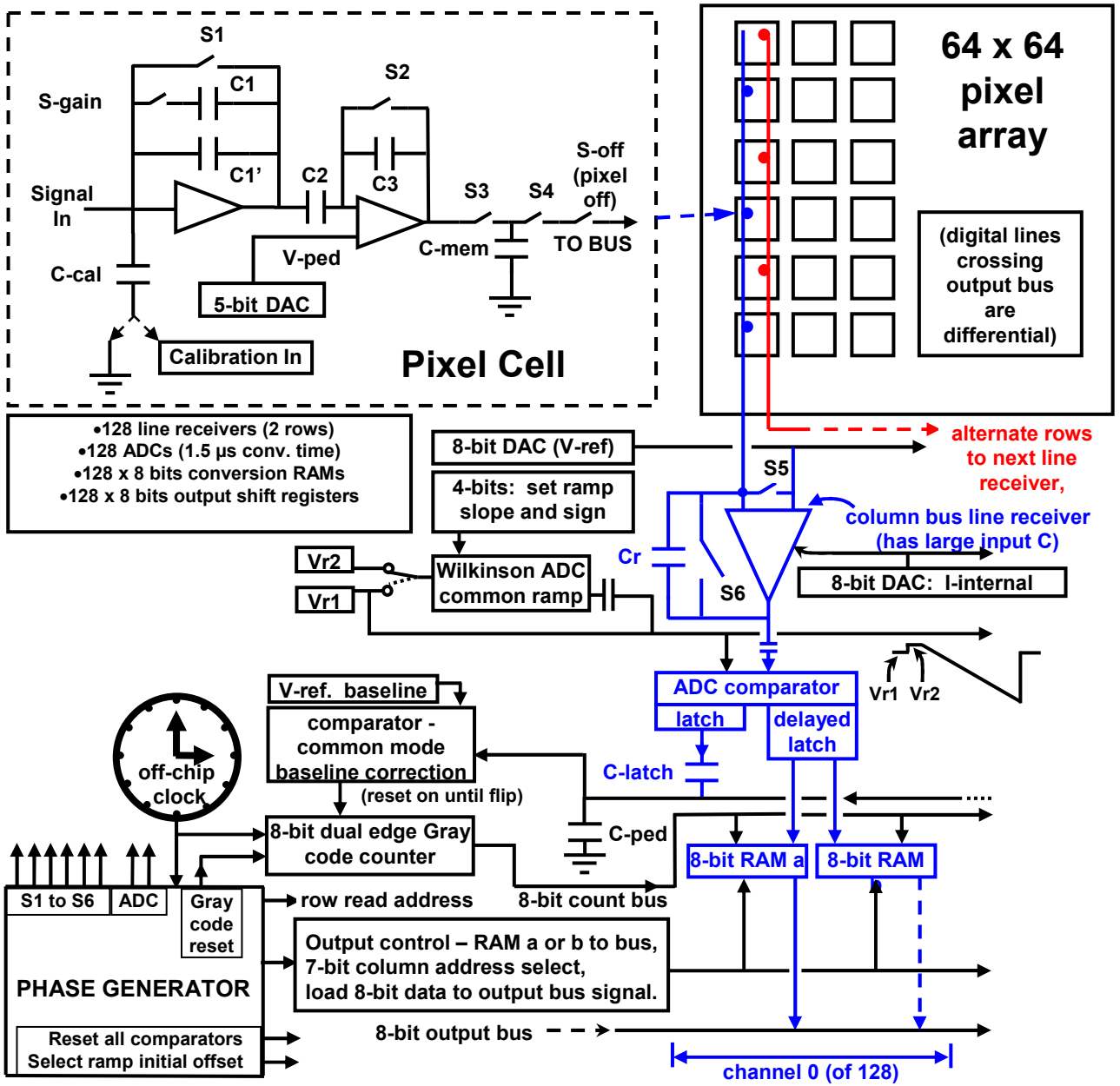

Figure 6. Block diagram of VLSI readout circuit.

Capacitor values (fF): C1=37, C1'=25, C2=75, C3=25, C-mem=900
C-receiver =450, C-cal=16, C-latch ≈10, C-ped ≈ 1,000, C-column bus ≈ 3,000

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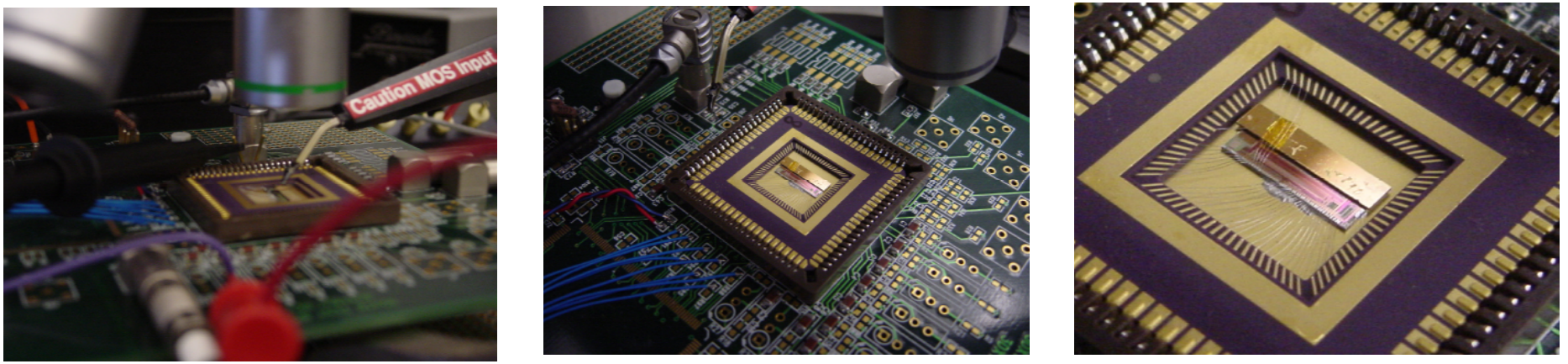


Figure 13. Sensor – readout chip – chip carrier mounted on a circuit board and placed on a probe station (left), and at larger magnification (center and right). The wire bonds to the chip carrier are visible in the right view.

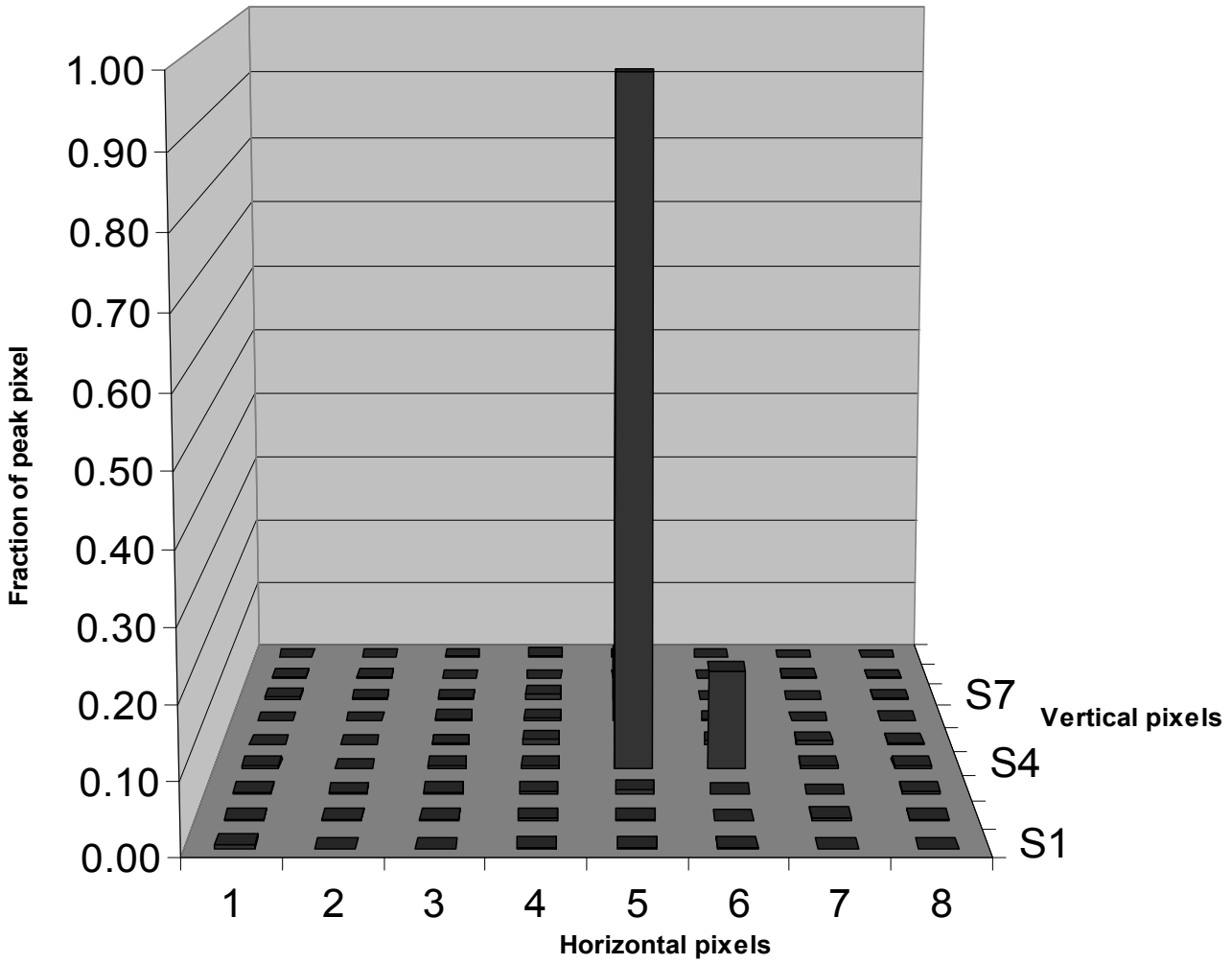
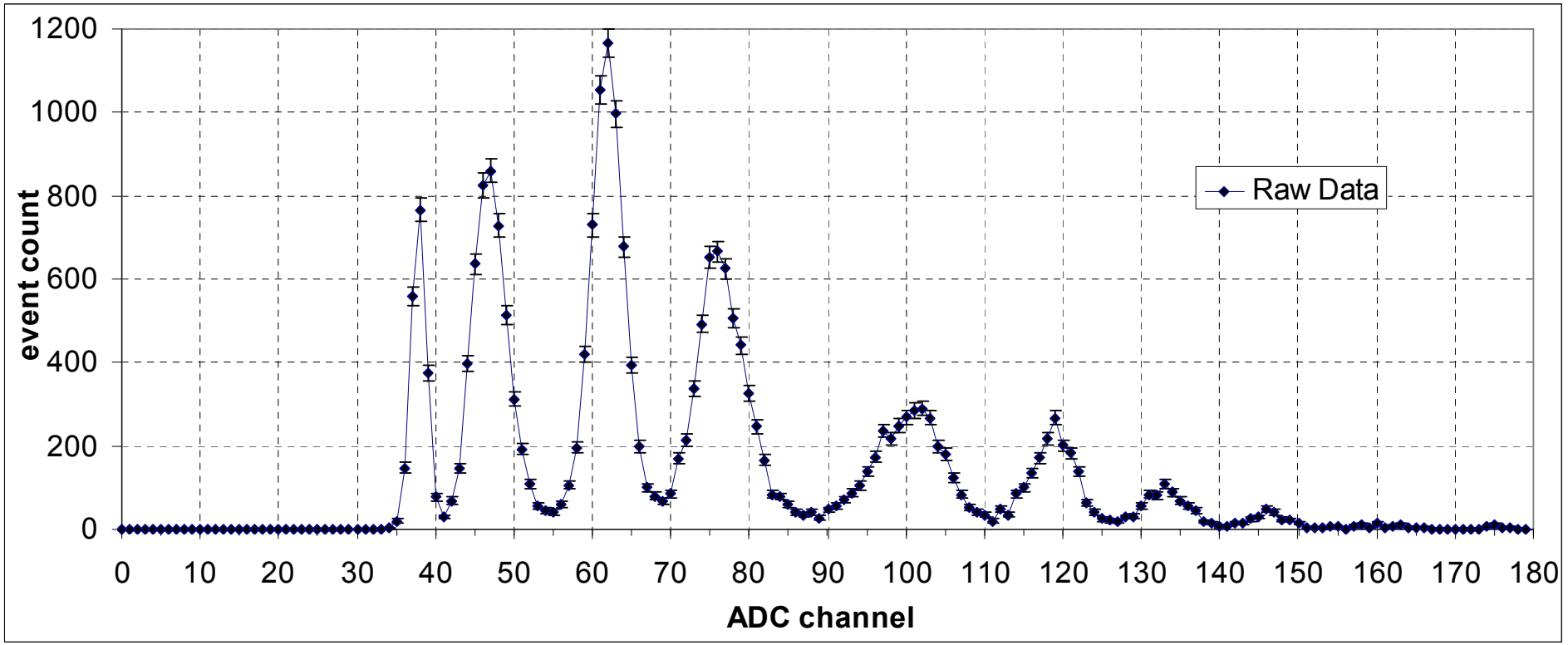


Figure 16. Map of 8 x 8 pixel area surrounding aiming point of the x-ray beam.


1200
1000
800
600
400
200
0
event count
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160
170
180
ADC channel
Raw Data

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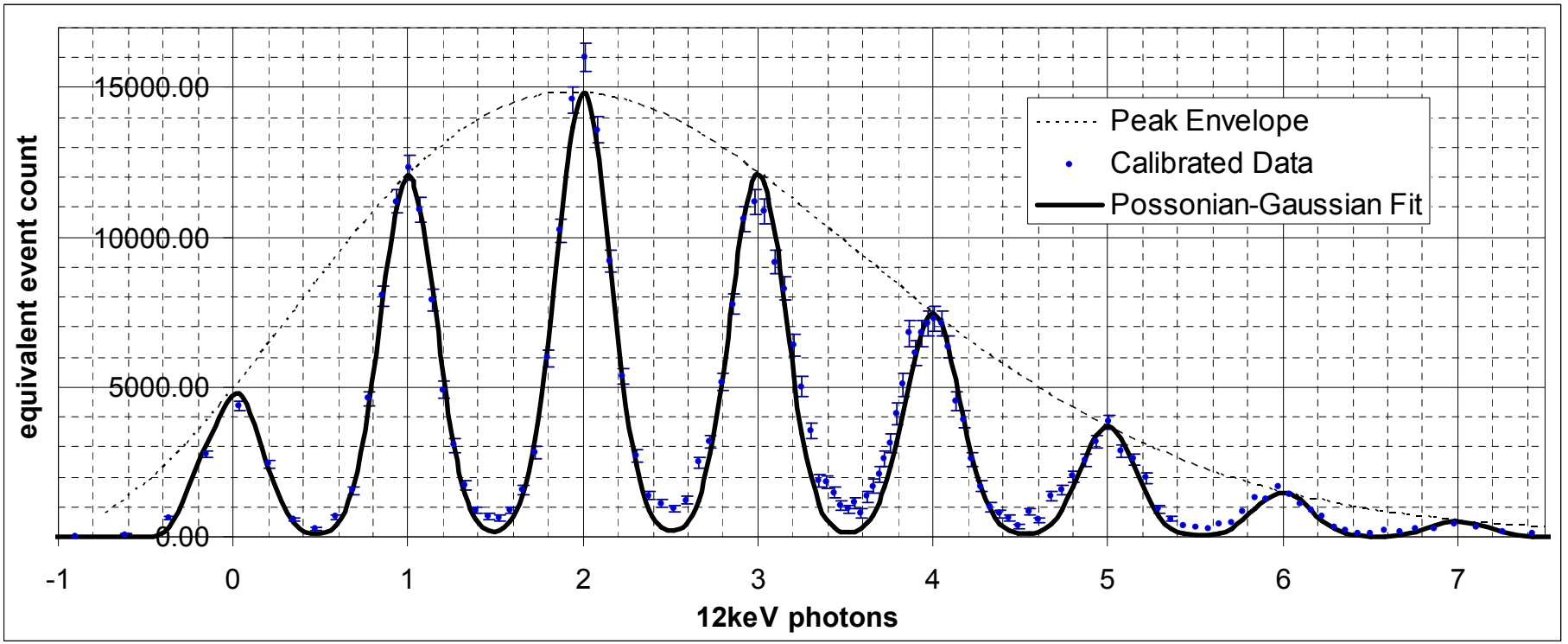
15000.00
10000.00
5000.00
0.00
equivalent event count
-1
0
1
2
3
4
5
6
7
12keV photons
Peak Envelope
Calibrated Data
Possonian-Gaussian Fit

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Conclusions

1. Expectations for 3D sensors from the initial calculations have been verified:

   a. They are fast. Amplifier-limited rise and fall times of 3.5 ns at room temperature, even after irradiation by 10e15 / sq. cm. have been measured. (A new 0.13 micron line-width amplifier, has a rise time of 1.5 ns, makes pulses of 4.5 to 5 ns full width at the base.)

   b. They deplete at low voltages (~ 5 – 10 V) and have wide plateaus for infrared microbeam signals.

   c. Good resistance to radiation damage has been verified. (A sensor not designed for radiation hardness, with no oxygen diffusion, and no beneficial annealing had a signal plateau from 105 V to 150 V for an infrared light beam after irradiation by 10e15 55 MeV protons sq. cm (≈ 1.8 e 15 1-MeV neutrons / sq. cm.).

2. Outside the center parts of the electrodes, charge collection is efficient: a 14 KeV x-ray line from a 241-Am source fits a symmetric Gaussian with a sigma of 282 eV.

3. Sensors have reasonable leakage currents: about 1 nA / cu. mm. Active edge channels have the same leakage currents as interior ones. (Some recent runs have had higher leakage currents, possibly due to an iron-contaminated furnace tube.)

4. 4. A new feature, active edges, has been developed, bringing full sensitivity to within several microns of the physical edges.

5. A new kind of sensor has been fabricated and tested : planar / 3D – active edges. It has planar electrodes on the top surface, a single opposite-type implant on the bottom, and a 3D electrode on its edges which is continuous with the bottom. It has edge properties similar to those of full 3D sensors, with no dead volume anywhere inside, but without the speed or radiation hardness of full 3D.

6. Production of planar / 3D – active edges sensors for TOTEM should start this year.

7. NIH sensors are made using the same technology as TOTEM and will share the same wafer.

8. An R&D fabrication run of full 3D sensors for the ATLAS pixel B layer replacement, for the ATLAS pixel upgrade, and for FP420 is now underway.