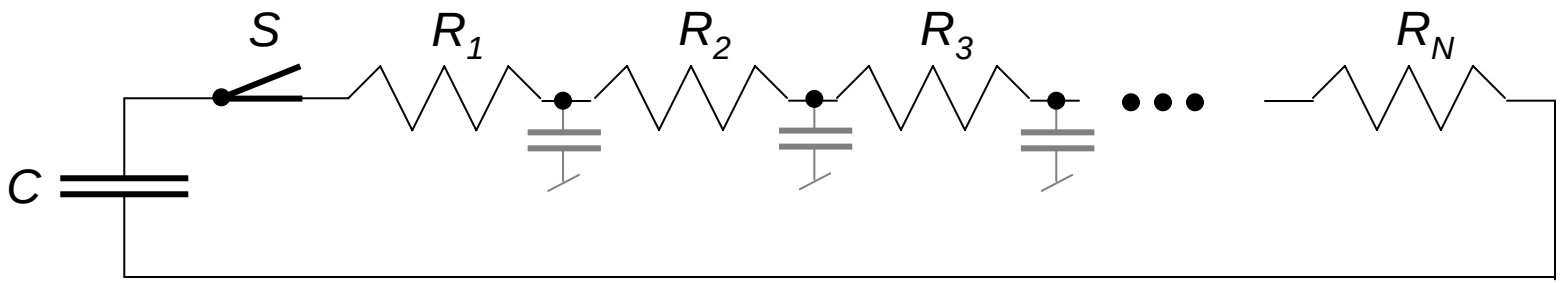
How to Design an Integrated Circuit

IC *design* is detailed and meticulous (i.e. not cheap)
IC *fabrication* is also not cheap
No user serviceable parts inside – the chip works or it doesn't
So why do we do this at LBL?
Is IC design really sorcery?

- History and Motivation
  - What's a circuit
  - What's an integrated circuit
- IC design process
- Our friend the MOS transistor
- Let's make a chip
- Examples
- Trends

P. Denes
Engineering Division

Circuit Problem ca. 1750

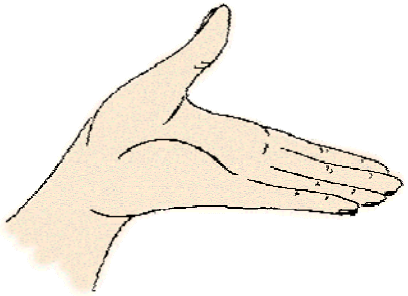


Charge capacitor ***C***
Close switch ***S***
Estimate propagation time through this transmission line
N ~ 1000

Solution

R_1 .. R_{1000}

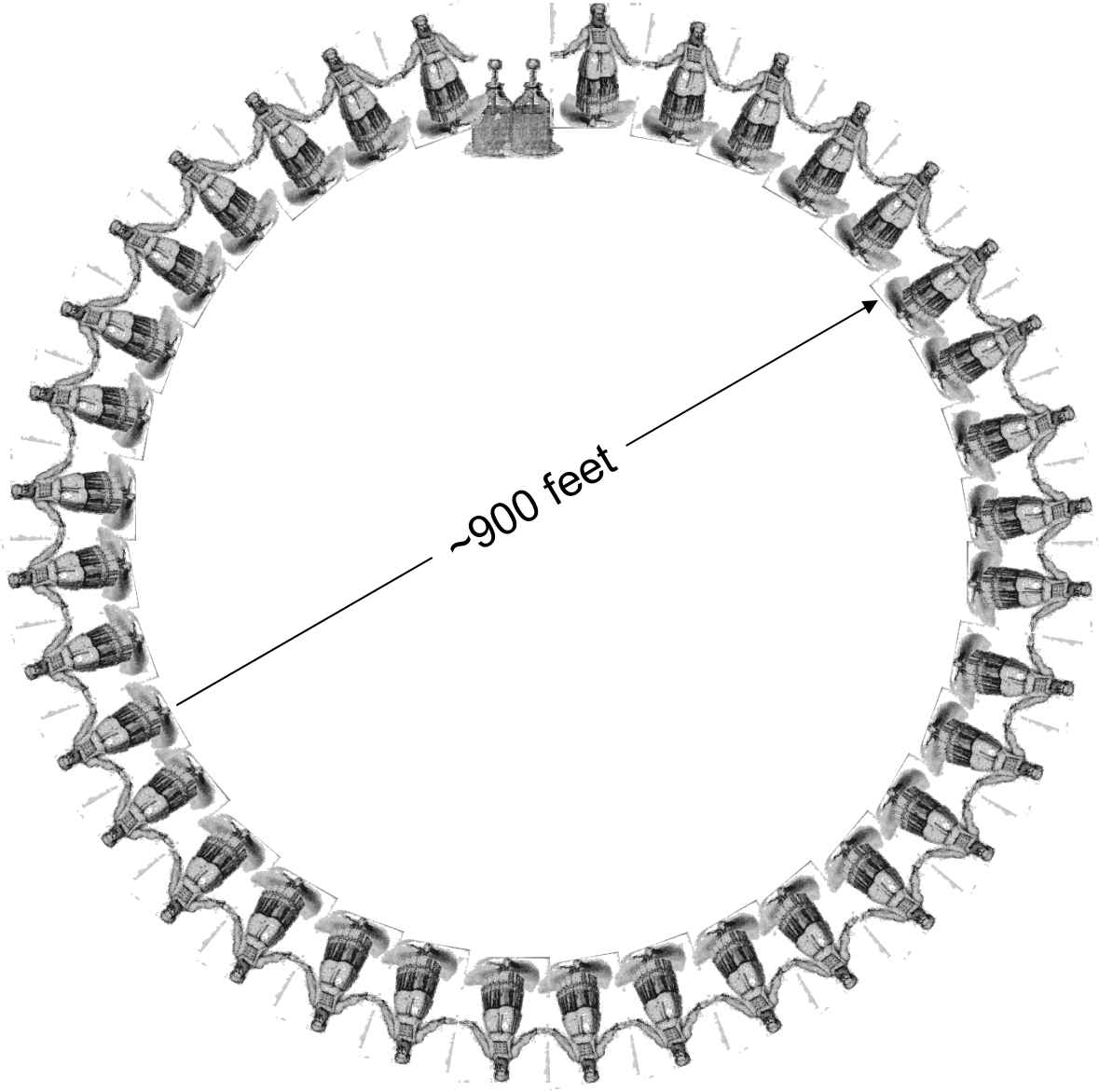
C



S

French physicist Abbe Nollet
Components used:
1000 Carthusian monks
Capacitor based on design from University of Leyden
Resistive contact to C

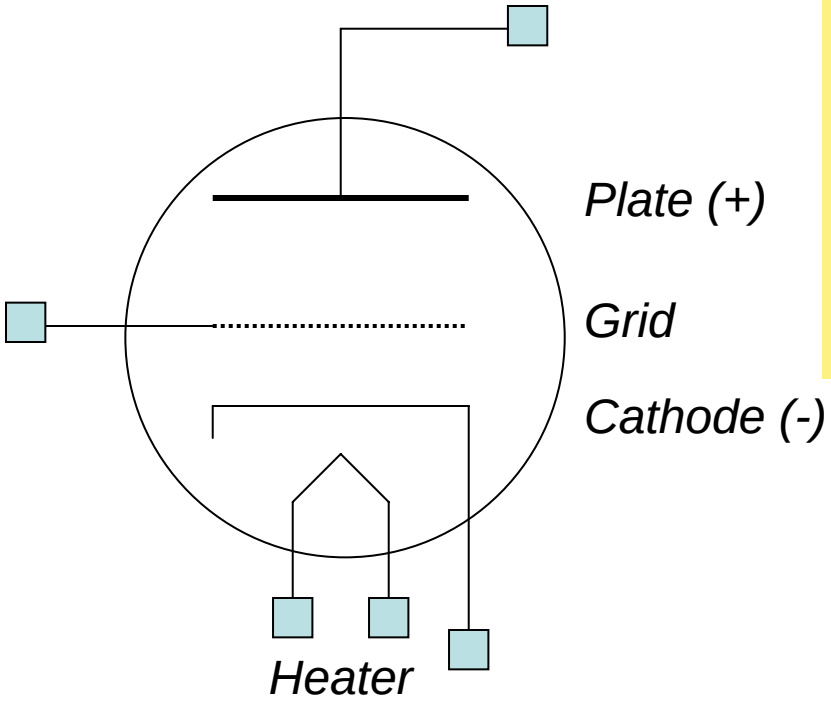
Circuit Layout

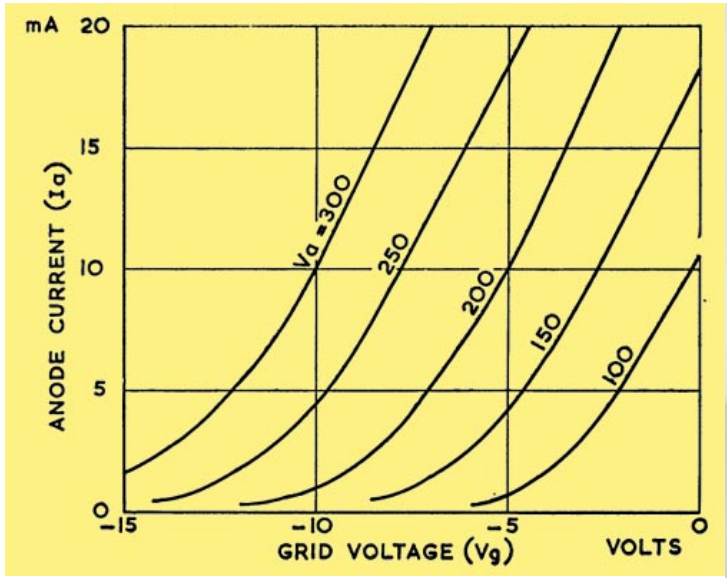


- Simultaneous jumping of monks → "electricity is fast"
- Circuit composed of well-defined, discrete parts connected together
- (Circuit dimensions are a bit large)

Fast Forward → 1906

Triode
Lee de Forest





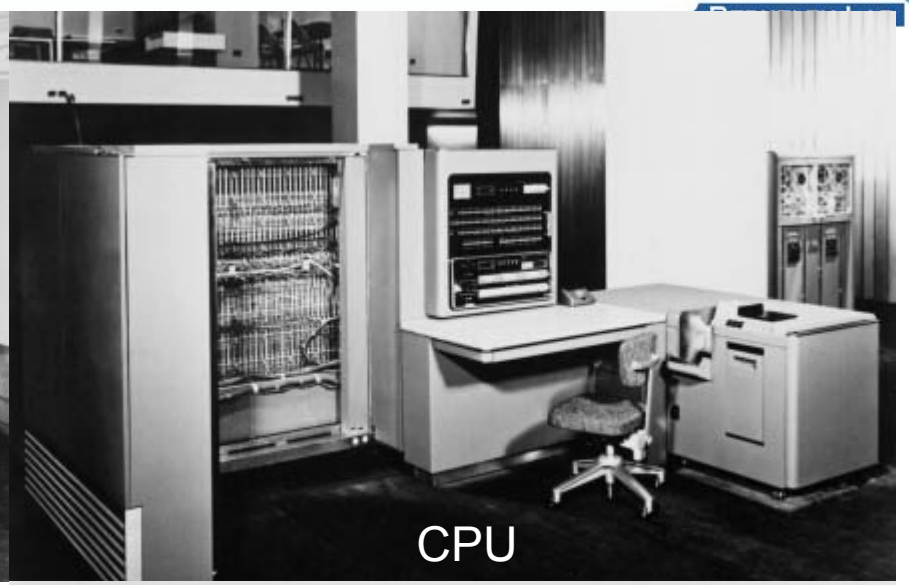
- Grid modulates conduction
- Can be used for analog applications
- Can also be used for digital applications

ENIAC – 1945, U. Penn.

Designed to calculate ballistic ordnance firing tables
Electronic Numerical Integrator And Computer

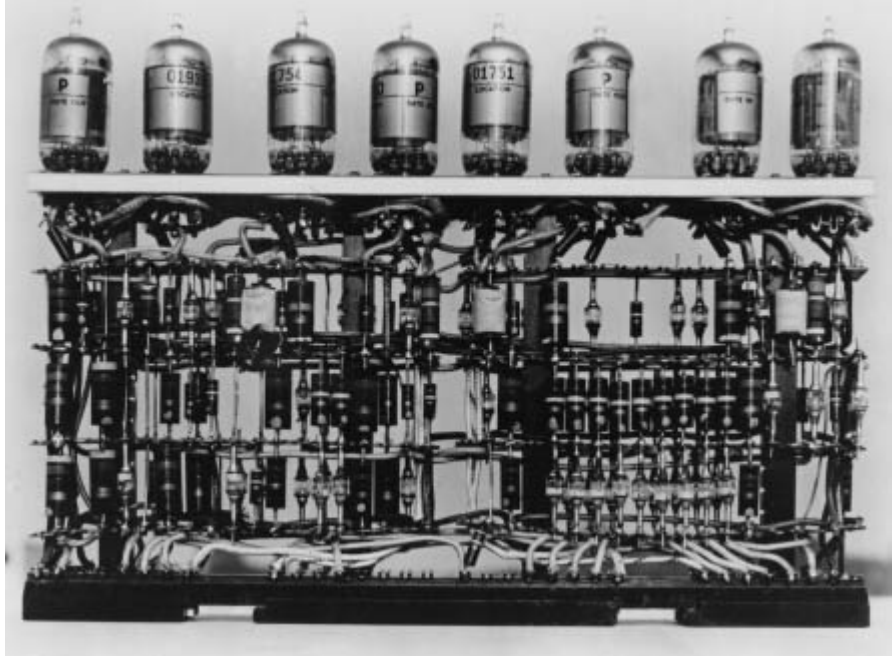
Its thirty separate units, plus power supply and forced-air cooling, weighed over thirty tons. Its 19,000 vacuum tubes, 1,500 relays, and hundreds of thousands of resistors, capacitors, and inductors consumed almost 200 kilowatts of electrical power.

IBM 701 -1952

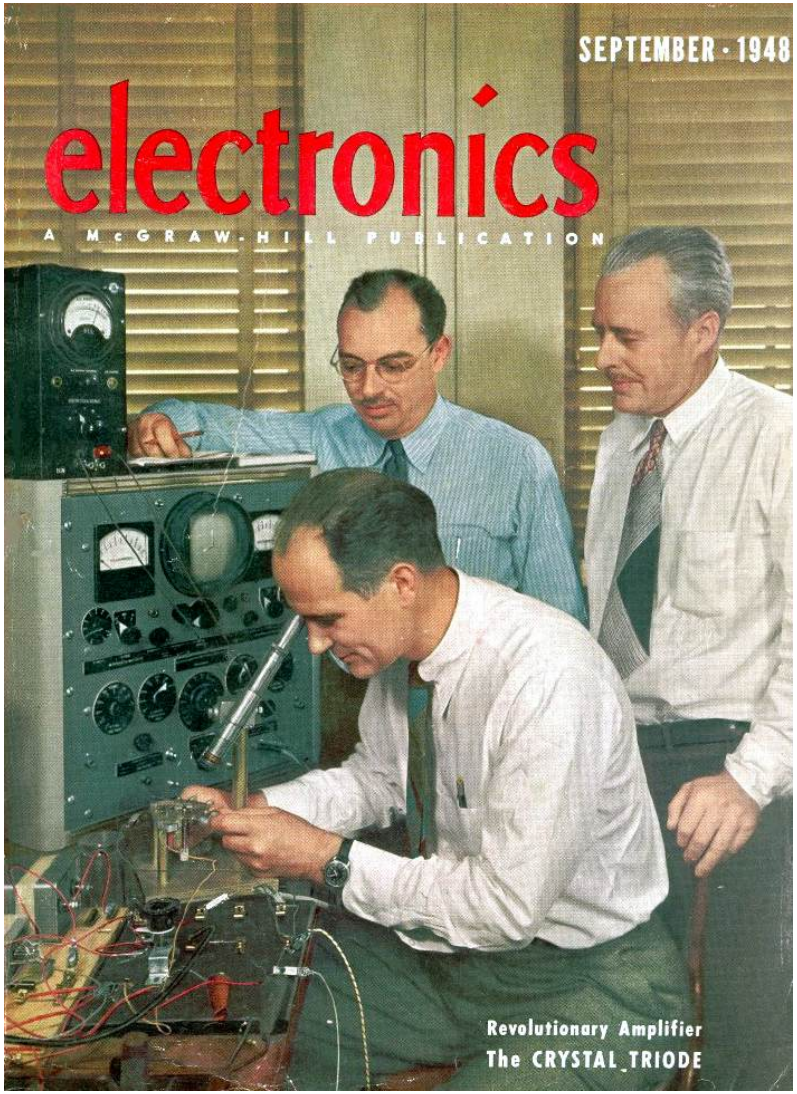


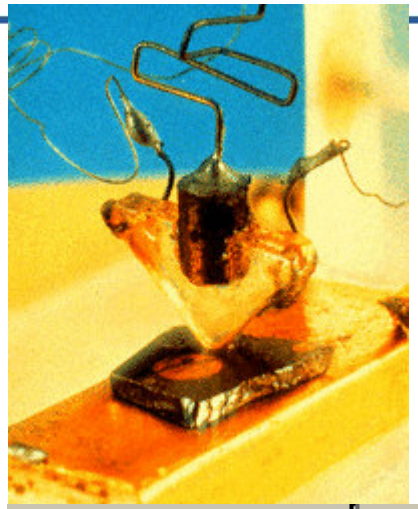
16 kHz cycle
2k words fast storage
1st computer for scientific work

Modular circuit assemblies of components



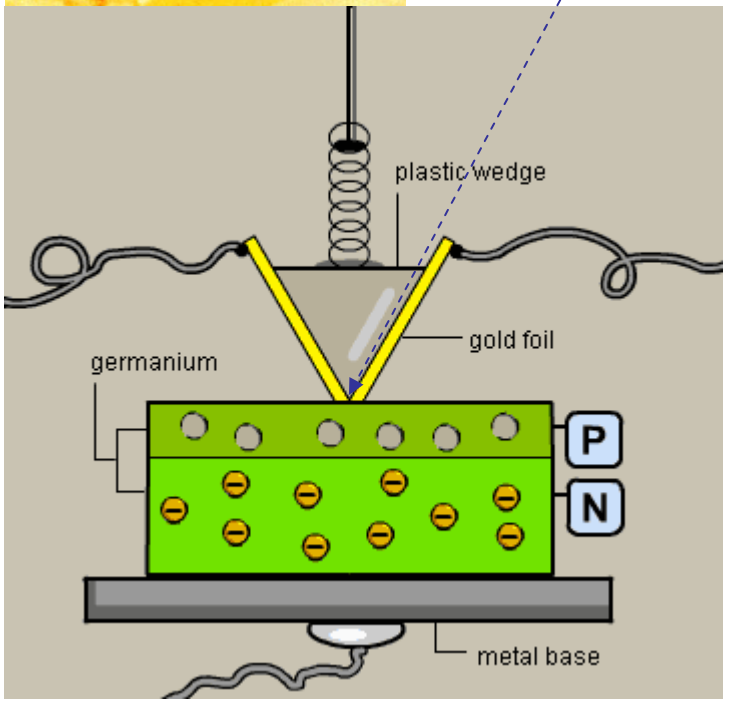
The solution?





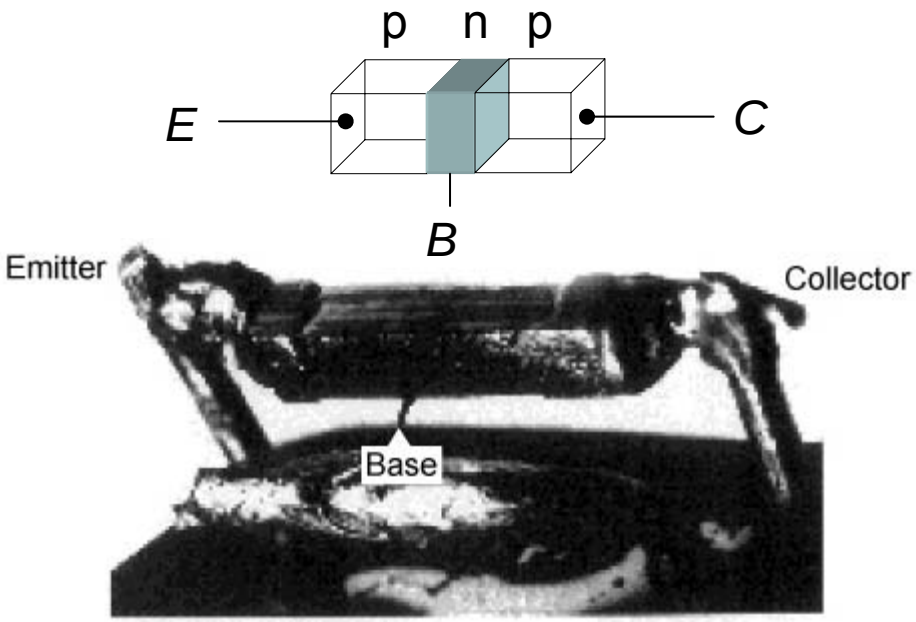
Point contact transistor

Thin razor cut



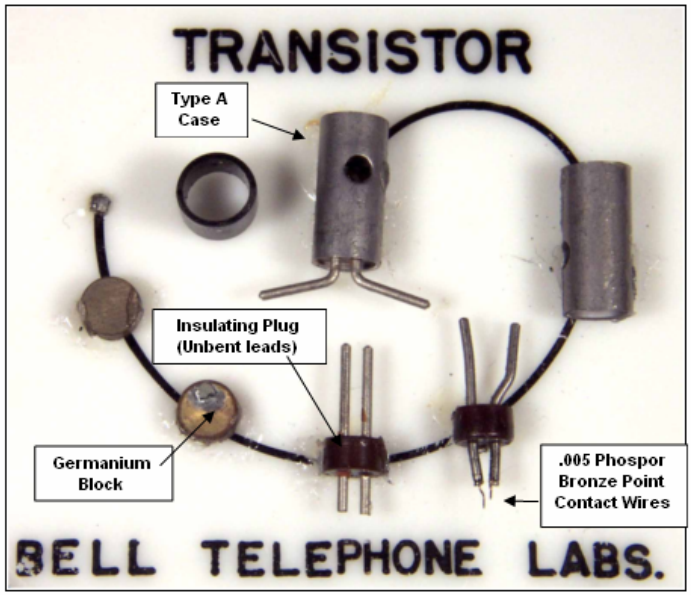
Almost

- Point contact transistor is a surface effect device (and surfaces are easy to contaminate – not to mention paper clips can be mechanically unstable)
- Schottky contacts, rather than pn junctions
- Shockley junction transistor (1949)



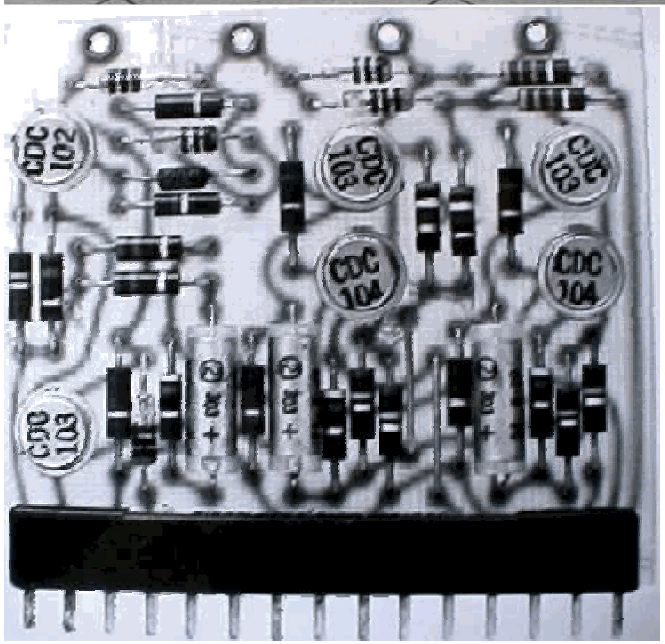
Ge

Although the point contact transistor did live for a while



CDC 1604/160 - 1960

160 kHz cycle
32k words fast storage



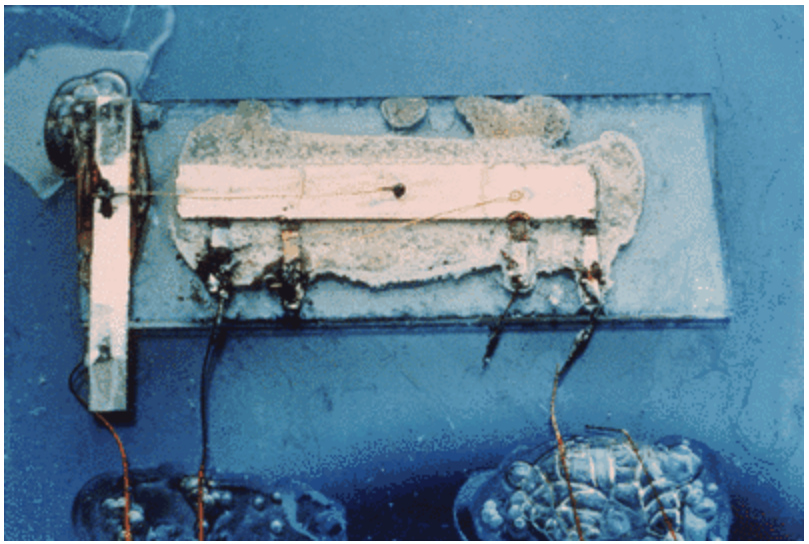
Modular circuit assemblies of components

The first desktop (literally)

Integrated Circuits - 1958

Jack Kilby
Ge
(1 transistor)

Texas Instruments
(Patent)

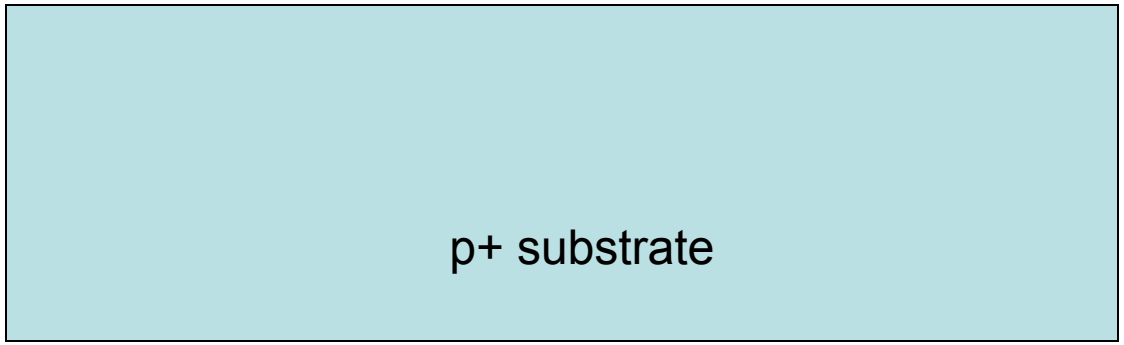


Legal wrangles
Resolved in mid-60's

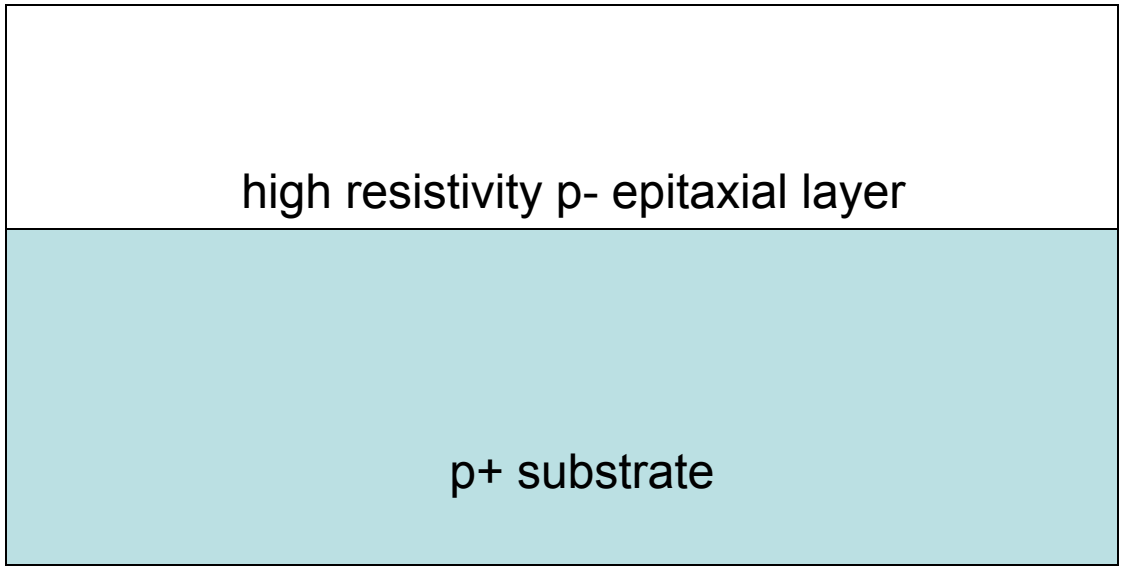
Robert Noyce
Si
(2 transistors)

Fairchild
(Patent)

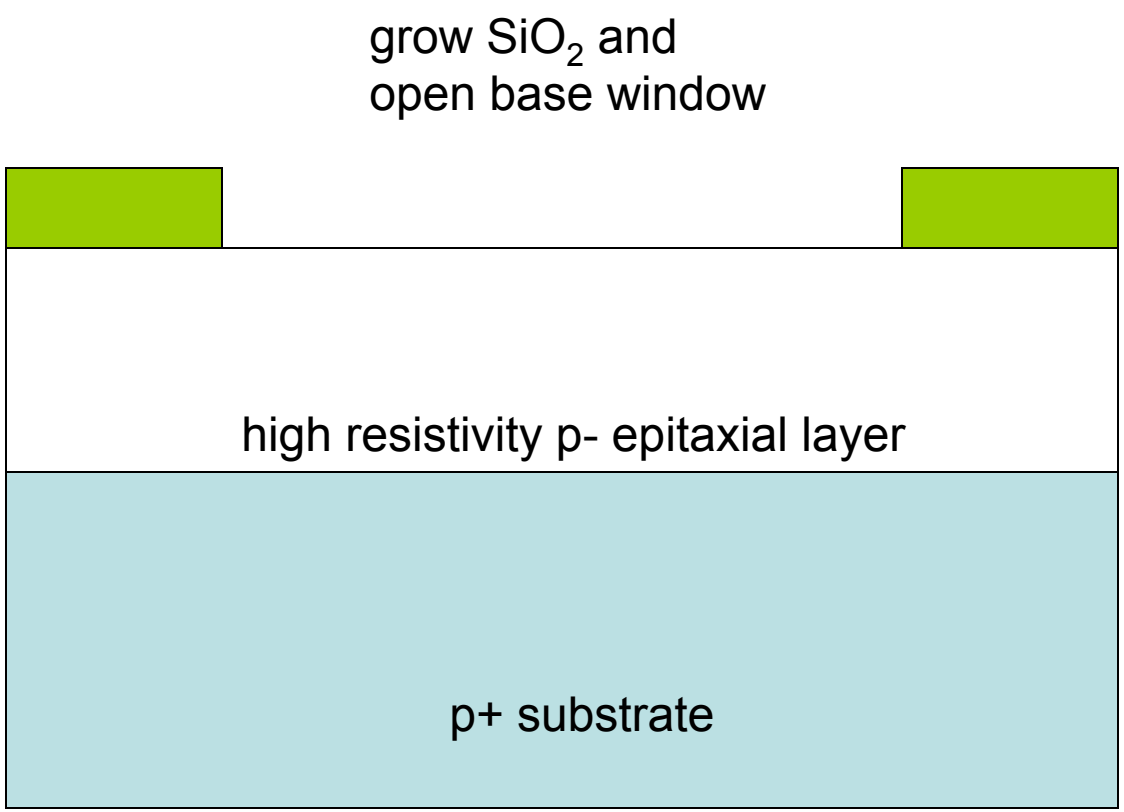
Early Circuits – Planar Bipolar Process



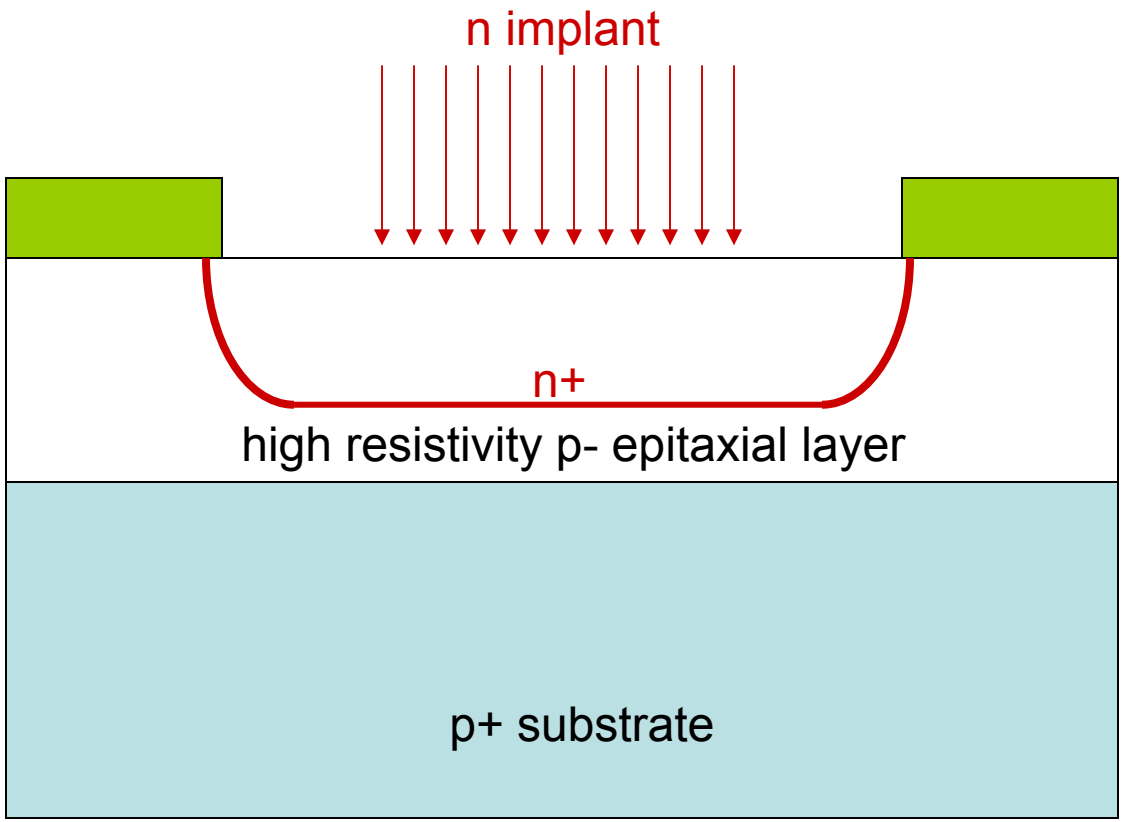
Early Circuits – Planar Bipolar Process



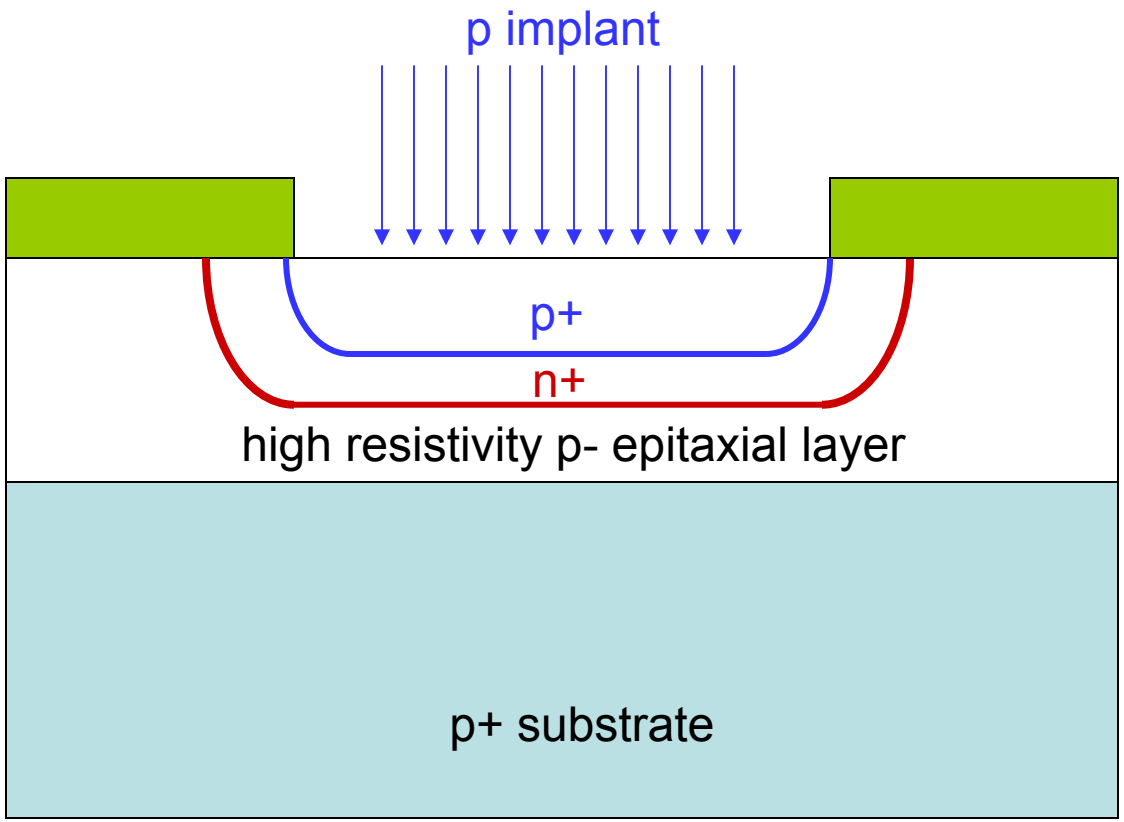
Early Circuits – Planar Bipolar Process



Early Circuits – Planar Bipolar Process



Early Circuits – Planar Bipolar Process



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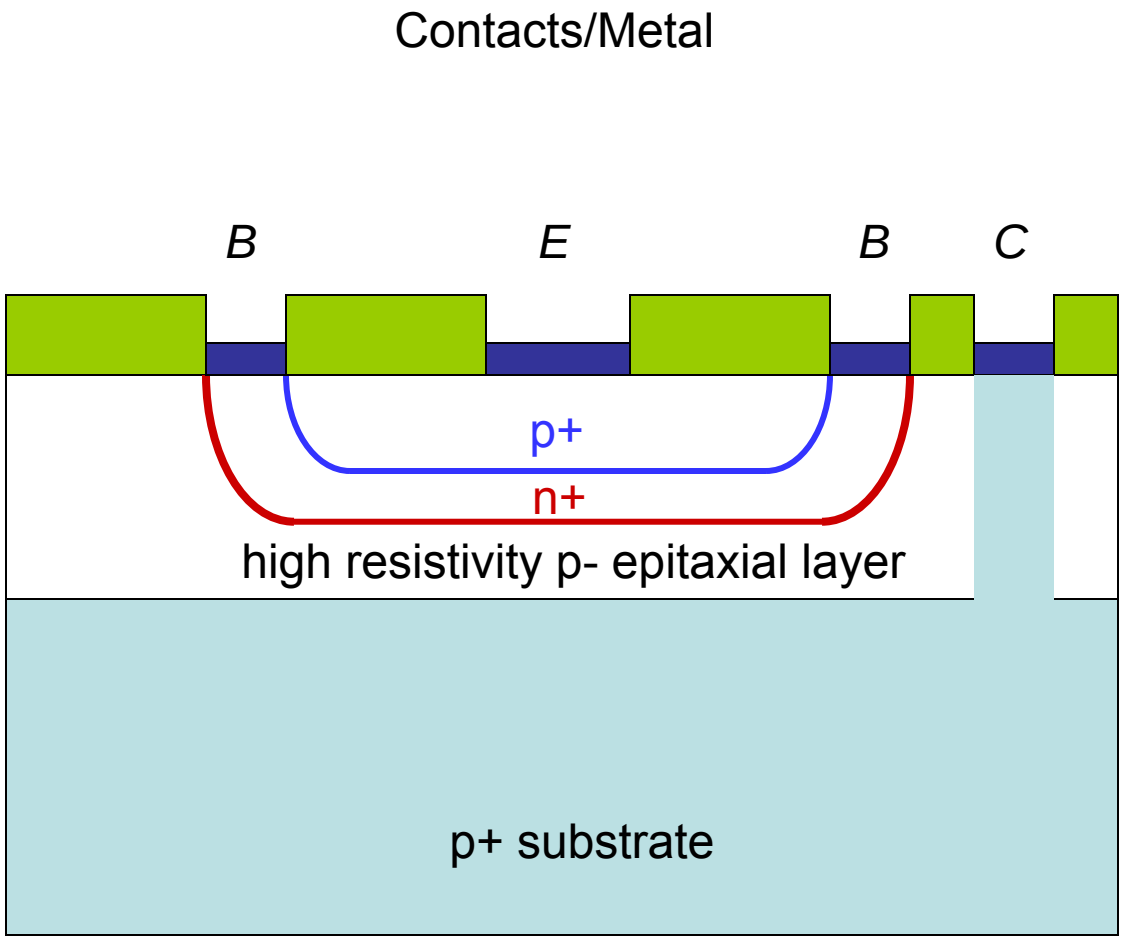
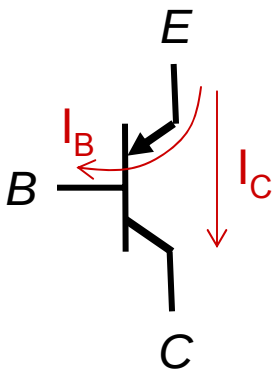
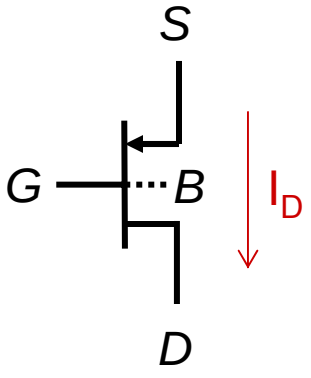


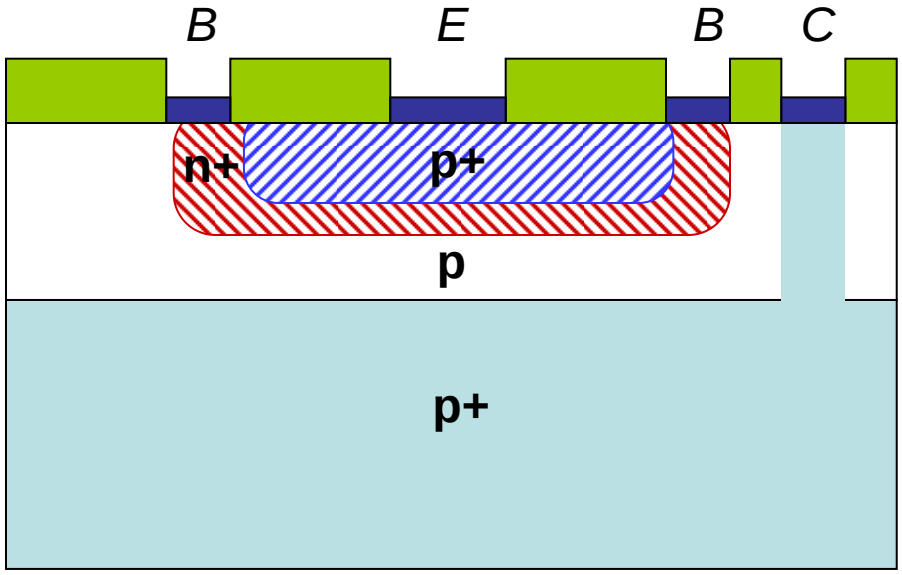
Bipolar Junction vs. Insulated Gate Transistors

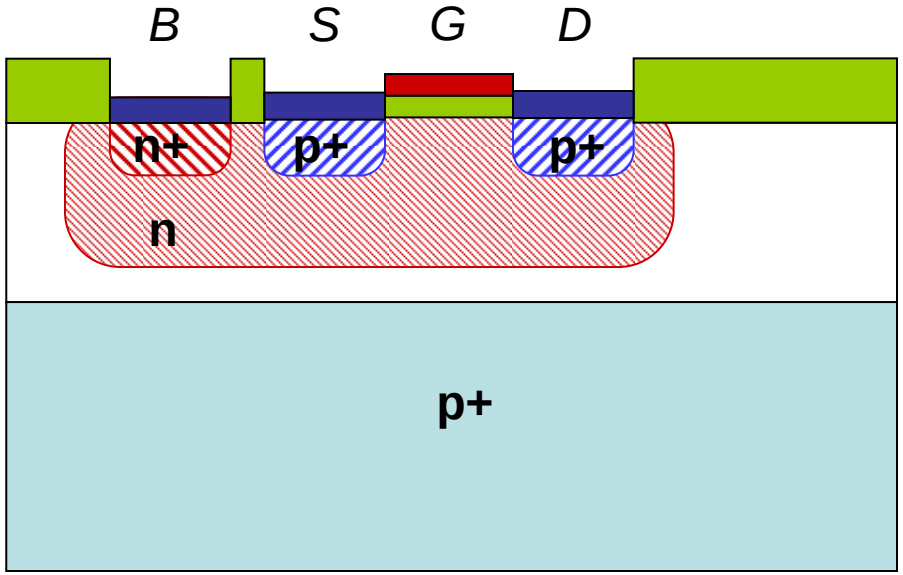


$I_C \sim \beta I_B$
$I_B \sim \exp(V_{BE}/kT)$



$I_D \sim (V_{GS} - V_T)^2$ $V_{GS}>V_T$
$I_D \sim 0$ $V_{GS}<V_T$



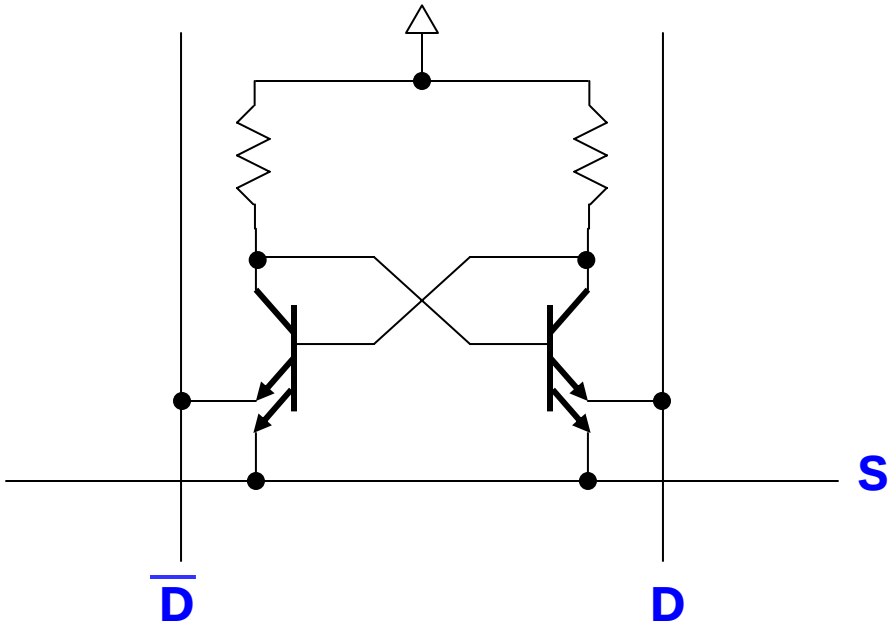


1st MOS on Si - 1960

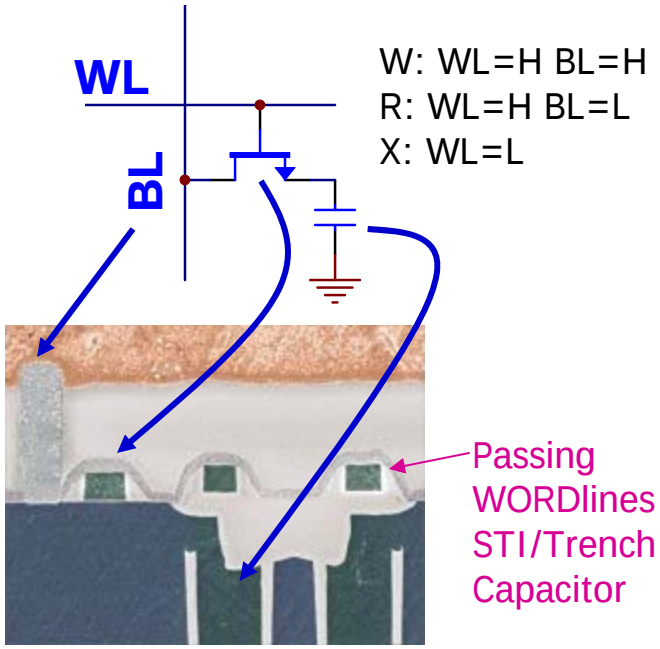
MOS and CMOS take over

- Early circuits were mostly bipolar (especially analog)
- MOS took hold for memory
- CMOS invented in 1963, but took off (once fabrication became good enough) in the 80's

Bipolar SRAM



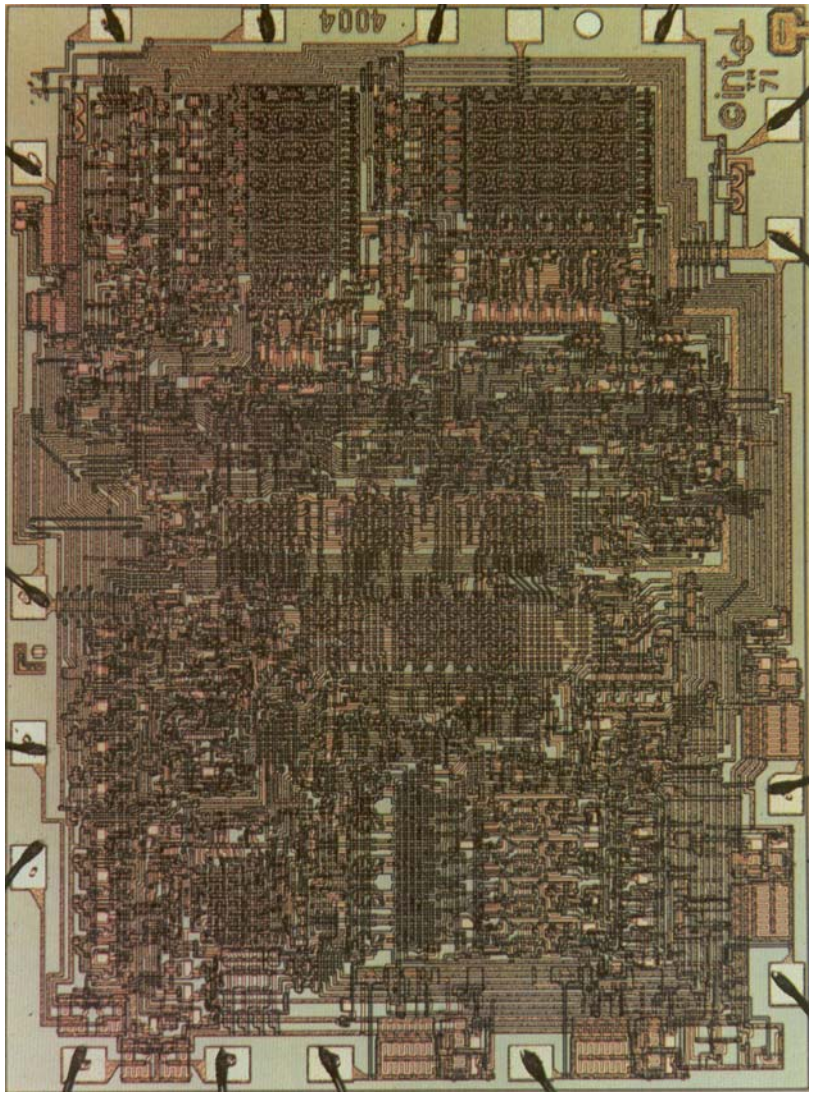
CMOS DRAM



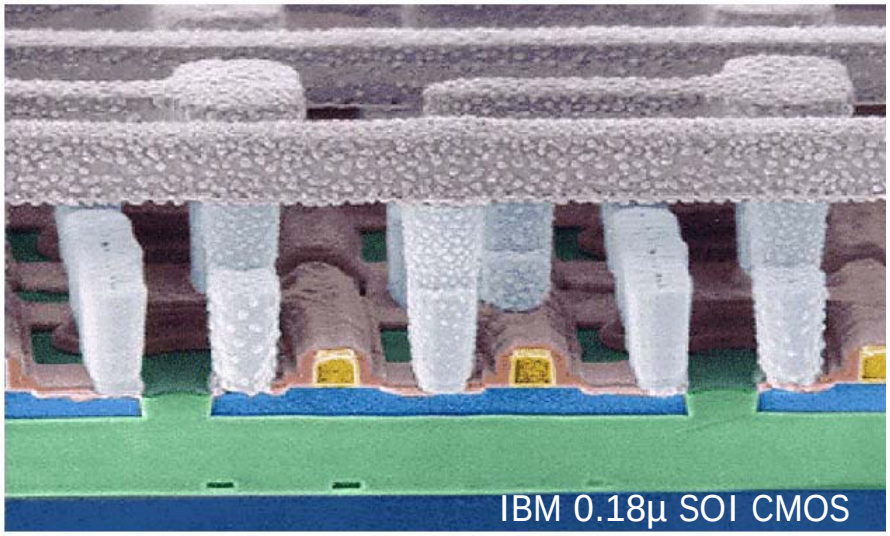
MOS logic – Intel 4004 - 1970

The first single chip CPU was the Intel 4004, a 4-bit processor meant for a calculator. It processed data in 4 bits, but its instructions were 8 bits long. Program and Data memory were separate, 1K data memory and a 12-bit PC for 4K program memory (in the form of a 4 level stack, used for CALL and RET instructions). There were also sixteen 4-bit (or eight 8-bit) general purpose registers.
The 4004 had 46 instructions, using only 2,300 transistors in a 16-pin DIP. It ran at a clock rate of 740kHz (eight clock cycles per CPU cycle of 10.8 microseconds) - the original goal was 1MHz, to allow it to compute BCD arithmetic as fast (per digit) as a 1960's era IBM 1620.

8 µm PMOS



Timeout - Glossary



Metal Interconnect

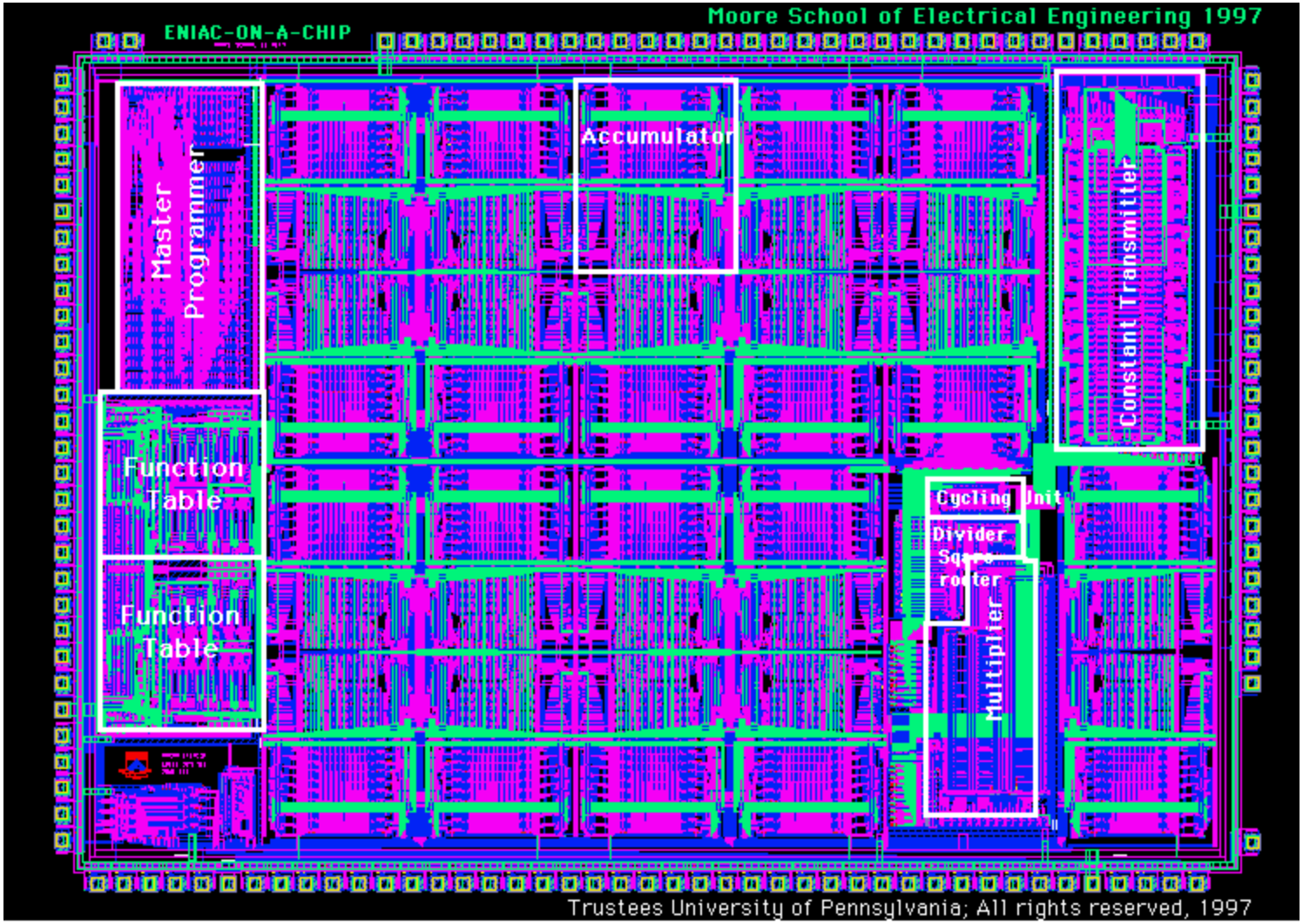
Metal Interconnect

Polysilicon gate

Process – the complete fabrication process which produces the integrated circuits. It includes photolithographic mask preparation, wafer preparation and processing, etc. The *process* defines for the designer what kinds of devices are available and what their performance characteristics should be

Feature size (or line width) – the smallest dimension which can be reliably lithographed. So a “1 µm CMOS process” contains N- and P-channel MOS transistors with 1 µm minimum feature size

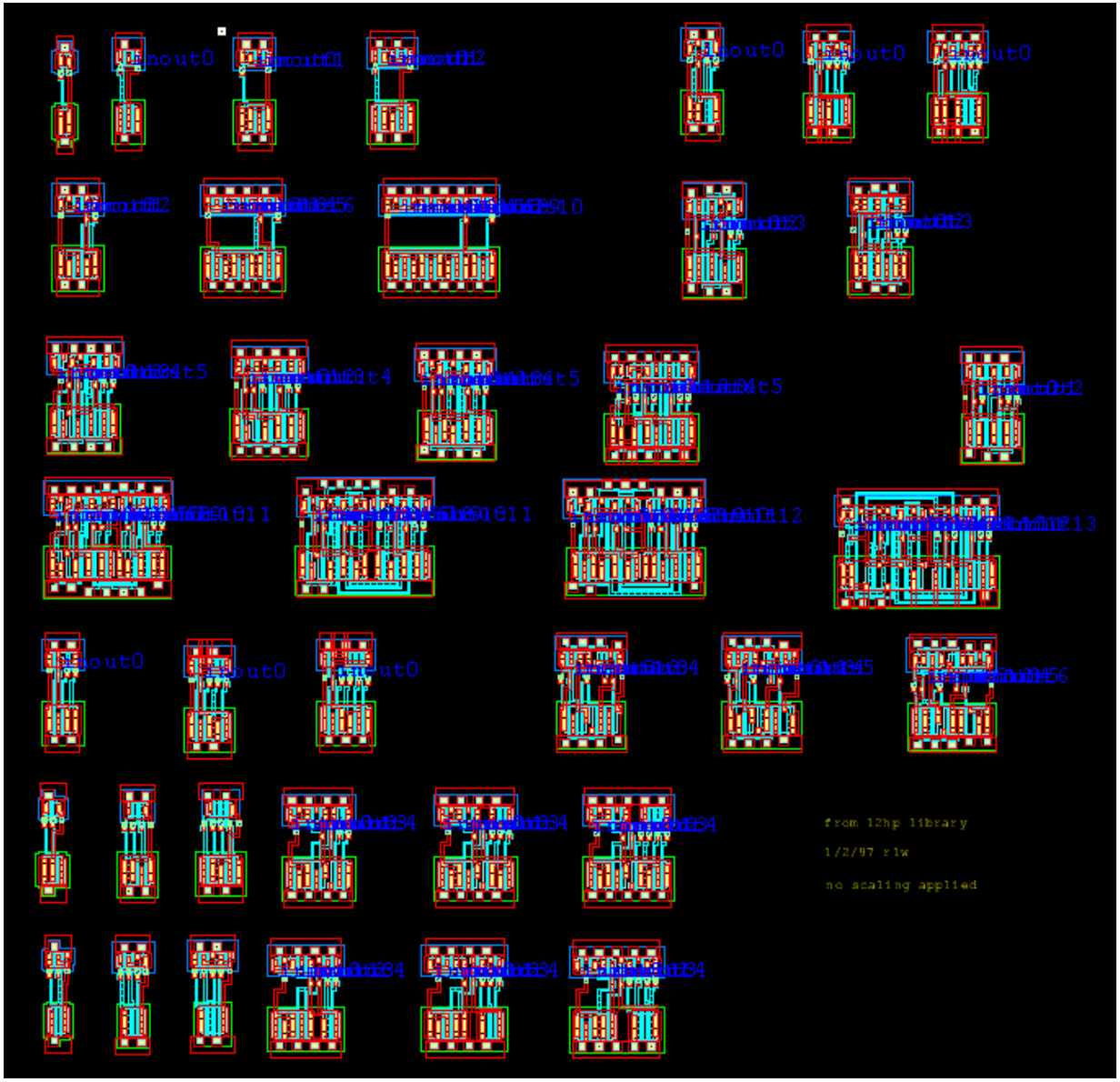
ENIAC – 50th Anniversary Edition



Size: 7.44mm x 5.29mm; 174,569 transistors; 0.5 um CMOS technology (triple metal layer).

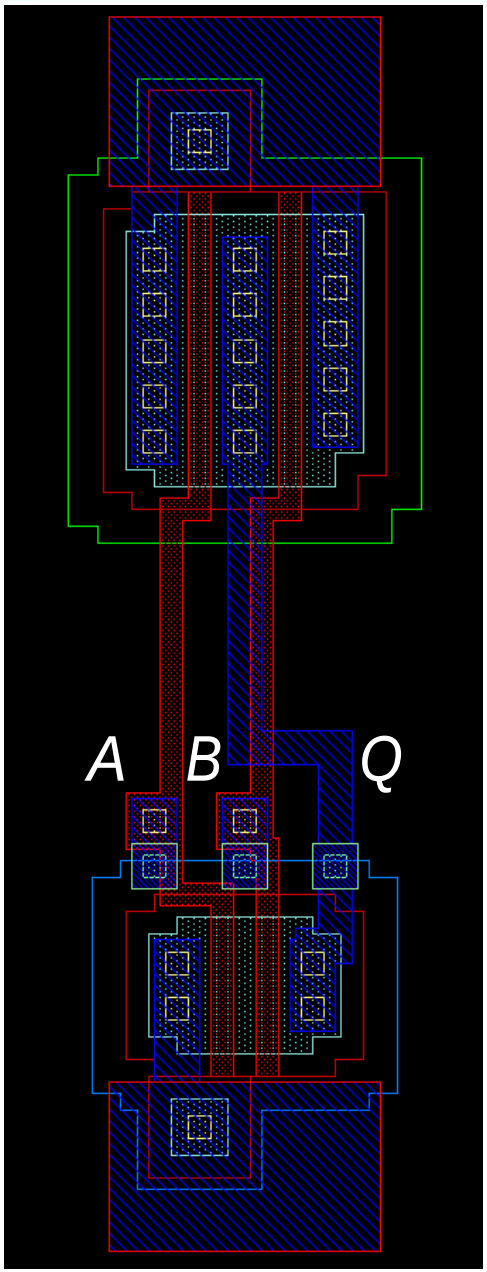
30 mg vs 30 tons

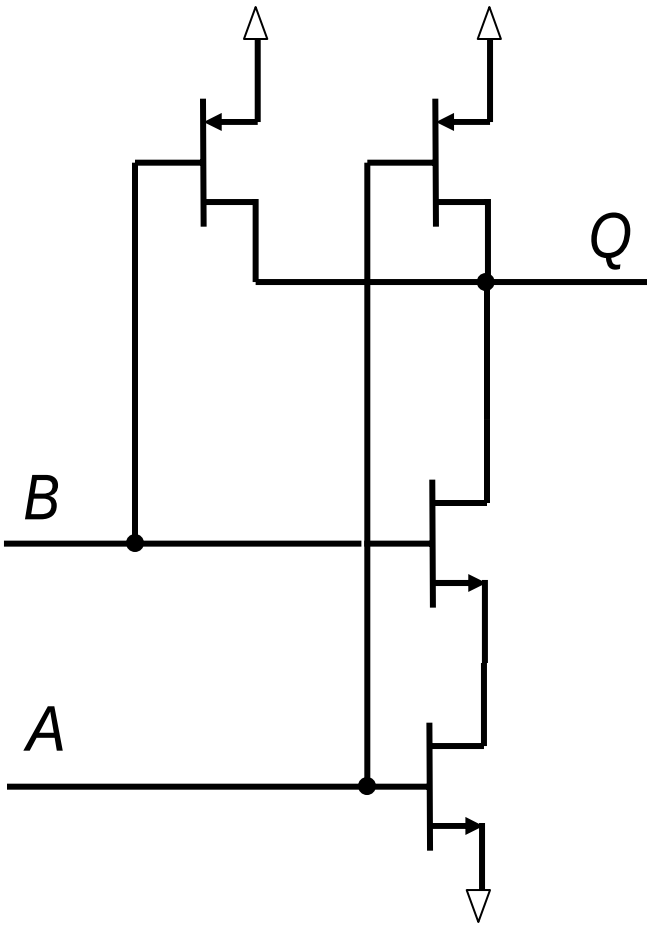
Digital Standard Cells

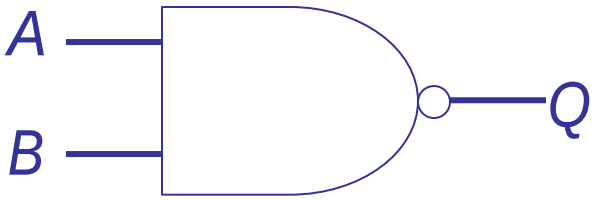


- Predefined logic gates (“cells”) - Circuit composed of well-defined, discrete parts connected together
- write a *description* (program) of the logic functions
- *synthesize* the design (using the library)
- *place* and *route* the design

For example







But This Is *Not* What We Do

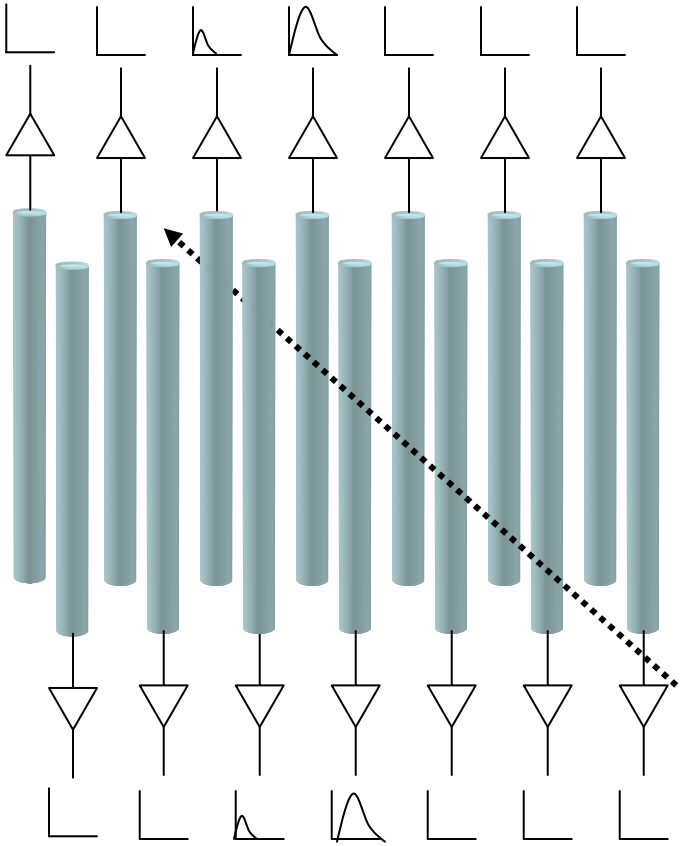
We do mixed-mode design - analog functions, supported by digital logic.
The analog functions are full custom: design the circuit at the transistor level, and design/optimize each transistor for the given function. This is not assembling a collection of pre-defined modules.

Timeout - Glossary

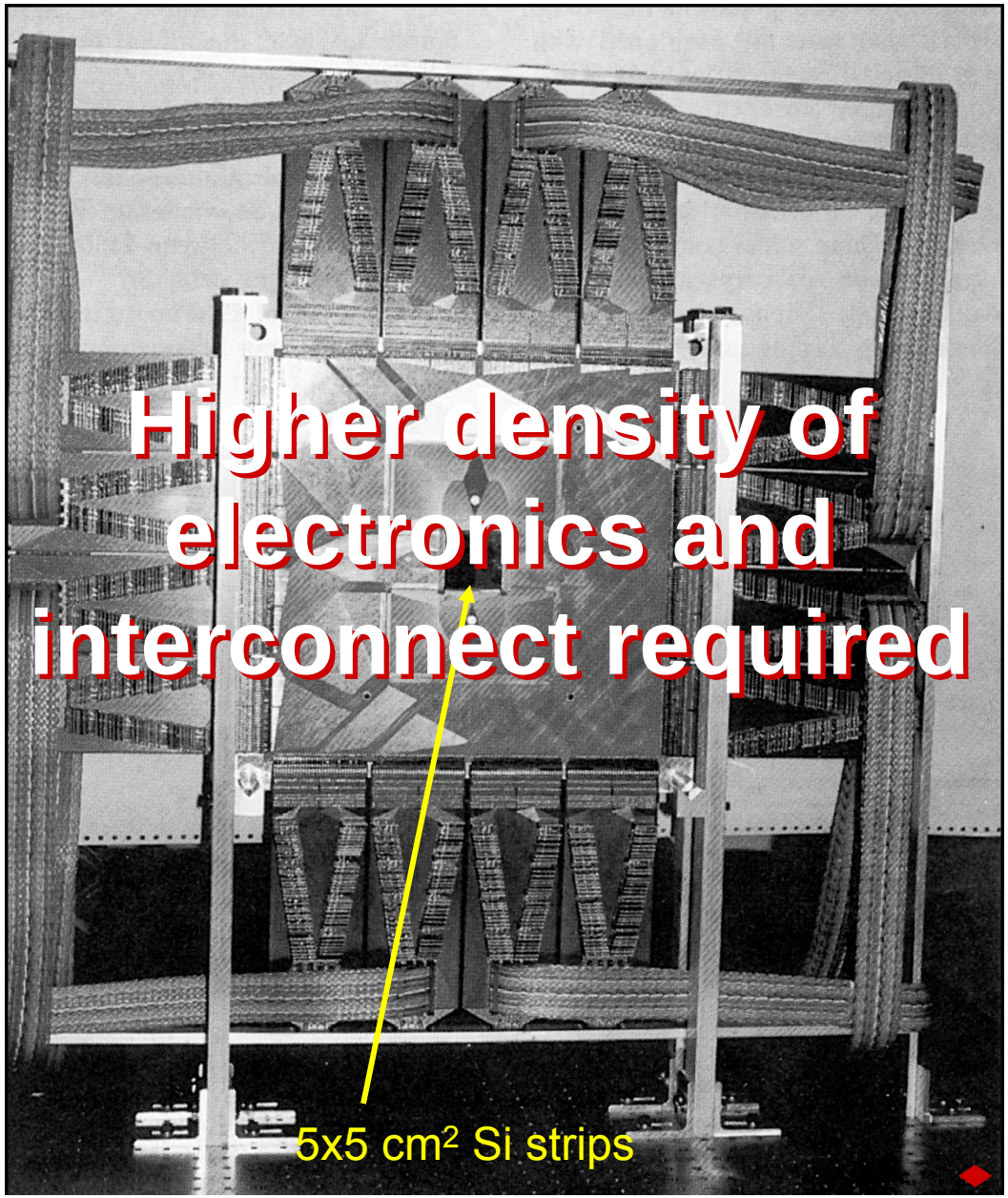
Full custom design means that we draw each transistor. What we can adjust are the width (W) and length (L) of the channel. For a given **process**, the transconductance ($\partial I/\partial V$) and capacitance depend on W, L and the process parameters.

Why do *we* do this?

Particle Tracking Detectors

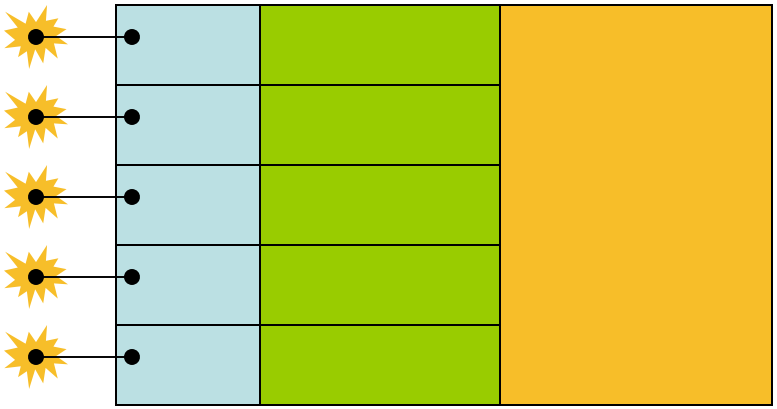


High rate fixed target experiments in the ’80s (NA11, E706, …) needing finer granularity (to reduce occupancy)



What we do

- Design custom ICs, typically in support of lab programs
- Generally, these ICs have many channels and are connected to some sort of sensor, transducer, … at the front-end, do some sort of signal acquisition/processing, and send information, usually digital, off the back end of the chip

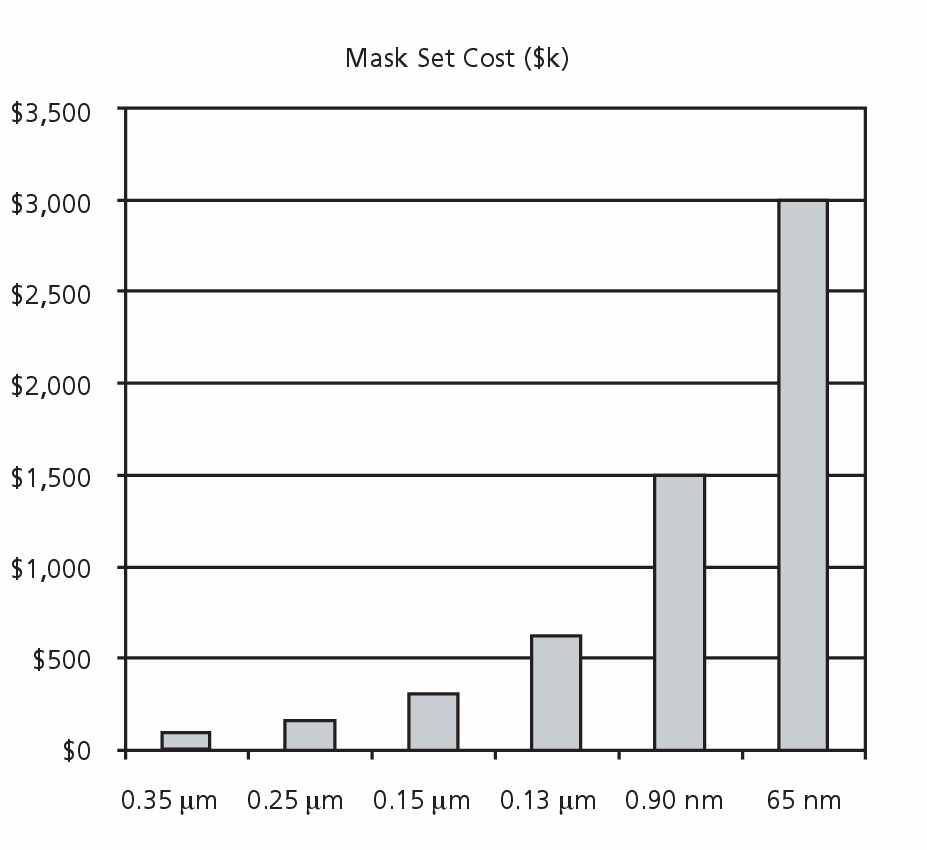


Analog FE "Conversion" Digital BE

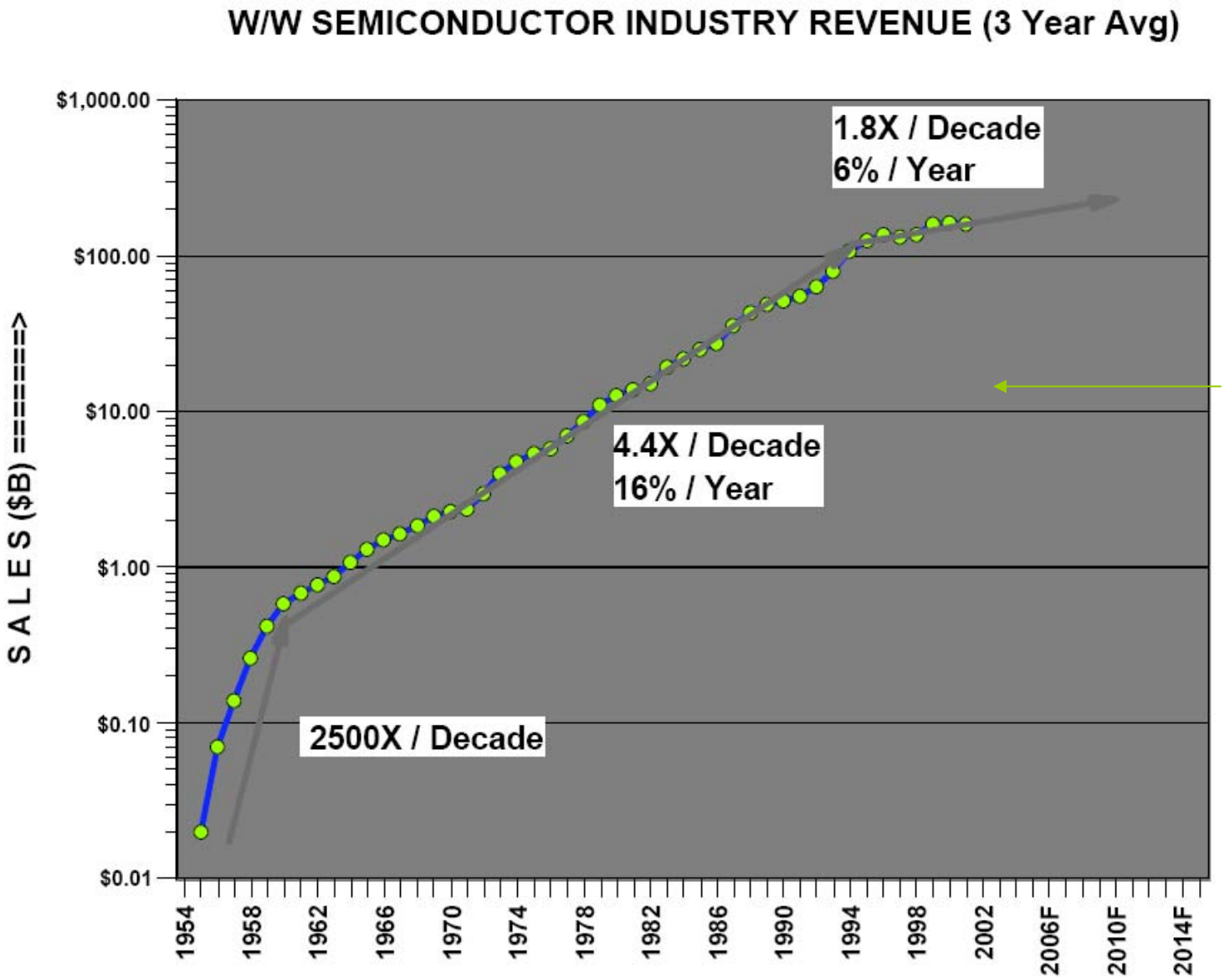
- We conceptualize the design, implement it electrically and produce the data needed to prepare the masks
- We *don't* actually fabricate the ICs – we use commercial IC processes

Commercial Processes

- Mask sets for modern technologies are very expensive (so we don't work at the cutting edge)
- One wants to try ideas out first anyway, so we use "Multi-project" services (brokers, who assemble many people's projects onto one run)
- So our technology choices are limited

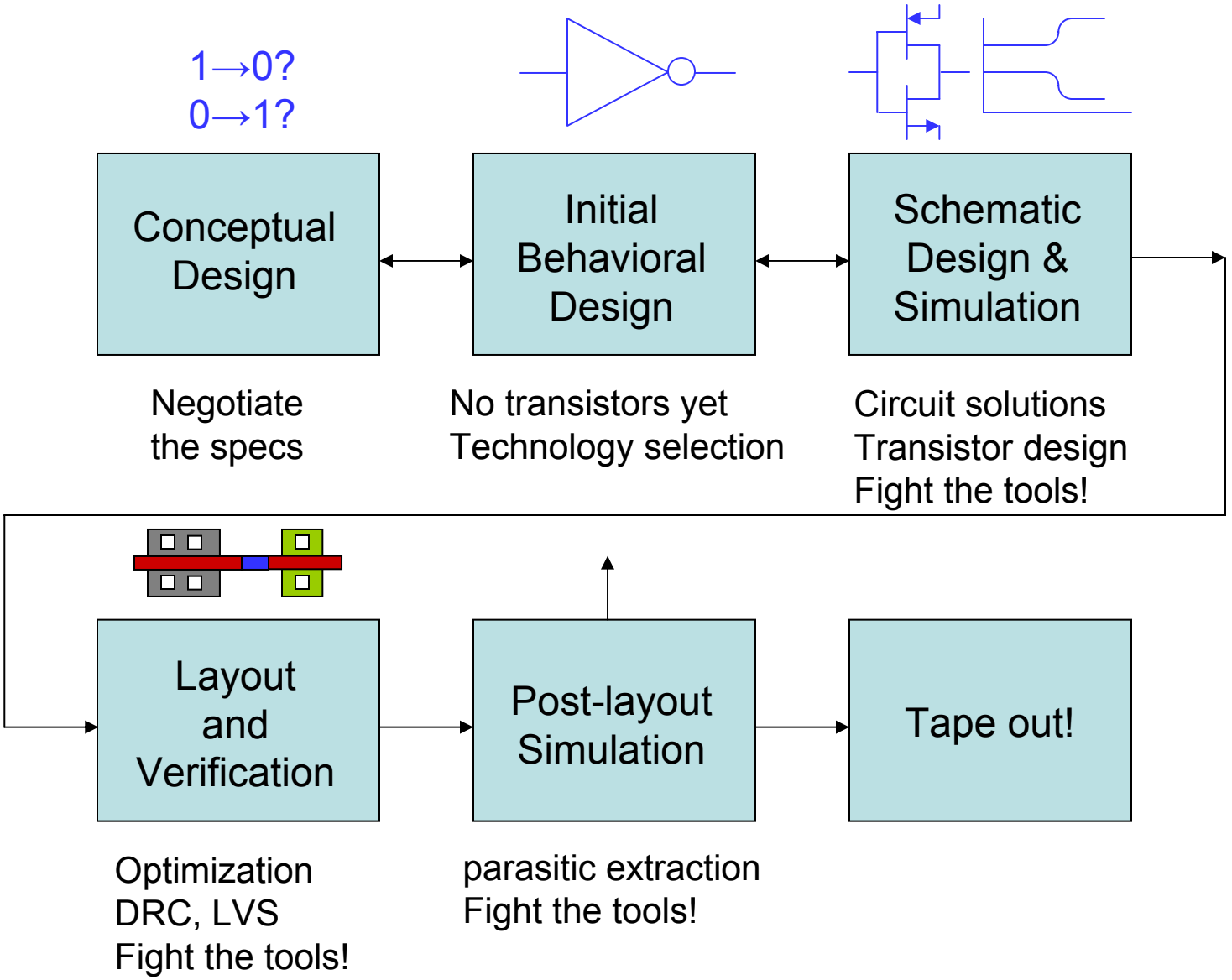


Large R&D Investment



2003 investment ~$14B (17% of sales). Recently, investment ~12-15% of sales…

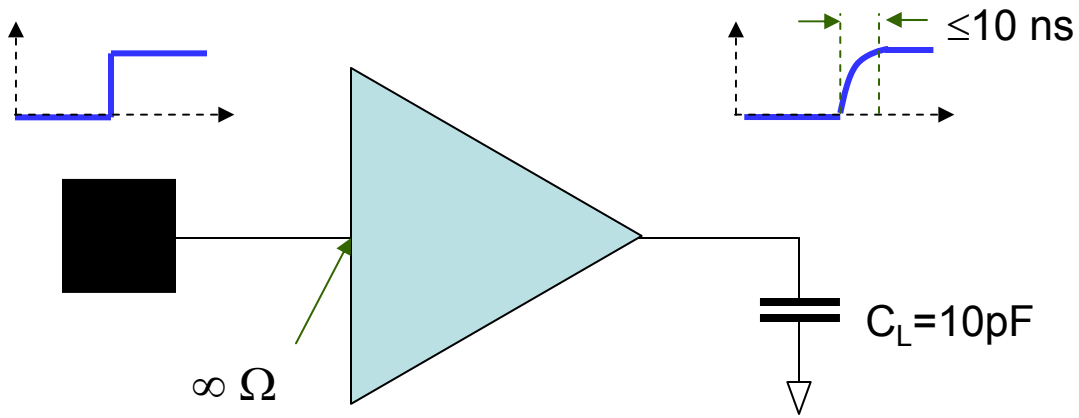
Steps in the IC Design Process



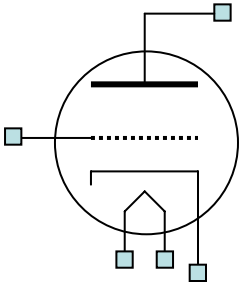
Let's Make A Chip

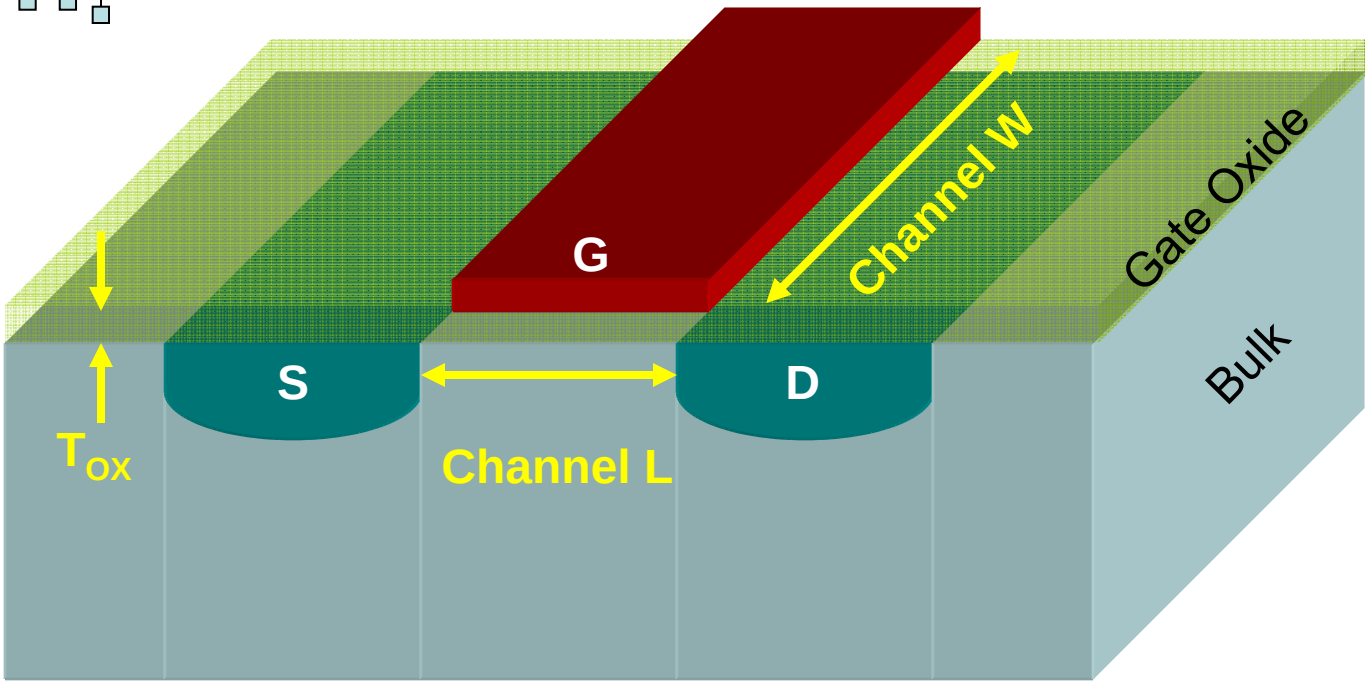
This will be a pretty banal example to fit within the time of this talk

- For a made-up application, we have a high-output-impedance sensor that needs a buffer amplifier. Specifications:
  - Drive an output load of 1 pF in less than 10 ns
  - Use no more than 1 mW
  - Be precise to >6 bits

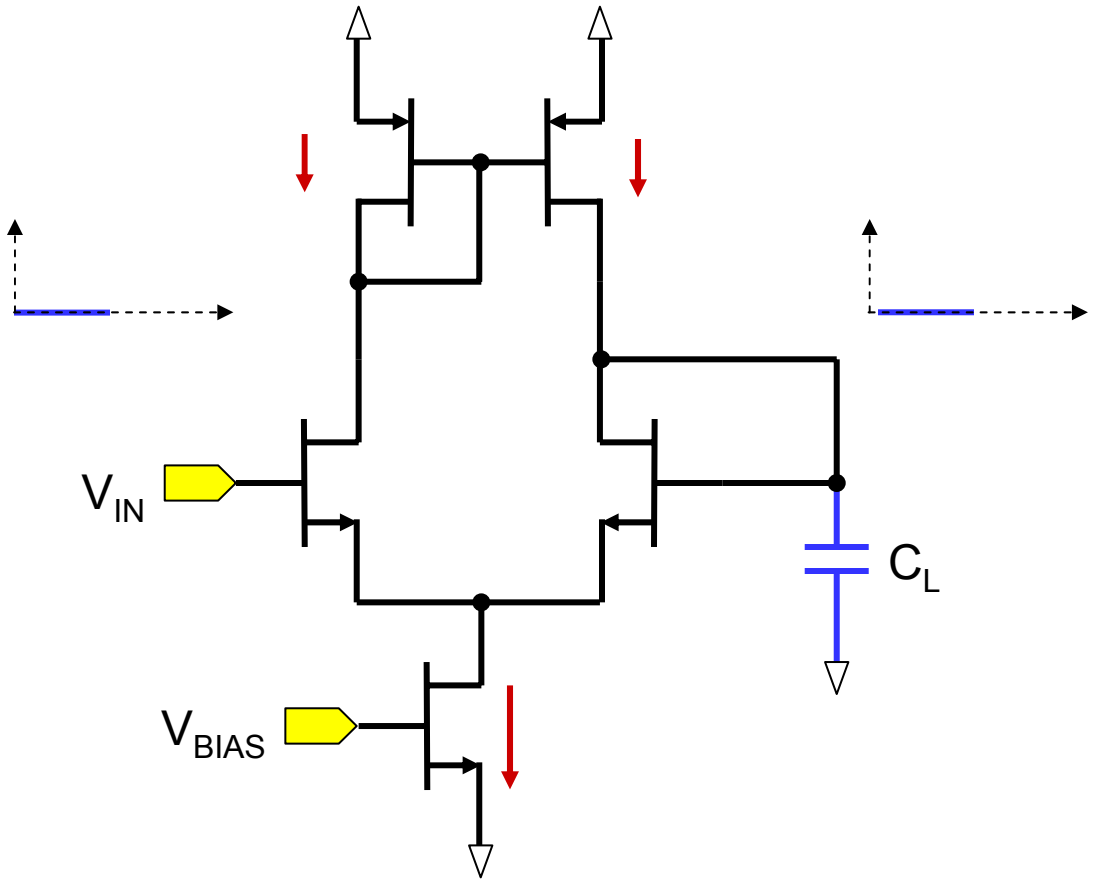


Our Friend the MOS Transistor

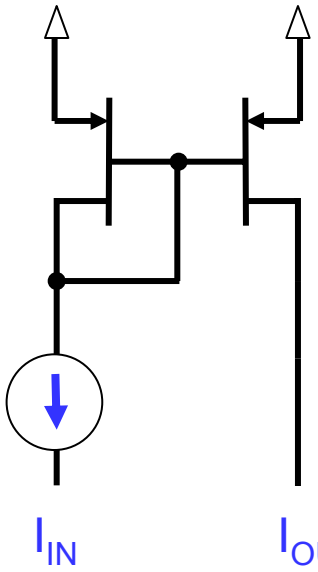




Design

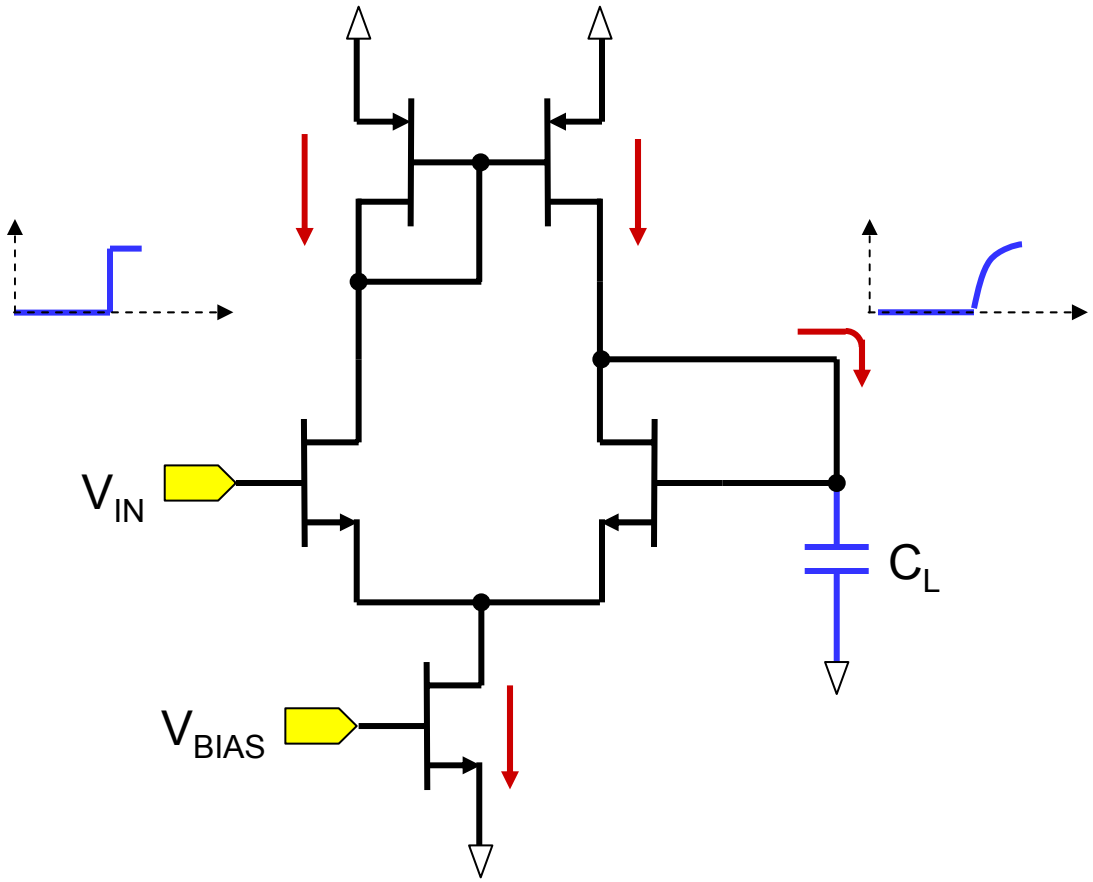


Current Mirror

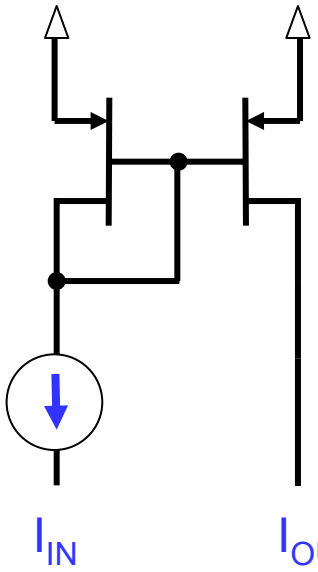


Same V_{GS}
Same current

Design



Current Mirror



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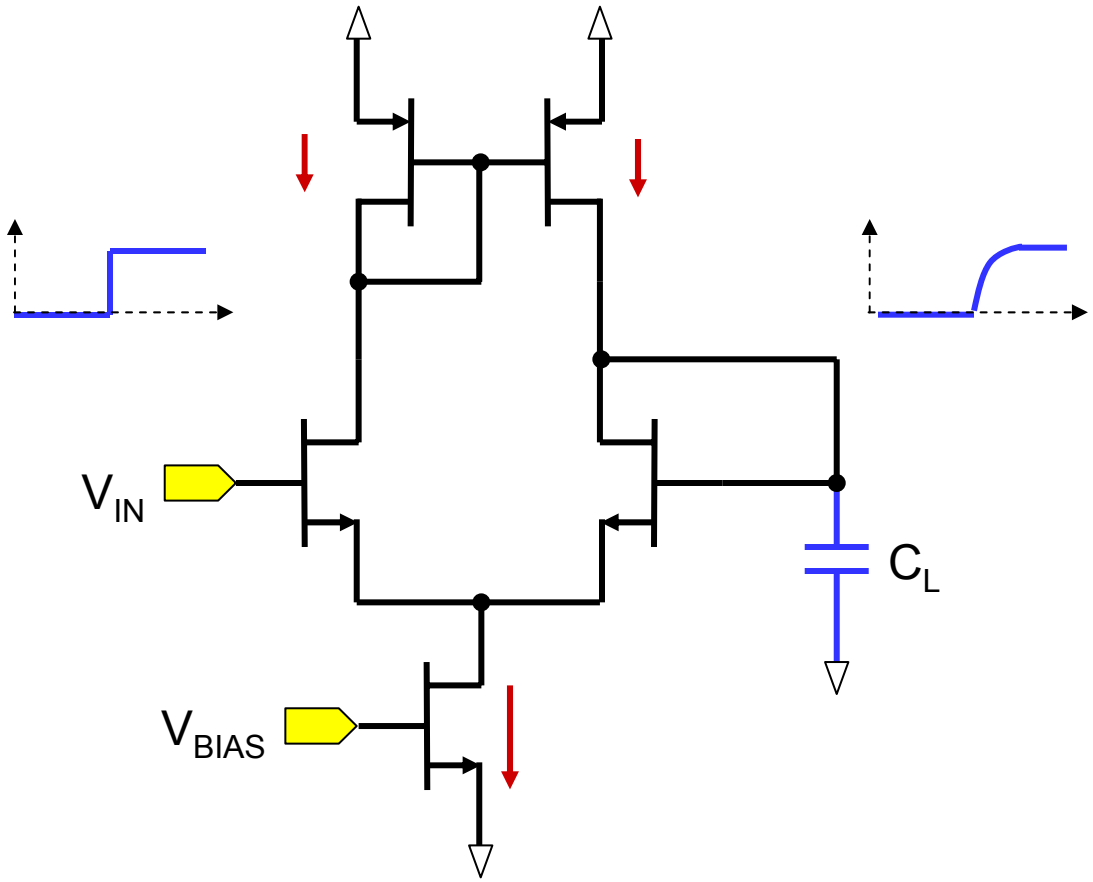
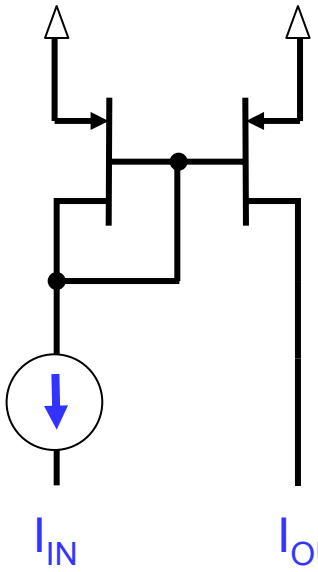
Design

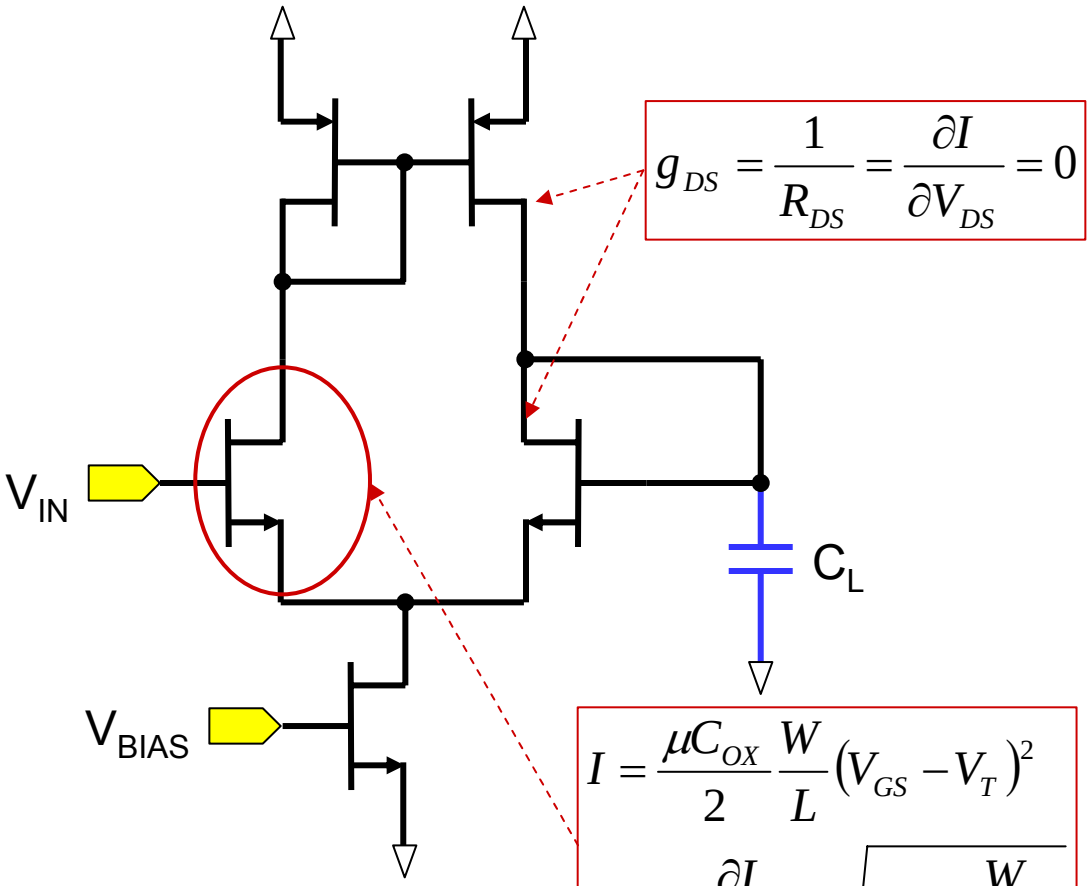


Current Mirror



Same V_{GS}
Same current

Hand Calculation



$\mu = 0.03\,\mathrm{m}^2/\mathrm{V}$ Process

$T_{OX} = 7.1\,\mathrm{nm}$ Parameters

$$C_{OX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{OX}} = 0.0048\,\mathrm{F/m}^2$$

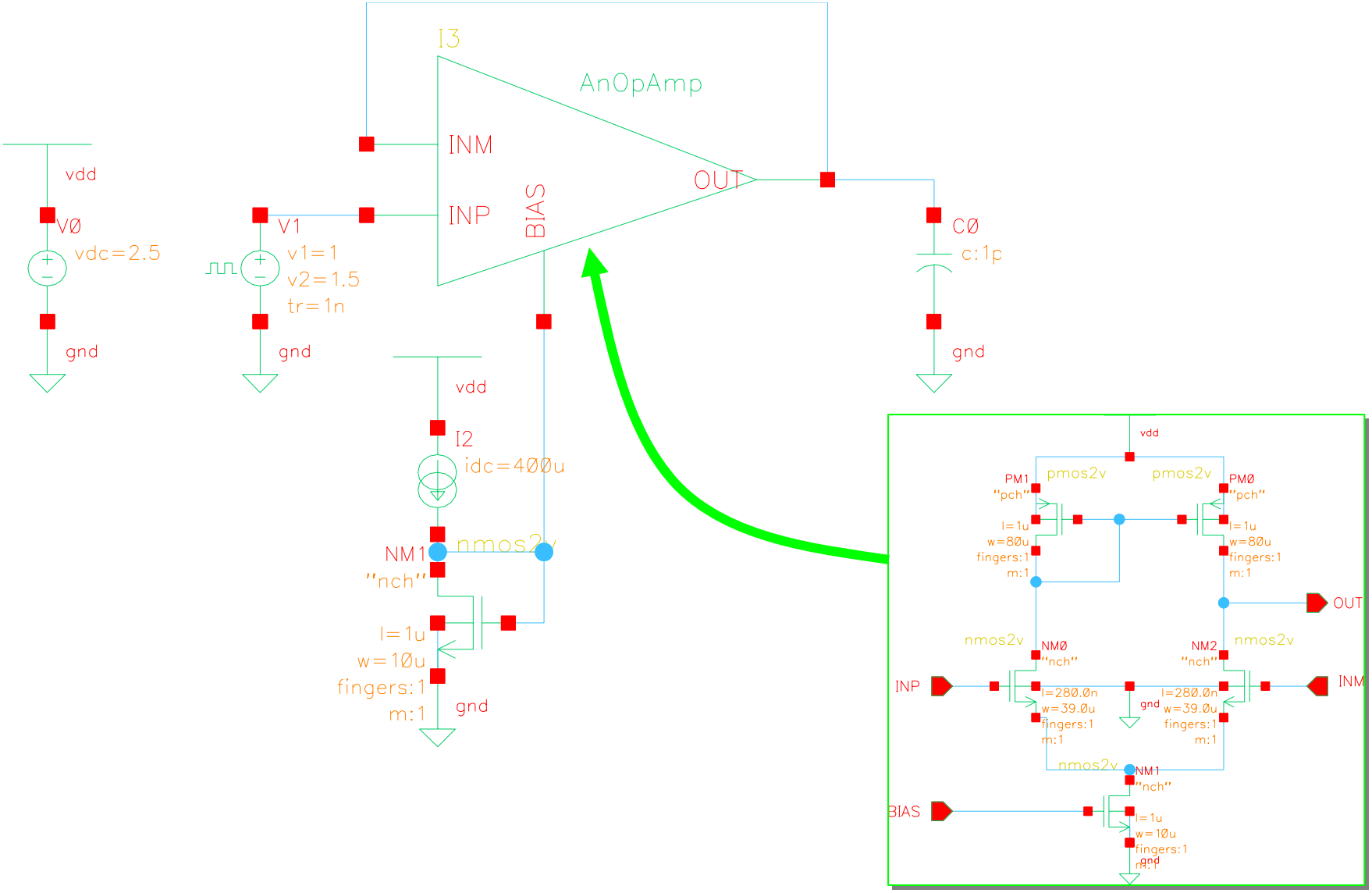
$1\,\mathrm{mW} \Rightarrow 400\ \mu\mathrm{A}$

$$g_m = \frac{\partial I}{\partial V_{GS}} = \sqrt{\mu C_{OX} \frac{W}{L} I}$$

$$= 2\,\mathrm{mA/V} \text{ for } \frac{W}{L} \sim 140$$

Check the calculation with simulation

Simulation Schematic



Simulation

Netlist

```
MS2 D1 D1 VDD VDD PCH L=1U W=80U M=1
C1 OUT GROUND 1P
V3 N$617 GROUND DC 0V AC 1 0
V2 INP N$617 PULSE ( 1 1.5 50N 1NS 1NS 1 2 )
I1 VDD N$207 DC 0.25MA
MN4 N$207 N$207 GROUND GROUND NCH L=1U W=20U M=1
MN3 OUT OUT S1 GROUND NCH L=0.28U W=39U M=1
MN2 D1 INP S1 GROUND NCH L=0.28U W=39U M=1
MS1 OUT D1 VDD VDD PCH L=1U W=80U M=1
MN1 S1 N$207 GROUND GROUND NCH L=1U W=20U M=1
V1 VDD GROUND DC 2.5V
```

Choice of model

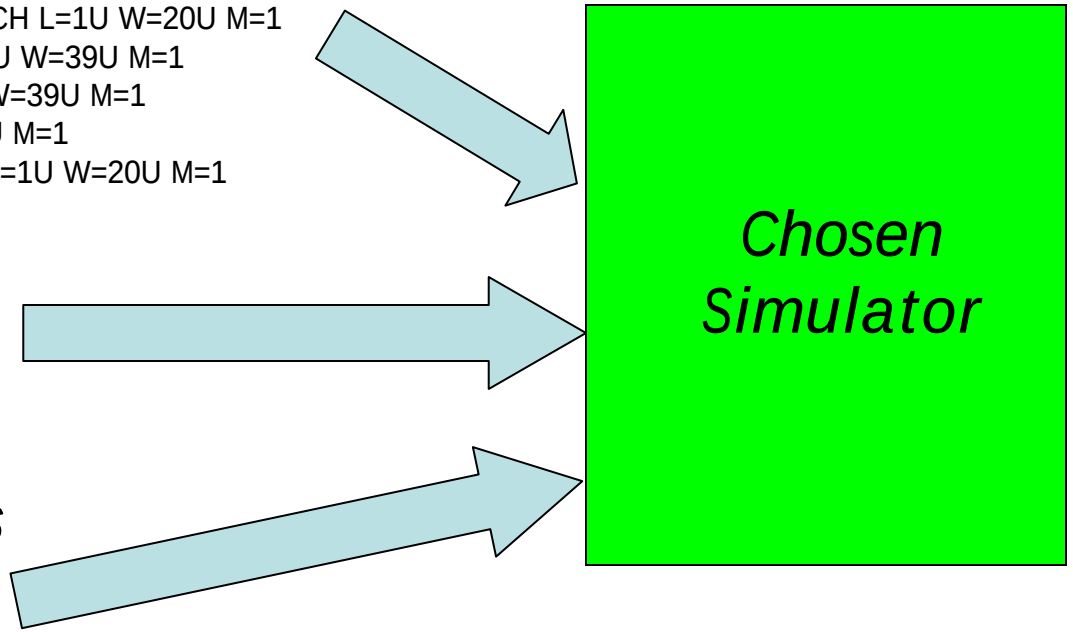
$$I = \frac{\mu C_{OX}}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2$$

Process parameters

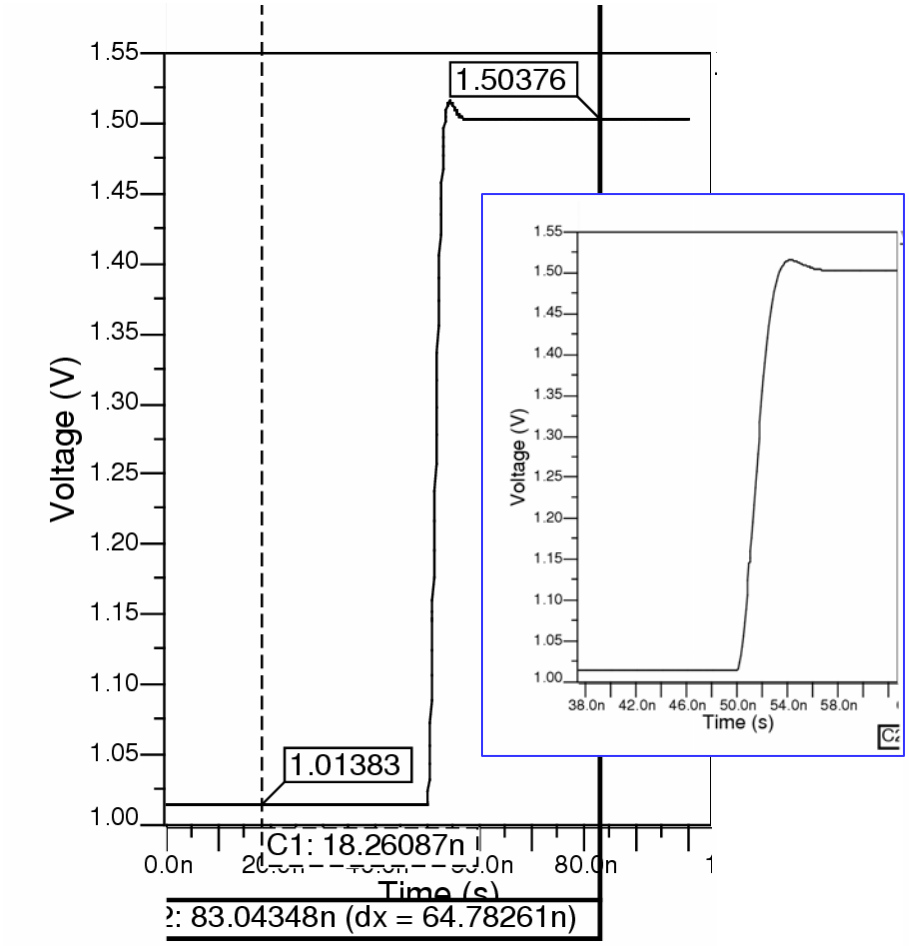
$$\mu = 0.03\,\mathrm{m}^2/\mathrm{V}$$

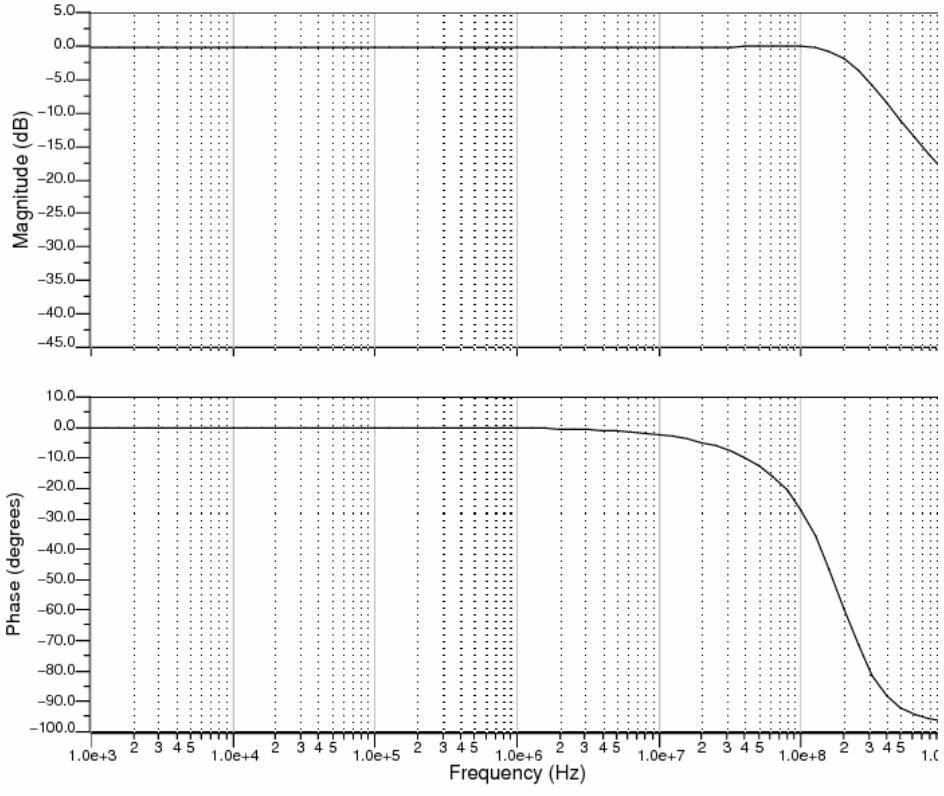
$$T_{OX} = 7.1\,\mathrm{nm}$$

$$C_{OX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{OX}} = 0.0048\,\mathrm{F/m}^2$$



How Did We Do?





Response to a 1 → 1.5V step

2nd Order Effects are Critical in IC Design

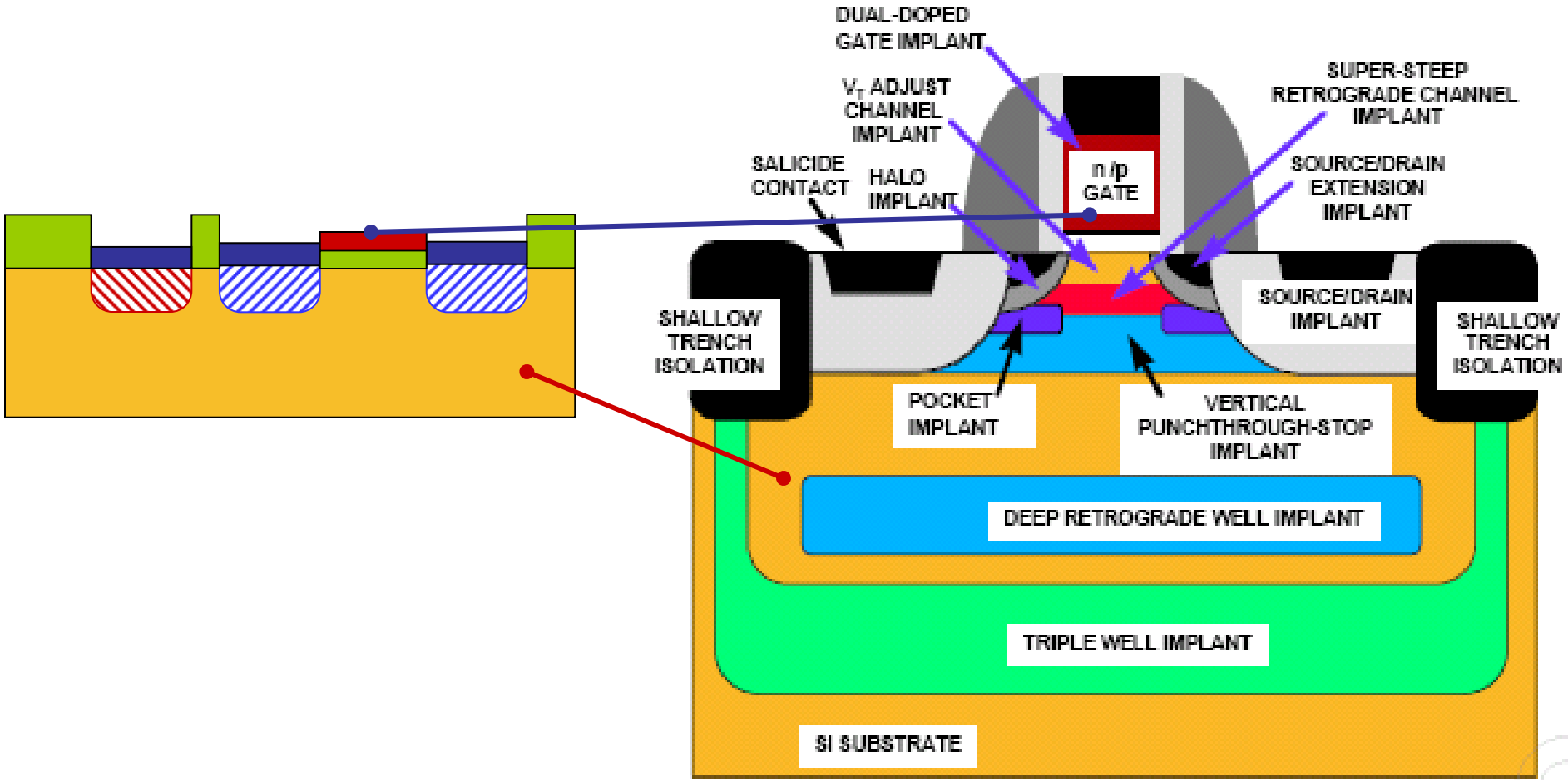
- g_m – not too bad, hand calculation → 2 mA/V, simulation → 1.86 mA/V
- R_{DS} – not so good, hand calculation → ∞ Ω, simulation → 24 kΩ
  - Channel length modulation: $I_{DS} \rightarrow I_{DS}(1 + \lambda V_{DS})$ so $R = 1/\lambda I_{DS}$
- DC gain – not so good, hand calculation → ∞, actual value is $A_V = g_m R_{DS}$ = 1.86 mA/V x 24 k Ω ~ 50 ⇒ offset of 1-2%

- OK – so now, I understand everything, right?

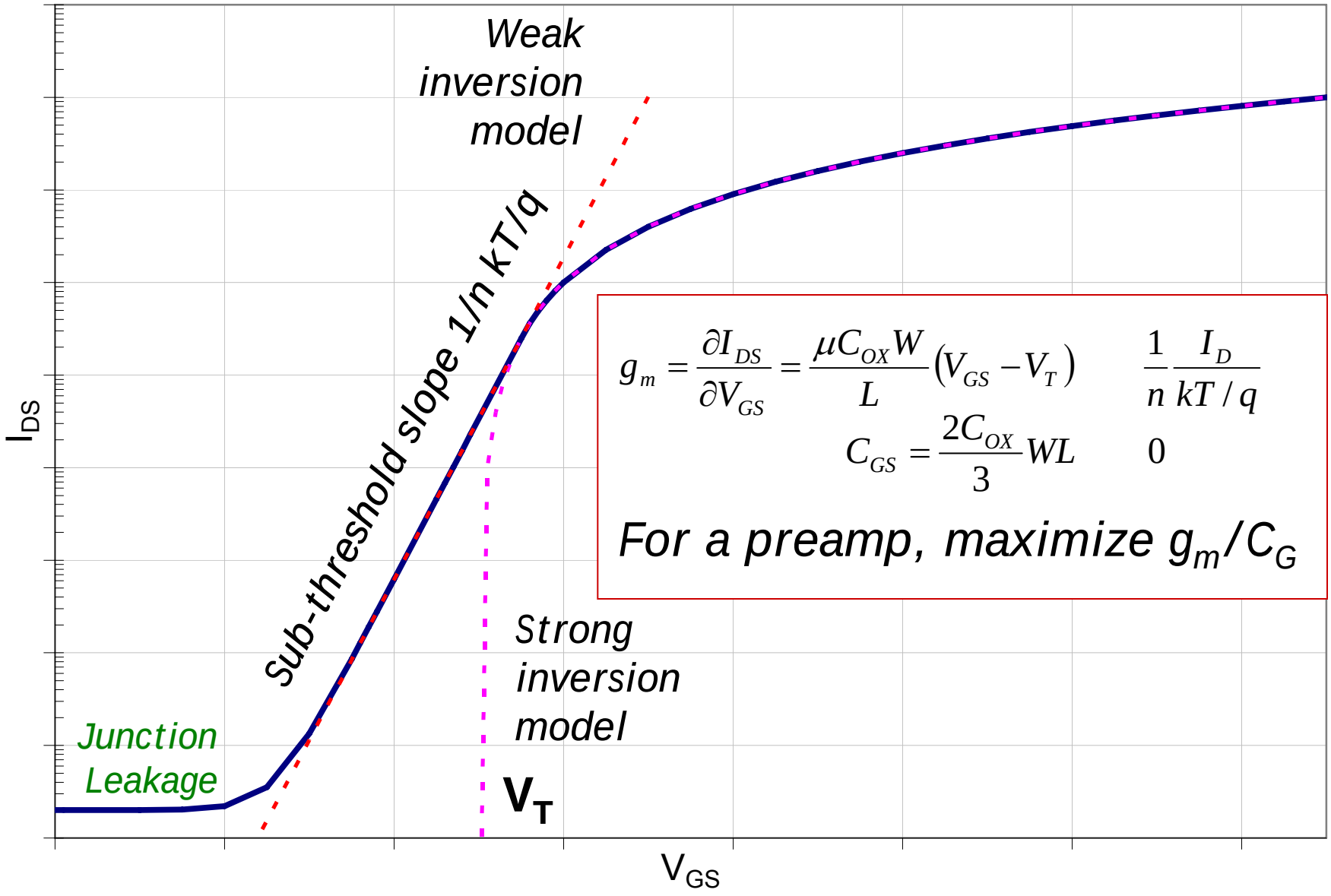
Modern Devices are more Complicated

Simple model

Modern Reality



2nd Order Effects may be 1st Order for the Design



$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu C_{OX} W}{L}(V_{GS} - V_T) \qquad \frac{1}{n}\frac{I_D}{kT/q}$$

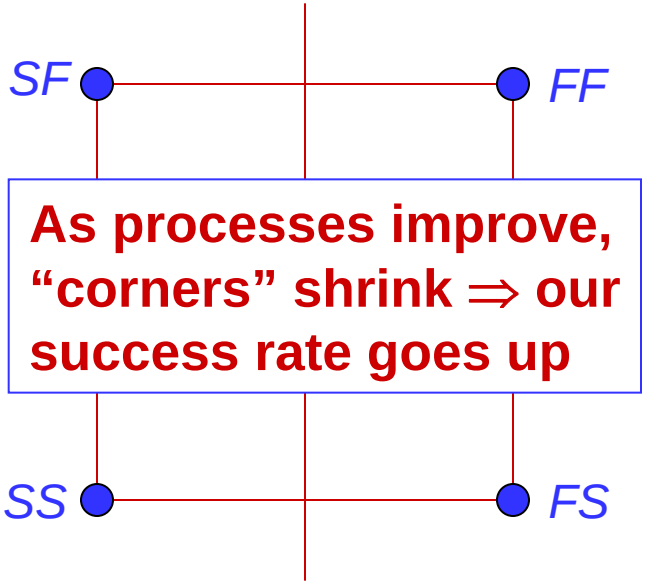
$$C_{GS} = \frac{2C_{OX}}{3}WL \qquad 0$$

For a preamp, maximize g_m/C_G

Process Variation

- Simulation parameters are for the “typical” process
- But what if you got the “Friday at 4:30” process?
- Foundries often provide “corner” data which attempt to represent, within device models, what are the “worst” and “best” cases. The designer needs to make sure that the design works under all of these cases (you don’t know who will be running the implanter the day of *your* run)

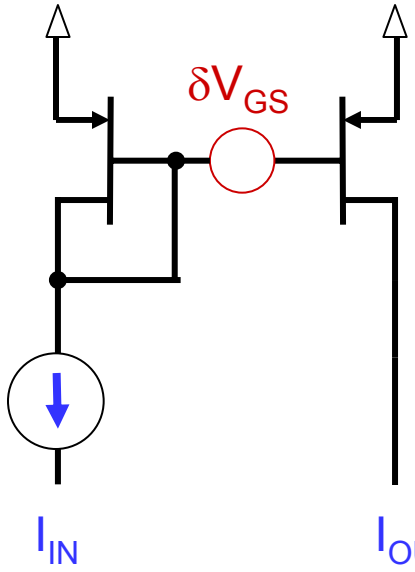
The process variation models often take the form that one flavor of transistor is “better” (or “faster”) than the other, and the cause may be correlated or anti-correlated with the other flavor. This leads to 5 cases: “typical” and the permutations of the extremes above.



- OK – so now, I understand everything, right?

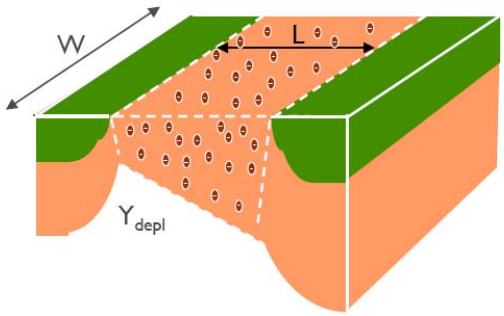
Matching

- Not all Carthusian monks are identical – nor are all MOS transistors
- Directional variation of implantation across the wafer; statistics of how many dopant atoms there are…



Same V_{GS}
≠Same current

PHILIPS example 90 nm CMOS node transistor

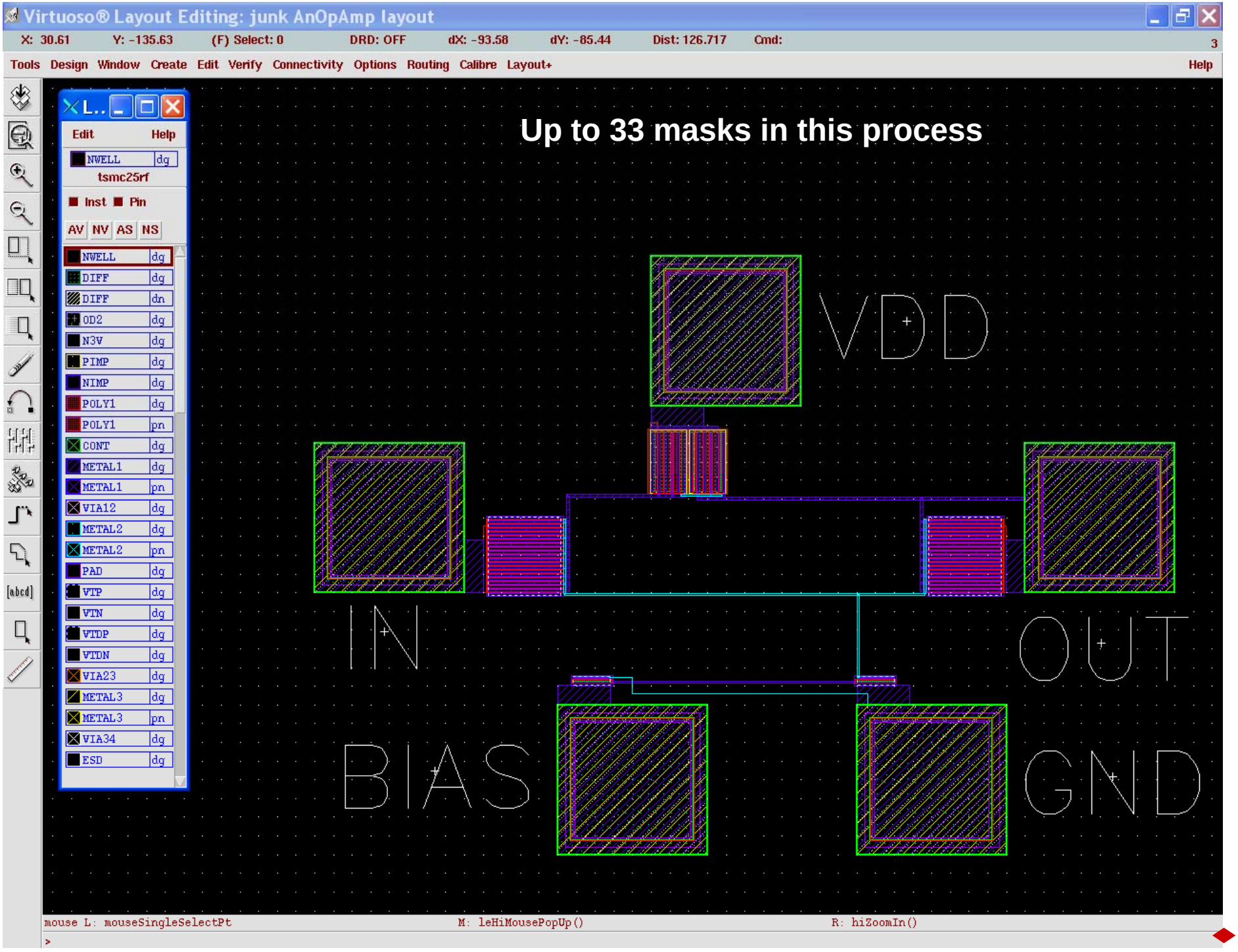


L ≈ 40 nm (effective)
W ≈ 60 nm (effective)
Y_{depl} ≈ 25 nm
$N_a \approx 2 \times 10^{18}$ /cm^3

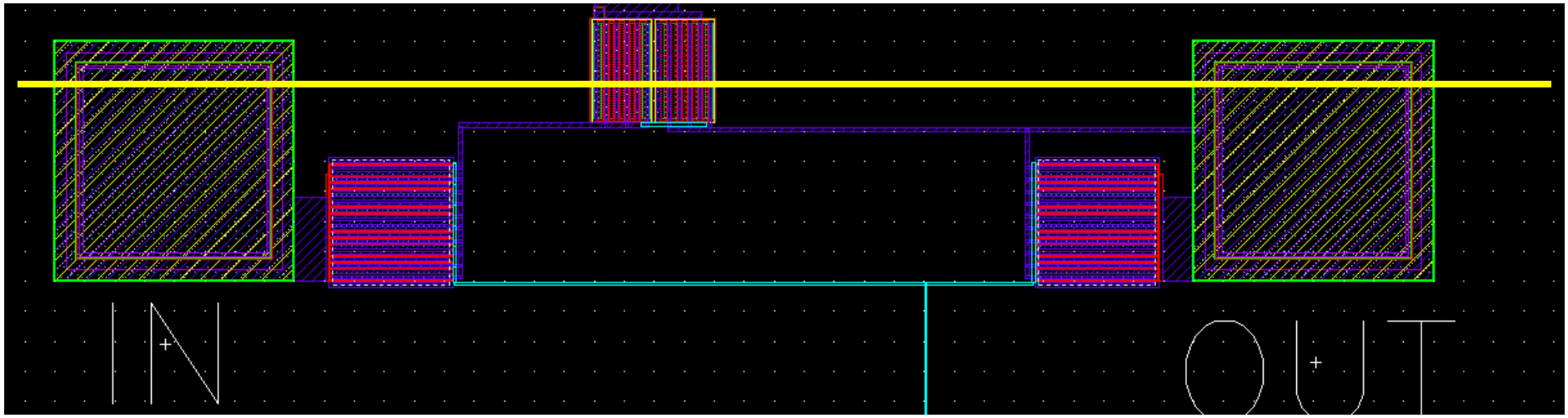
n_{act} ~ 1300 atoms

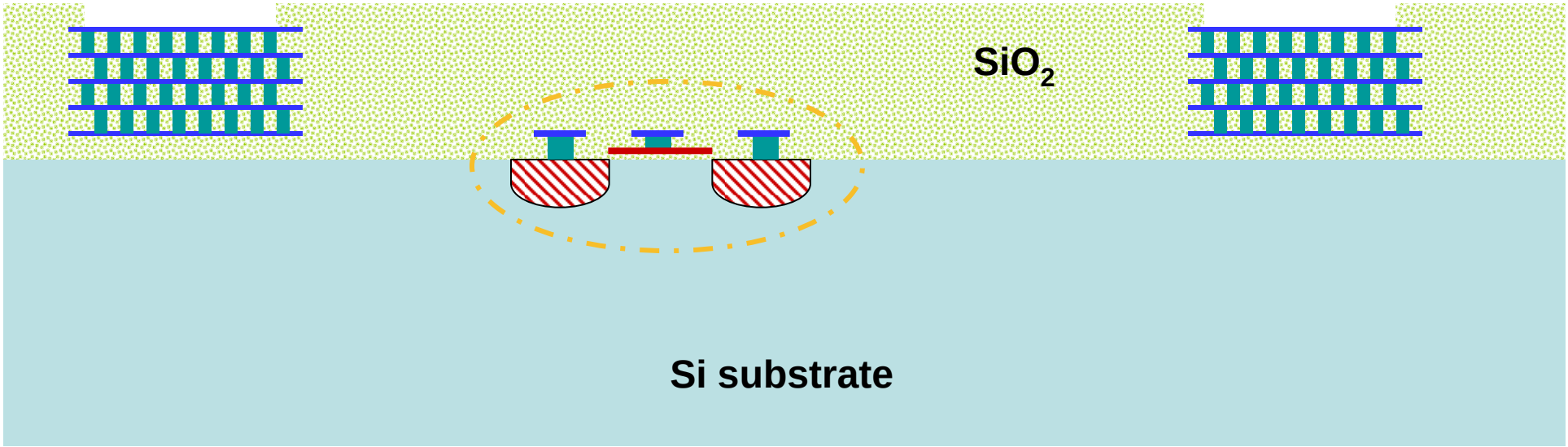
⇨ Poisson statistics

1 σ fluctuation $\sqrt{n_{act}}$ ~ 40 atoms

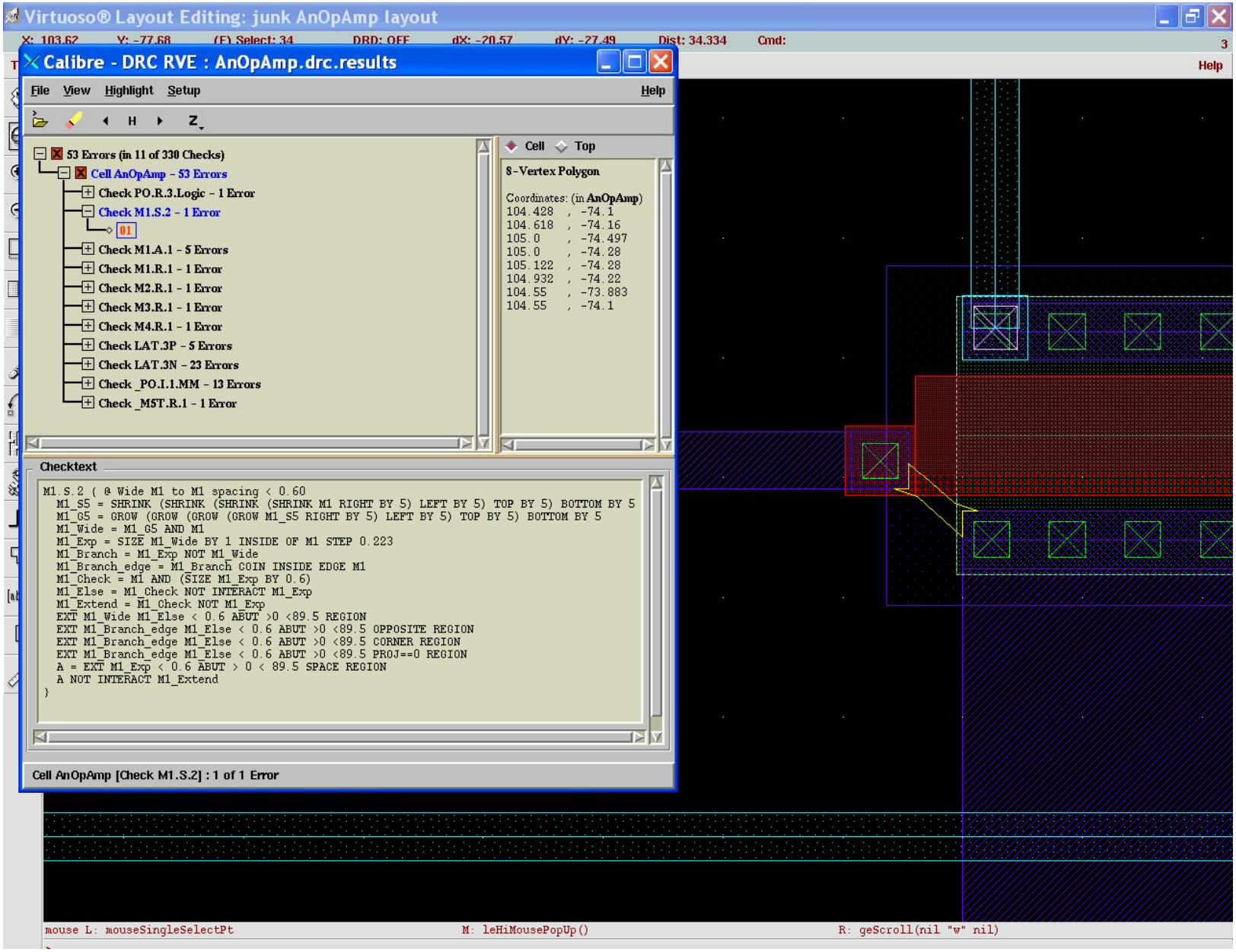

Virtuoso® Layout Editing: junk AnOpAmp layout
X: 30.61 Y: -135.63 (F) Select: 0 DRD: OFF dX: -93.58 dY: -85.44 Dist: 126.717 Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Calibre Layout+ Help
Edit Help
NWELL dg
tsmc25rf
Inst Pin
AV NV AS NS
NWELL dg
DIFF dg
DIFF dn
OD2 dg
N3V dg
PIMP dg
NIMP dg
POLY1 dg
POLY1 pn
CONT dg
METAL1 dg
METAL1 pn
VIA12 dg
METAL2 dg
METAL2 pn
PAD dg
VTP dg
VTN dg
VTDP dg
VTDN dg
VIA23 dg
METAL3 dg
METAL3 pn
VIA34 dg
ESD dg
Up to 33 masks in this process
VDD
IN
OUT
BIAS
GND
mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: hiZoomIn()

Drawn Layers





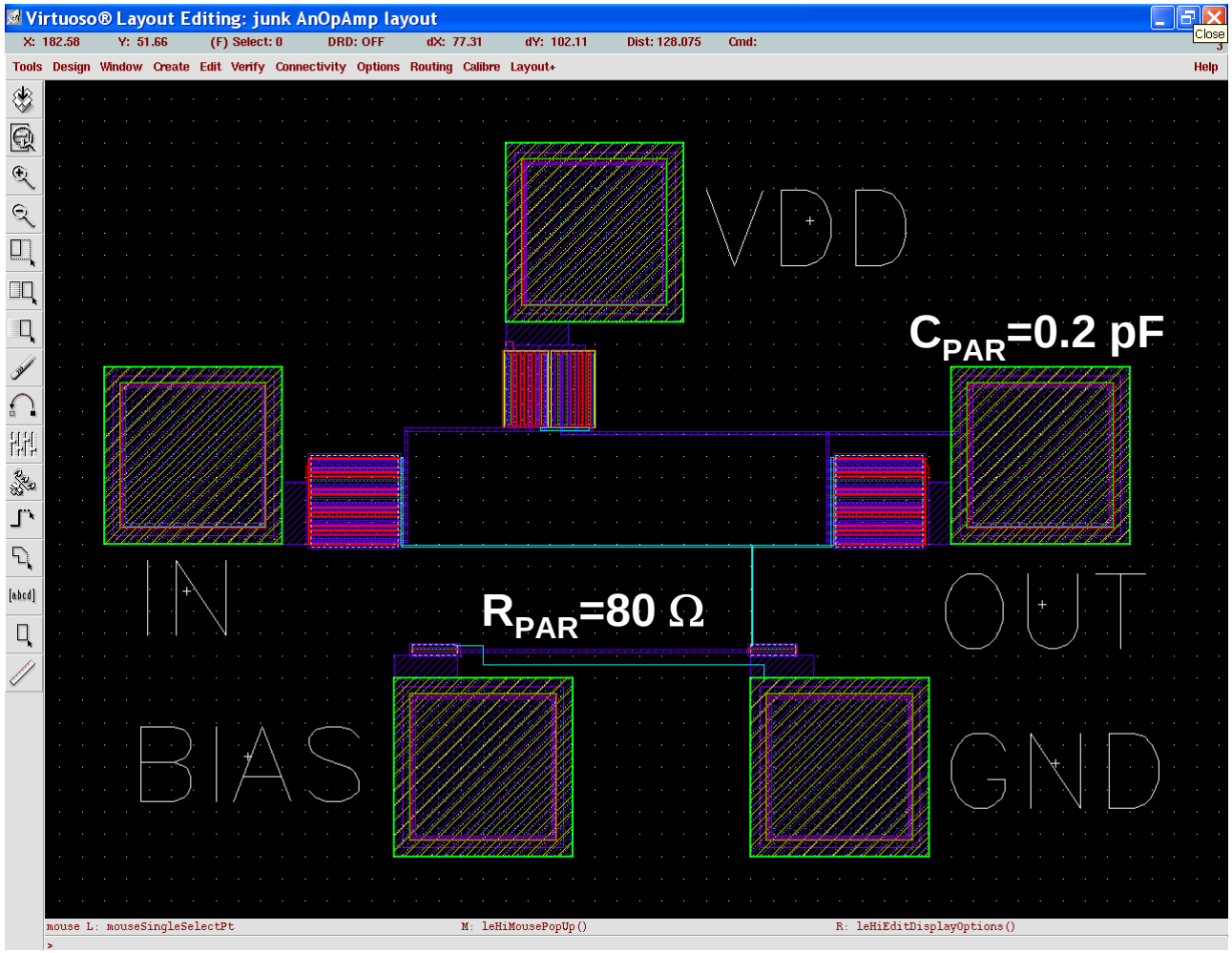
Verification



- DRC
- LVS

Still Not Done

- Extraction (of parasitics) and “post-layout” simulation
- 2nd Order Effects are Critical in IC Design

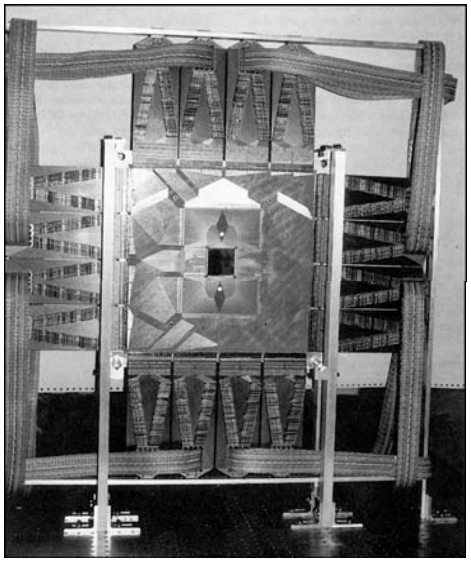


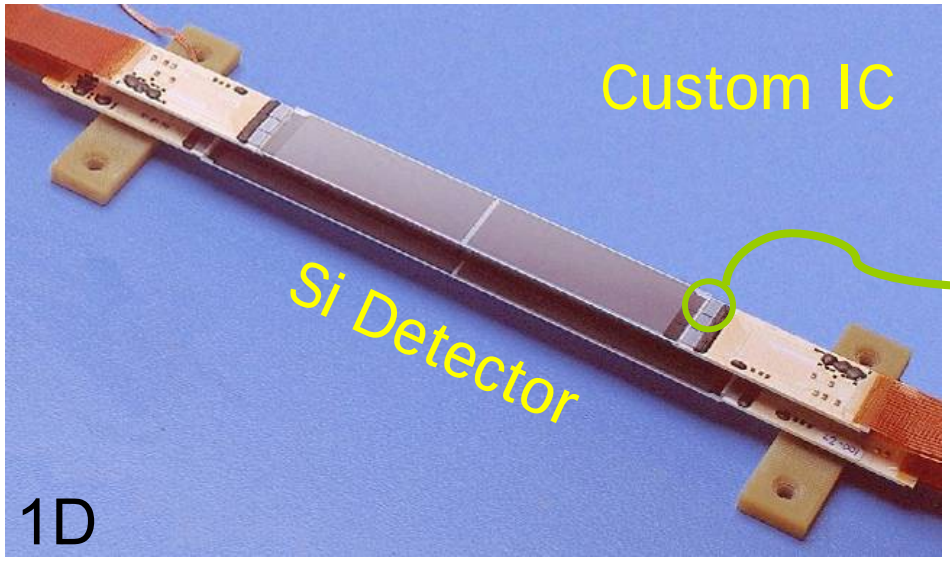
Various other design sins not checked

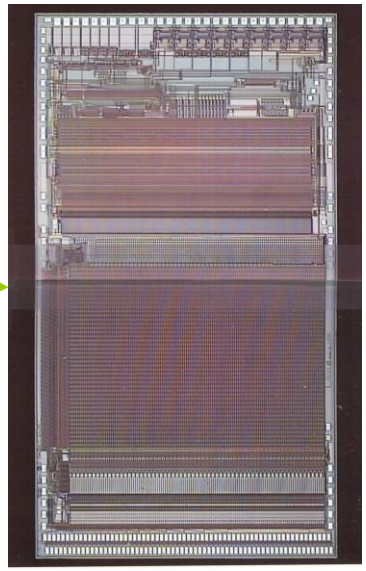
Current IC Group Projects

- 4-channel CCD readout (CDS + 16 bit dynamic range digitizer) for SNAP (space qualified)
- A “high-voltage” clock driver and sequencer for the above (space qualified)
- A 16-channel higher-speed variant for almost Column-Parallel CCD readout (>100 fps / Megapixel; ≥14 bits)
- 4-channel, 10 GS/s switched capacitor array with digitizers and digital waveform accumulators
- 16x16-channel CdTe pixel readout for high-energy x-ray astronomy (space qualified)
- Monolithic detectors (see below)

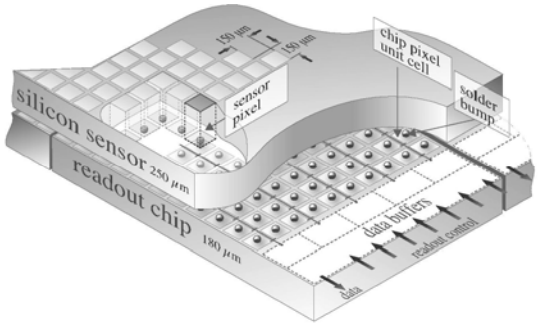
Increasing Integration

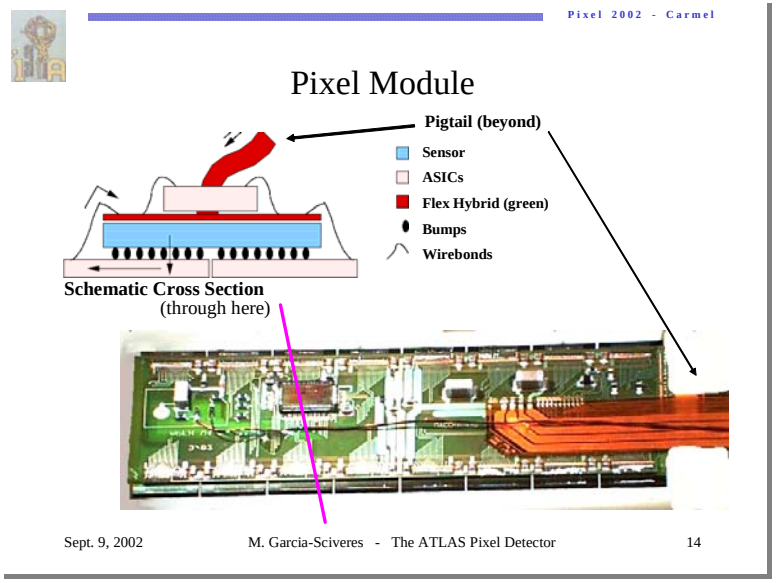


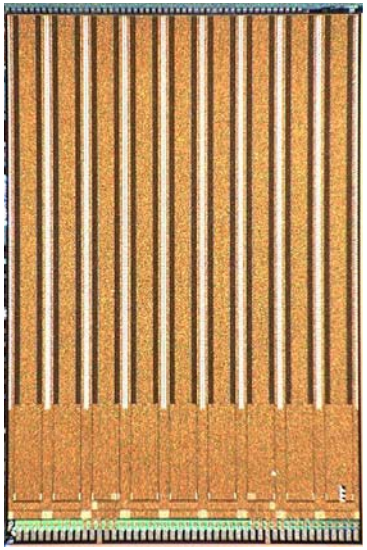




2D-Hybrid

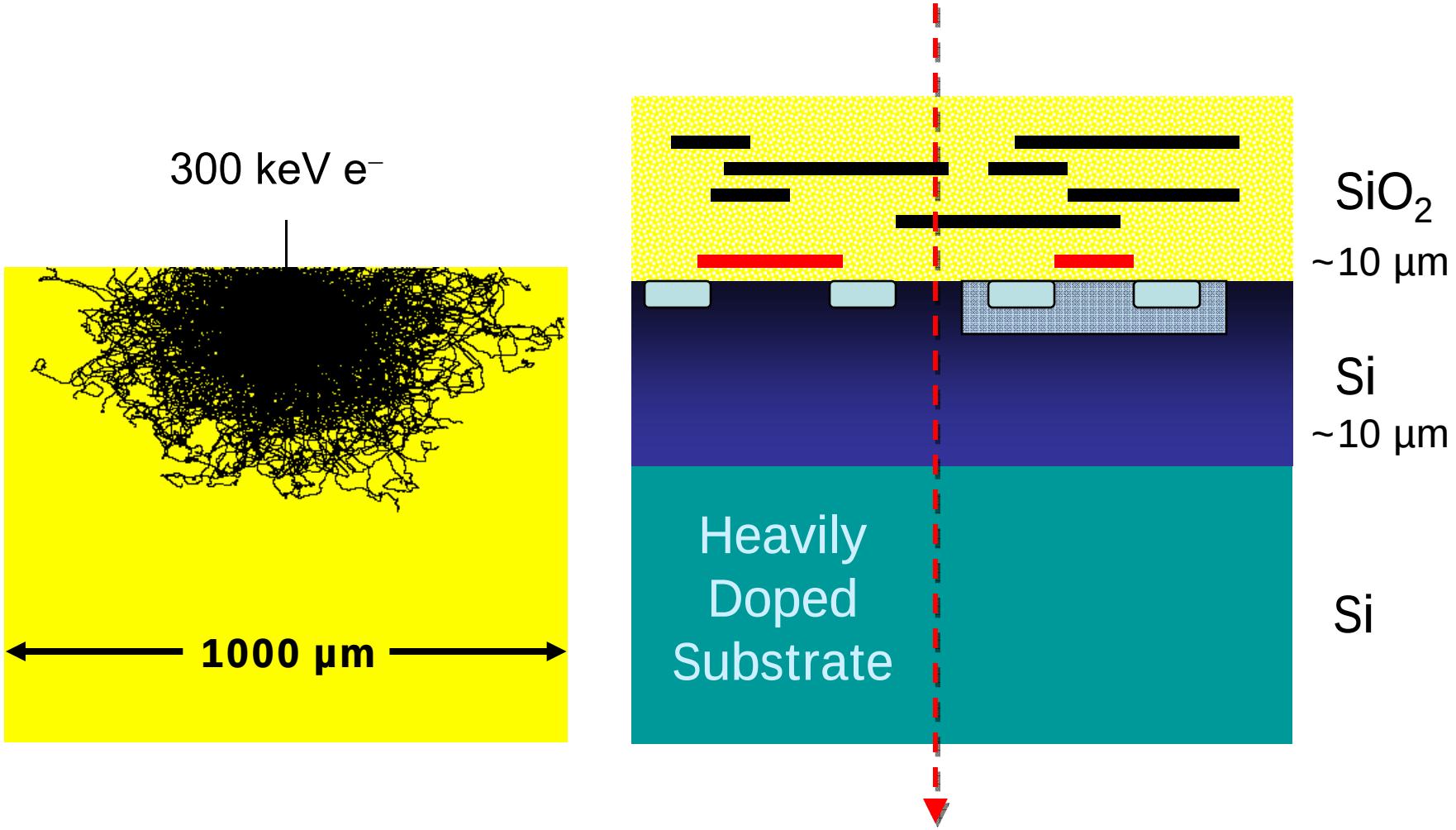




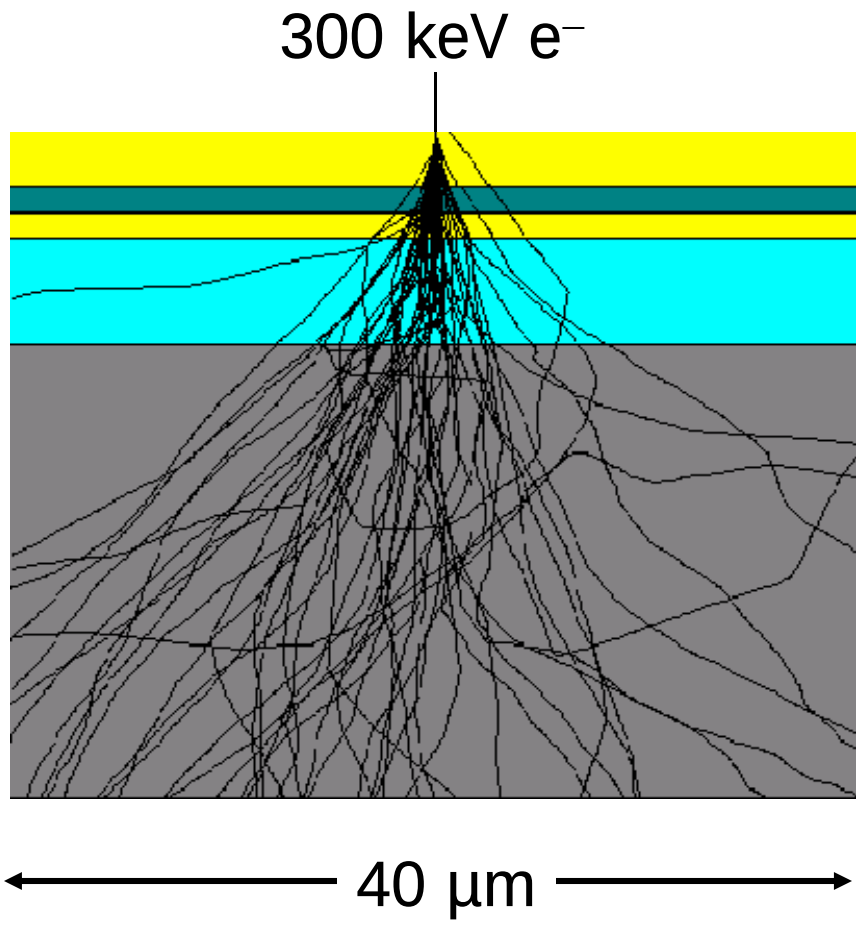


Active Pixels – the IC *is* the Detector

Used to replace CCDs in cheap (and now not-so-cheap) digital cameras
Also might make the ideal detectors for certain types of electron microscopy

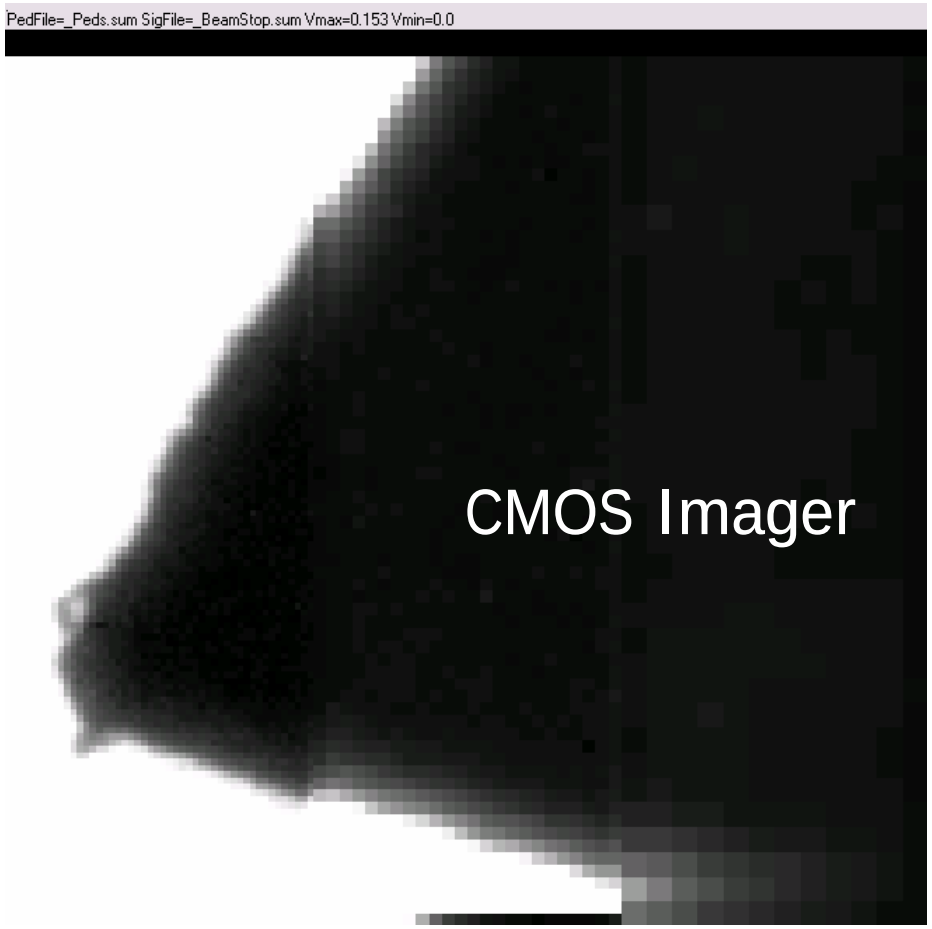


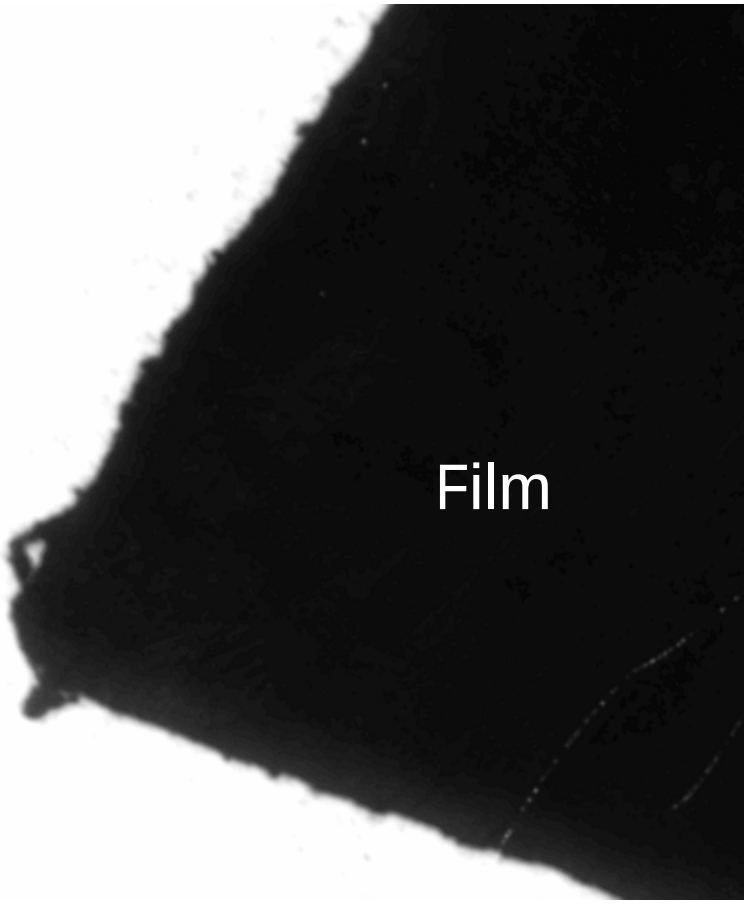
Well Adapted to High Sensitivity (speed)



- Thin detector
- Thin collection region *within* thin detector
- Gain – e^- are several times minimum ionizing: very high S/N
- Monolithic – can add on-chip electronics (ADCs, fast readout …)
- Use radiation-hardening techniques developed for HEP

1st Image (200 keV)





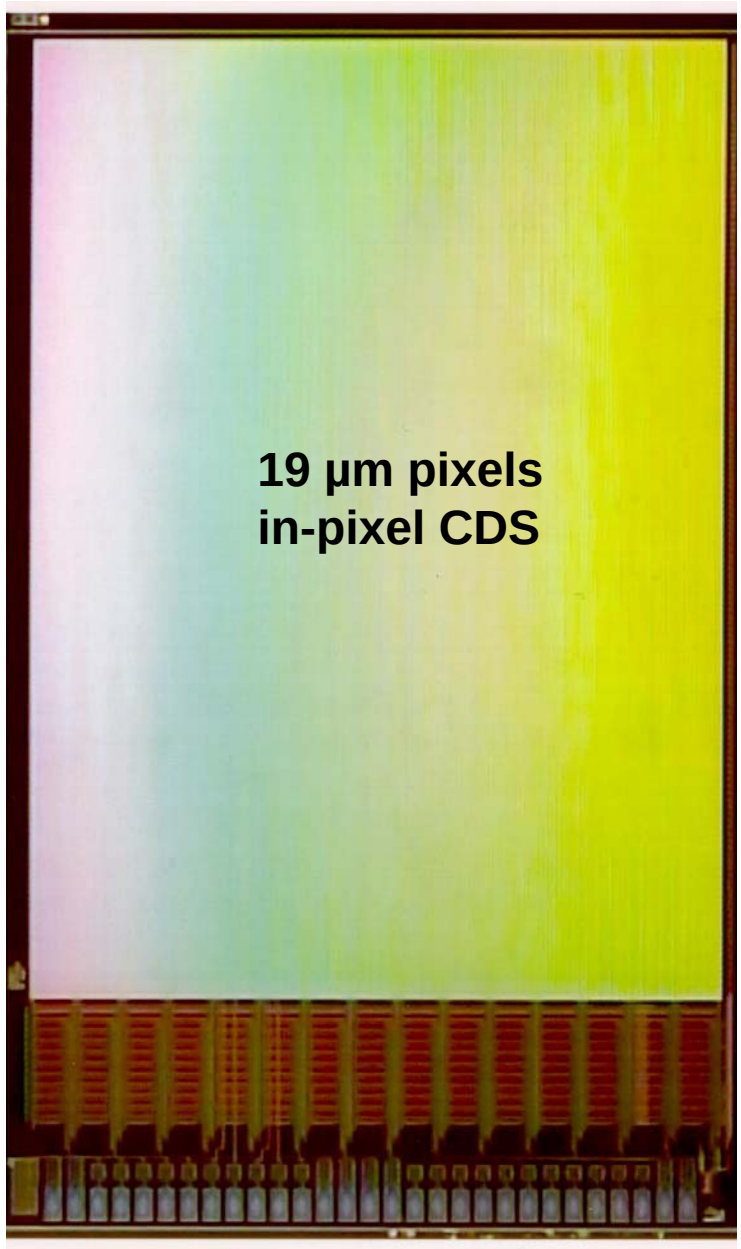
48x144
10 µm Pixels

24x72
20 µm Pixels

12x36
40 µm Pixels

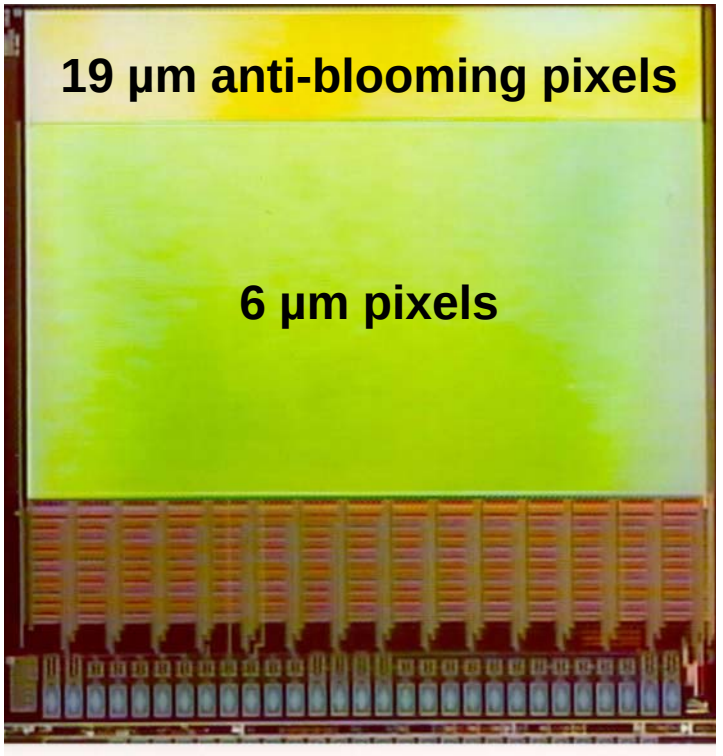
Beam stop on the 200 CX at NCEM

1st Useful Detector Prototypes



Constructing readout and
user interface software now

10 bit ADCs
on 19 µm
pitch



Future for IC Design

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

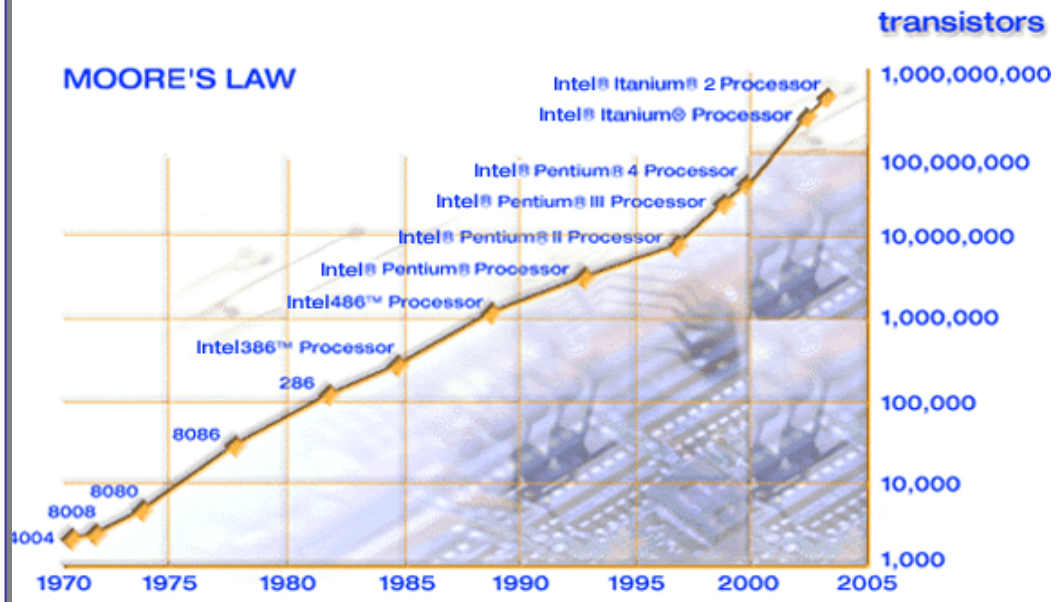
Both approaches have worked well and are being used in equipment today.

The author

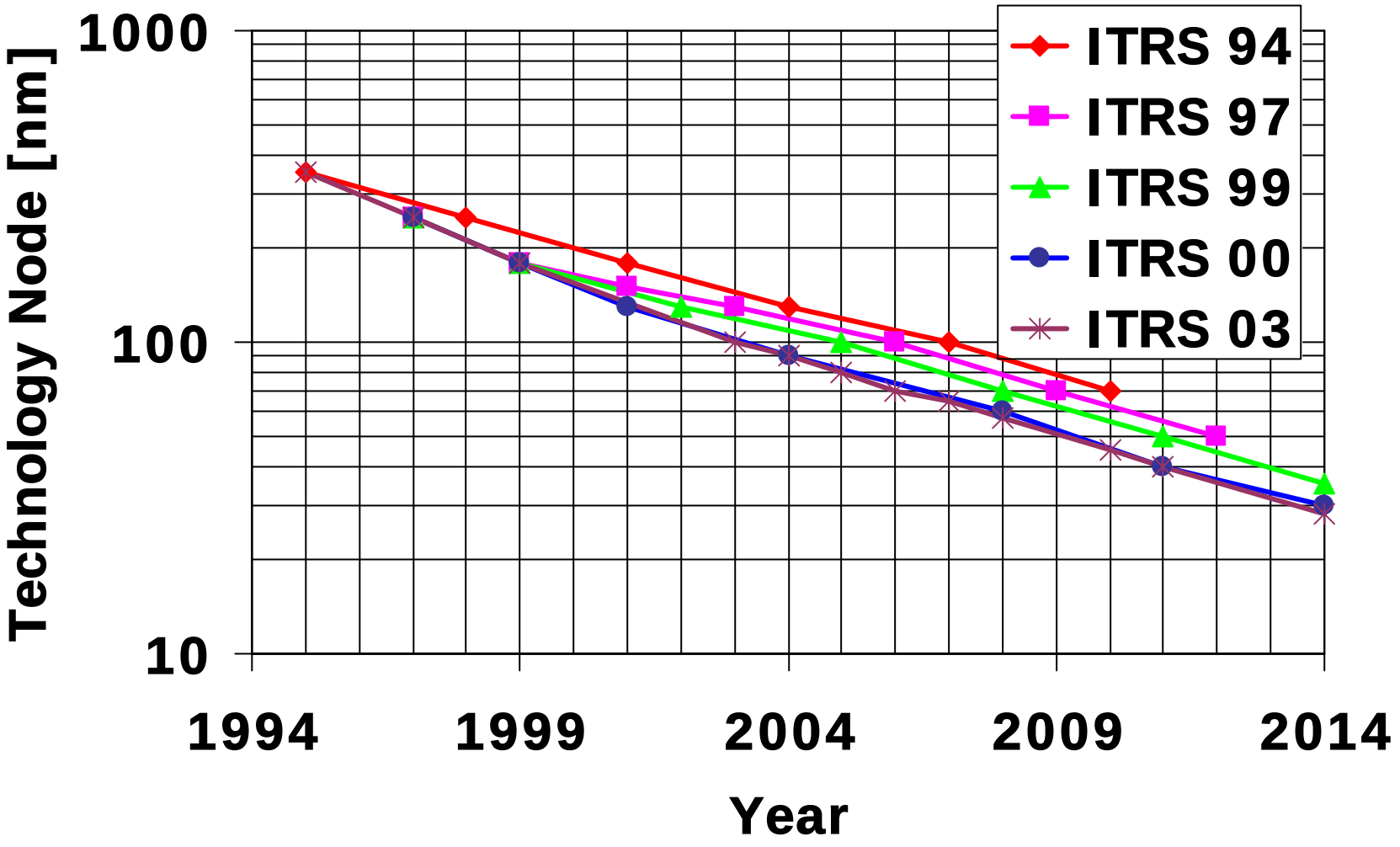
Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Electronics, Volume 38, Number 8, April 19, 1965

Mandatory Plot



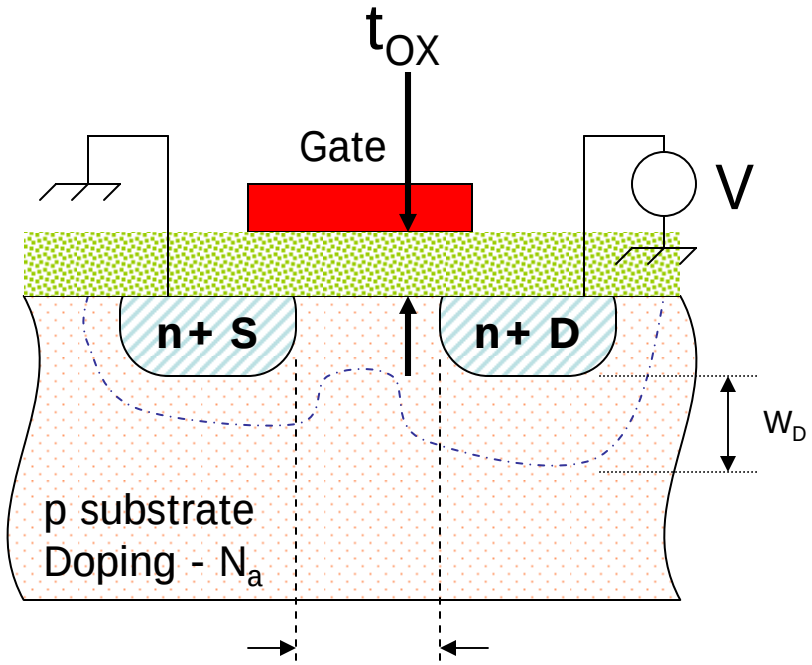
Technology Node Scaling



International Technology Roadmap for Semiconductors

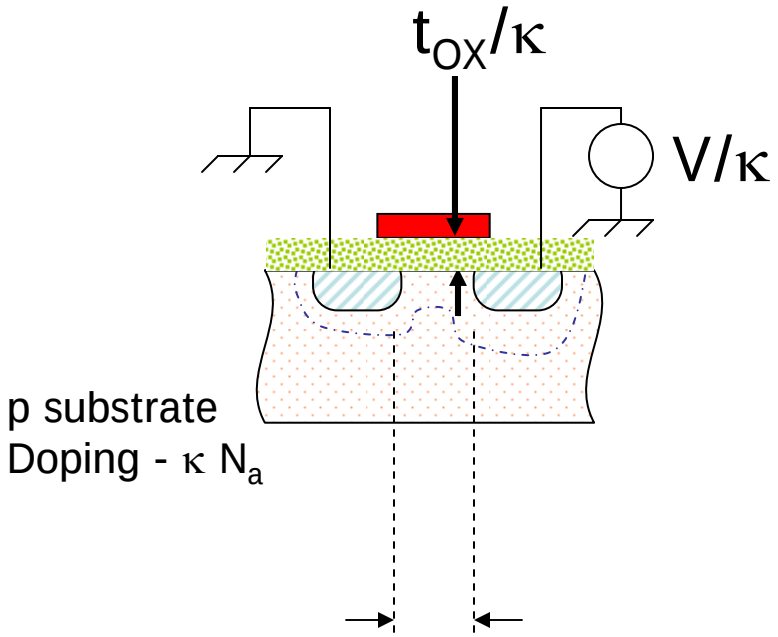
CMOS Scaling

NMOS



Channel Length L

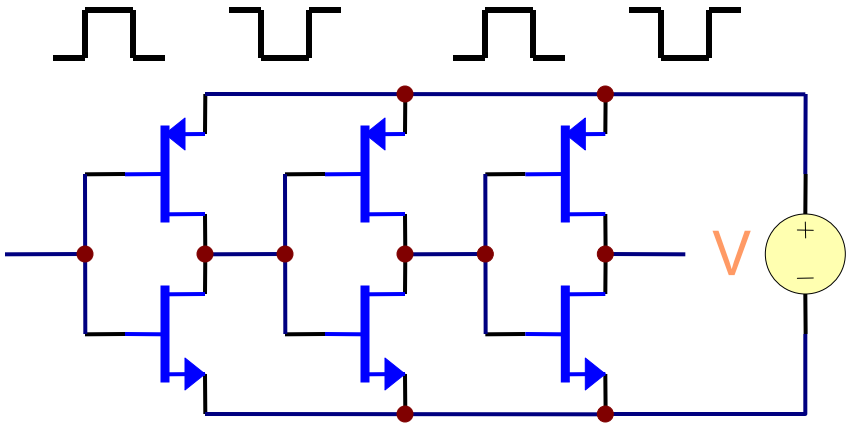
Scaled NMOS

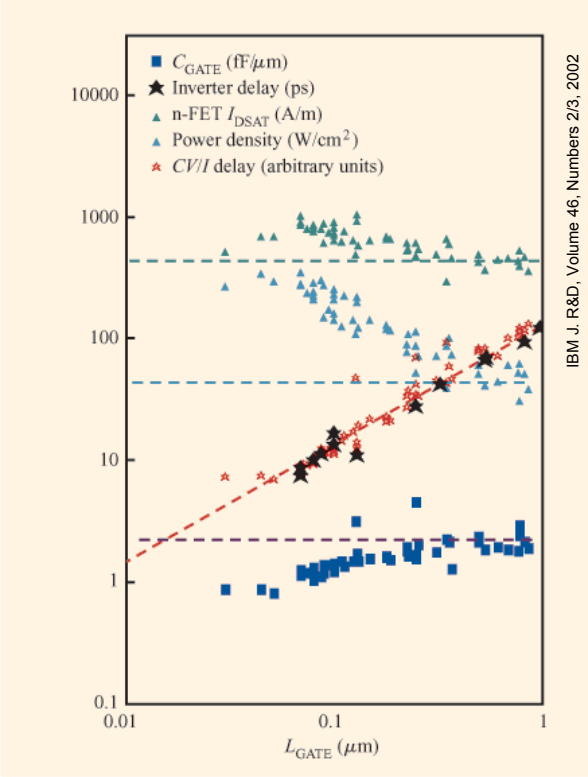


Channel Length L/κ

Constant Field Scaling

Advantages of Scaling

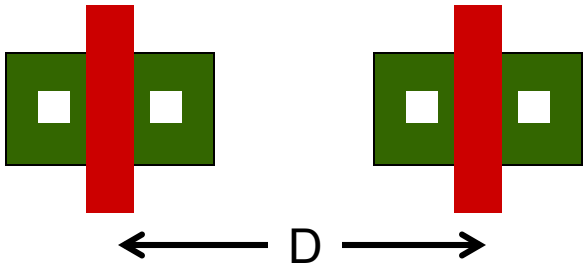


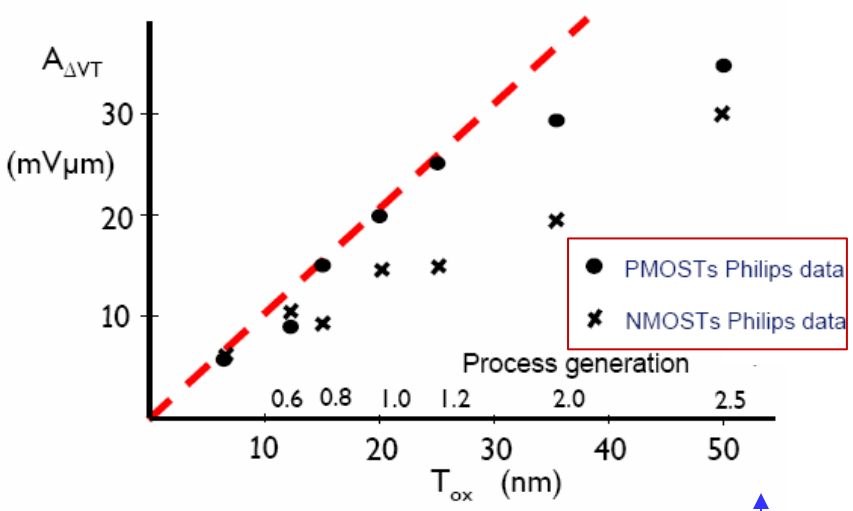


- Speed ~$C_{GATE}V_{DD}/I_{DSAT}$~ $1/\kappa$
- Circuit Density ~ $1/A \sim \kappa^2$
- Power/circuit ~ $1/\kappa^2$
- Power Density (P/A) ~ 1

Great for digital.
Just press the "zoom" button and shrink your layout!
Analog is another story

Another Word on Matching





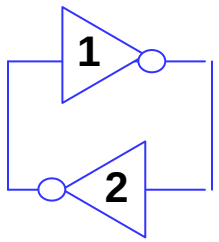
Fluctuations in doping

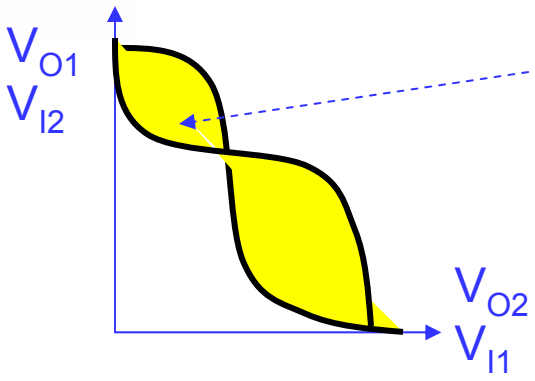
$$V_T \sim \sqrt{N_a} T_{OX} \propto \sqrt{WL}\, T_{OX}$$

$$\sigma(V_T) = \frac{A_{V_T}}{\sqrt{WL}} \oplus S_{V_T} D$$

$$A_{V_T} \propto T_{OX}$$

Scaling: W/L=const., L∝TOX
But newer technologies don't have
$A_{VT} \times L_{MIN}$ = const.
Bad for analog, *worse* for digital.
Digital to the rescue?





Mismatch affects this noise margin

What's Next?

Table 59a Single-gate Non-classical CMOS Technologies

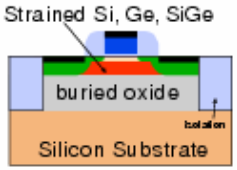
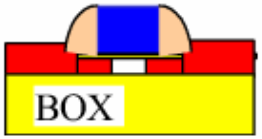
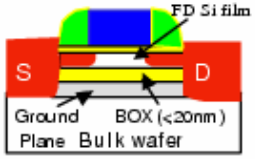
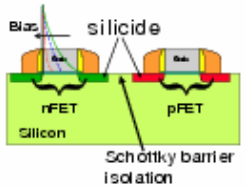
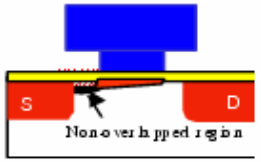
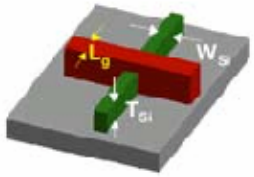
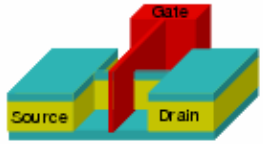
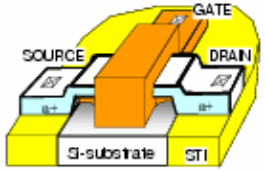
Device	*Transport-enhanced FETs*	*Ultra-thin Body SOI FETs*		*Source/Drain Engineered FETs*	
					
Concept	Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI	Fully depleted SOI with body thinner than 10 nm	Ultra-thin channel and localized ultra-thin BOX	Schottky source/drain	Non-overlapped S/D extensions on bulk, SOI, or DG devices

Table 59b Multiple-gate Non-classical CMOS Technologies

Device	*Multiple Gate FETs*				
	N-Gate (N>2) FETs	*Double-gate FETs*			
					
Concept	Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction

"Scaling" and "Death of CMOS" are talks on their own…

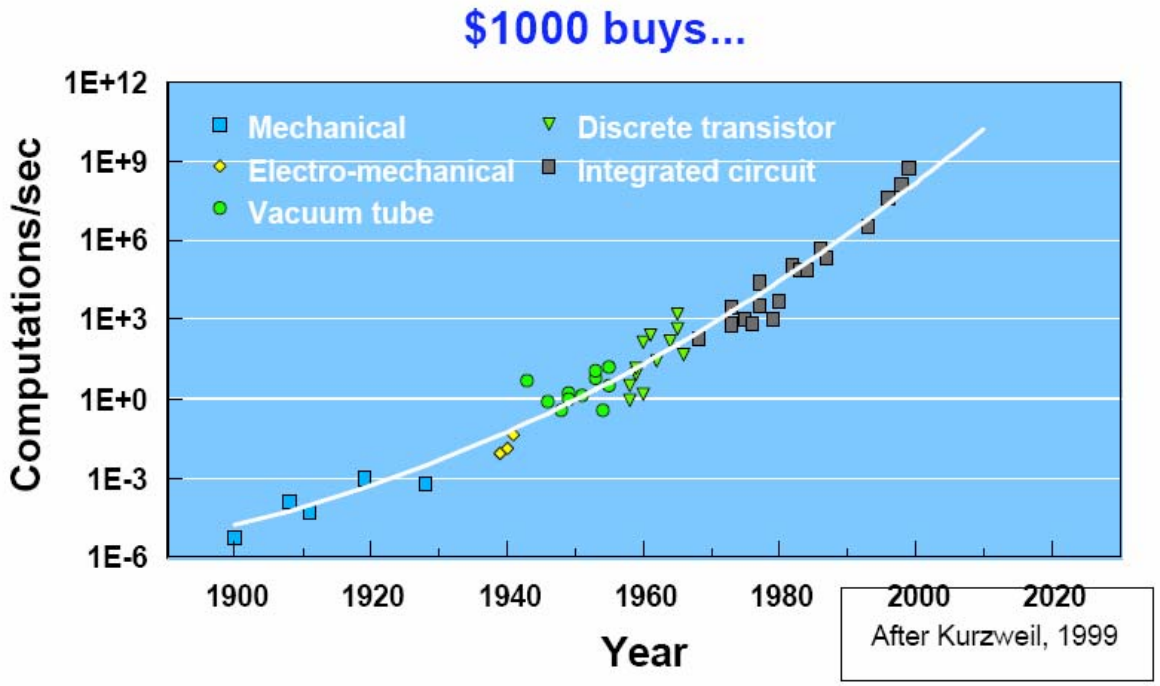
ITRS 2003

Future for IC Design at LBL

- Keep the edge in HEP (LHC upgrades, Linear Collider)
- Astronomy – on the ground and in space
- Biology and materials – imaging detectors
  - general “smart” detectors – 2D arrays measuring (x, y, E, t)
  - specialized “smart” detectors – e.g. built-in temporal autocorrelations
  - fast detectors for dynamics – “movies”
  - high sensitivity
- R&D
  - Hybrid pixilated APDs – 2D single photon counting arrays
  - Chemfets – CMOS circuits where the conduction modulation is by (bio) chemical reaction

How did we get to this point?

Growth of computations/second over time



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A Whichard
H Yaver
S Zimmermann

Topics not suitably addressed

- CMOS scaling
- New devices
- SiGe (and other strained Si) / SOI
- Analog design problems at fine feature size
- …