The ATLAS Pixel Detector

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Overview of the ATLAS experiment

- Physics at the LHC and overview of the ATLAS Detector

Role and Requirements for Pixel Detector:

- Critical element of tracking, providing vertexing information.

Technical Challenges and Status:

- Concentrate on sensors, electronics, and interconnects
- Provide general overview of project status

Performance Achieved:

- Results from lab tests, irradiations, and test-beam studies

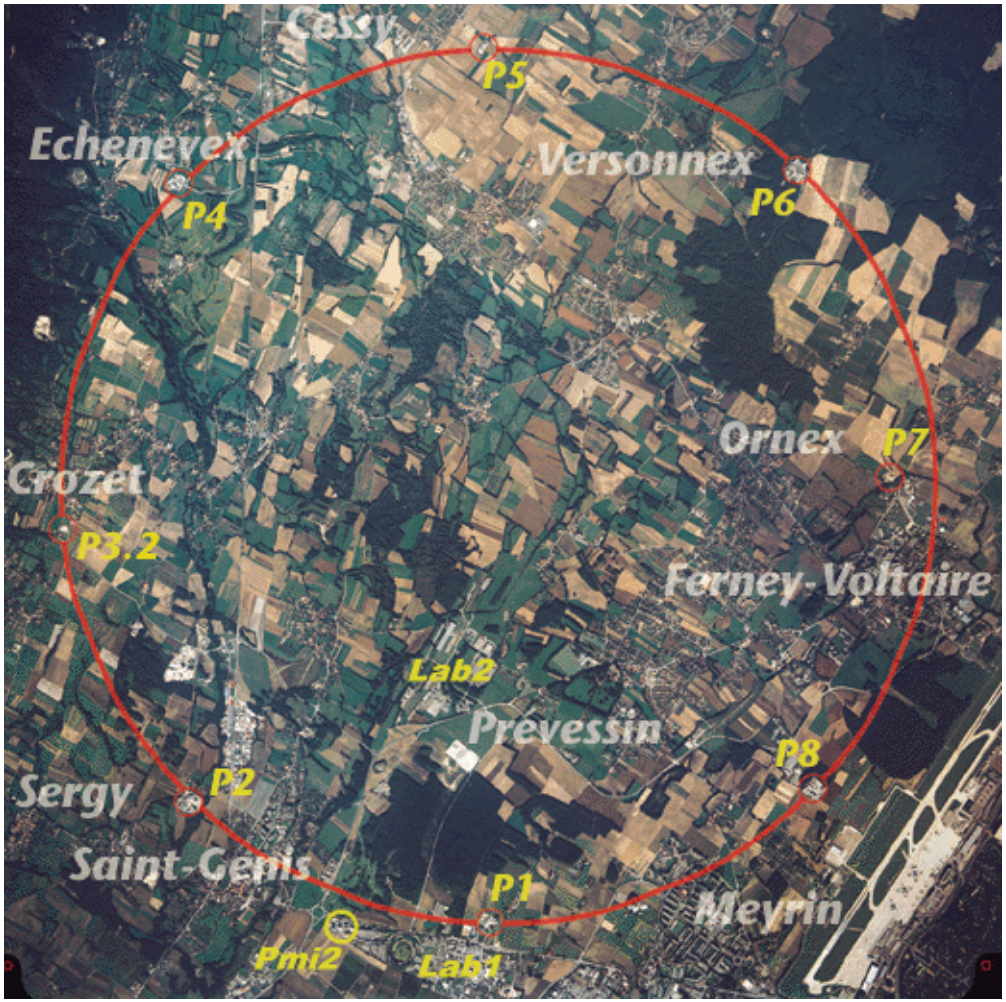
Future Evolution:

- Upgrades present still more difficult challenges

The Large Hadron Collider at CERN

Frontier facility in high-energy physics:

- Proton-proton collider with 7+7 TeV beams and luminosity up to 10^{34} $cm^{-2}s^{-1}$
- Accelerator being installed in 27km tunnel, consisting of 1232 dual-aperture dipoles operating at 8.4T and 1.9K (700KLiters of liquid Helium):



First dipoles being installed in the LHC tunnel on March 7 2005.

More than half of dipoles already delivered to CERN from industry.

Extremely rich physics program:

- First accelerator facility to allow systematic exploration of TeV-scale physics.
- For more than 20 years, this has been recognized as the key to understanding the origin of Electro-weak Symmetry Breaking and mass.
- Supersymmetry (SUSY) addresses many issues in Standard Model, including why EWSB scale is so much lower than Planck scale, why only Higgs acquires negative mass-squared to drive symmetry breaking, the apparent unification of the U(1), SU(2), and SU(3) gauge couplings at a common high scale, and providing CDM candidates as suggested by experimental cosmology.

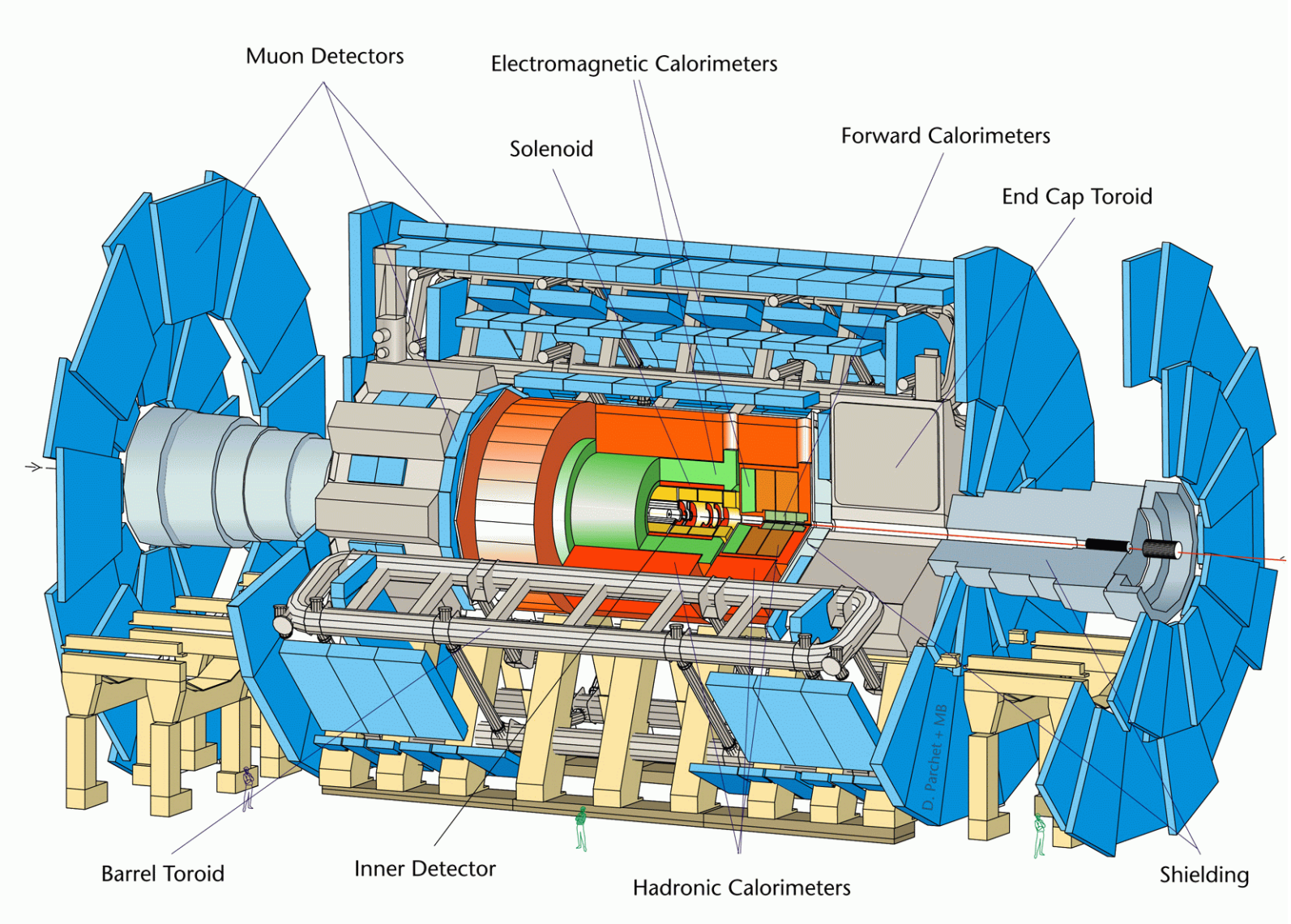
Menu of physics (besides the usual SM studies) includes:

- Top factory: producing 10^8 ttbar pairs per year at design luminosity.
- Complete coverage of SM Higgs sector and Minimal SUSY Higgs sector
- If no weakly-coupled symmetry breaking (Higgs-like), then has reach to explore strong symmetry breaking scenarios.
- Ability to observe SUSY signatures up to mass scales of about 2 TeV.
- Searches for compositeness or extra gauge bosons up to mass scales of 5 TeV.
- Sensitive to extra-dimension theories or other BSM phenomena...

Full physics menu requires operation at 10^{34} luminosity for many years => very challenging instrumentation issues !!!

The ATLAS Detector

Very large, general purpose magnetic detector for the LHC:



- Overall dimensions are roughly 45m long and 25m in diameter (and only 7000 T).

Some facts about ATLAS:

- Two large magnet systems, outer toroidal field for muon tracking, and inner solenoidal field for inner tracking.
- The toroidal field is formed by a barrel section and two endcaps, with a magnetic volume of roughly 26m long by 20m in diameter, and a bending power of 2-8Tm. The stored energy is about 1.2GJ.
- The muon system contains more than 1M readout channels, and the ensemble of chambers used have a total area of about 12000 m^2.
- The calorimetry system is almost entirely based on LAr (with the exception of central hadronic calorimeter using scintillator), weighs 4000T and covers to η=5. The complete system contains more than 200K readout channels.
- The Trigger and DAQ system can acquire events at 100KHz using a first level trigger based on calorimeter energy information and muon tracking information.
- The final event output rate, after the third level trigger, is expected to be several hundred Hz of several MB events. This would lead to data samples of 10^4 TB/year.
- ATLAS is a collaboration of roughly 2000 scientists and engineers from 151 institutions in 34 different countries.
- The completed detector is expected to see first collisions at the LHC in Q3 2007...

The ATLAS Inner Tracking Detector:

Outermost system uses gas-filled 4mm straws

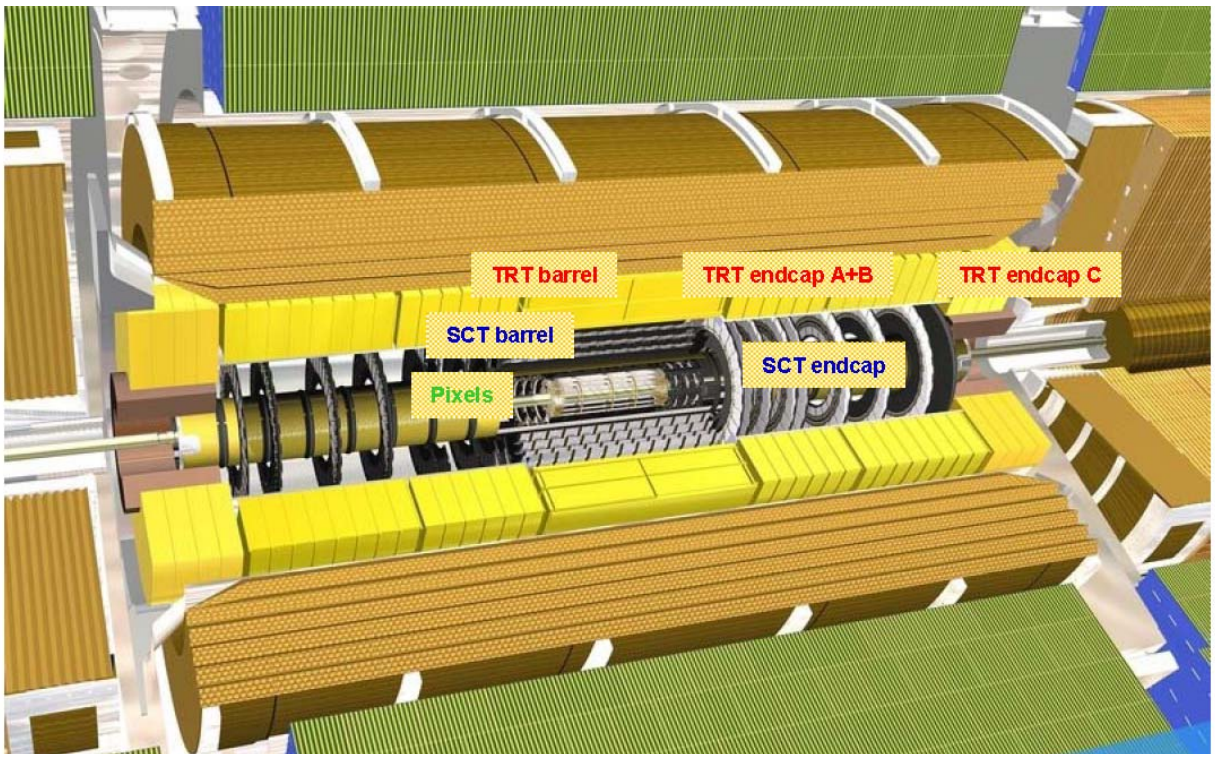
- Contains 420K electronics channels. Transition radiation detector gives particle ID.

Intermediate system is a large silicon strip tracker

- Four barrel layers and 9 disk layers contain 61 m^2 of silicon with 6.2M channels.

Innermost system is a silicon pixel tracker

- Three barrel layers and 3 disk layers contain 1.8 m^2 of silicon and 80M channels.



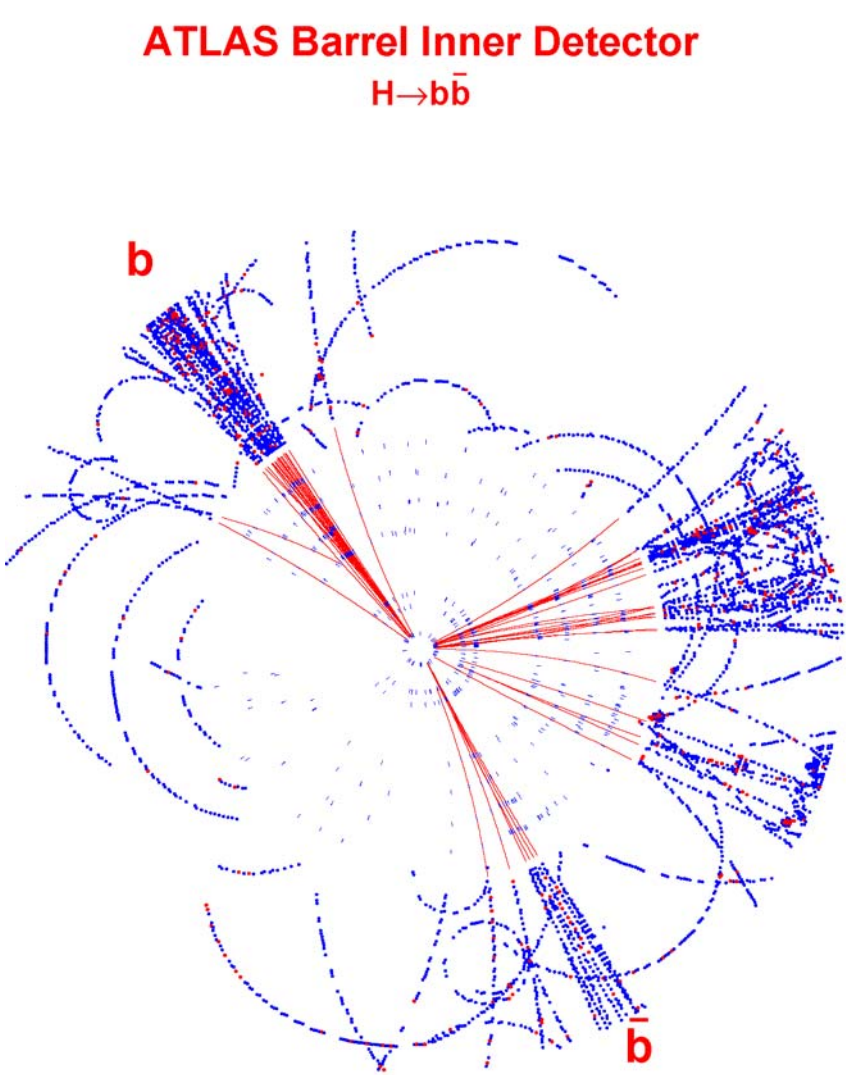
Tracking volume is about 7m long and has a radius of 1.2m

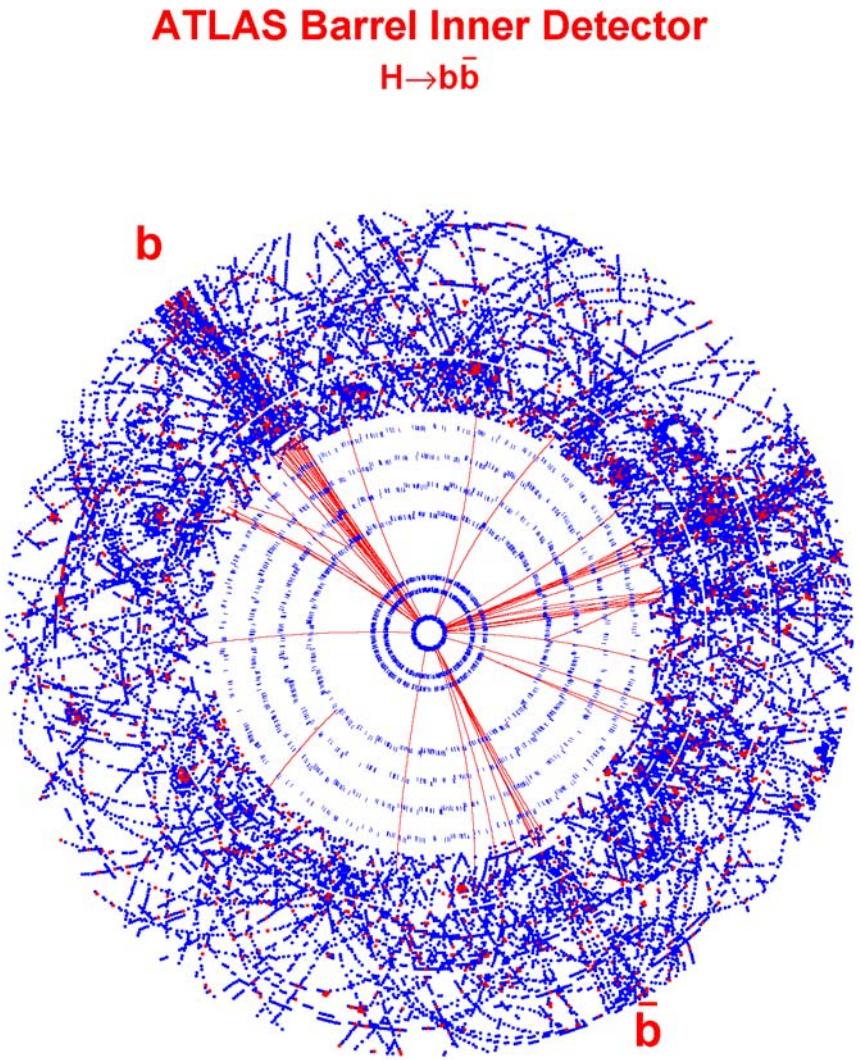
It is sitting inside a superconducting solenoid field of 2T.

Pattern Recognition in ATLAS Inner Detector

H → bb event at zero luminosity and at design luminosity:

- Vertexing and b-tagging will be challenging, and need pixel detectors !
  (Precision hits shown for $0 < \eta < 0.7$ only, TRT hits for $z > 0$ barrel only)





Requirements for Innermost (pixel) Tracking Layers:

Timing:

- LHC uses bunched beams at 40.079 MHz, there are 2808 collisions out of 3564 RF buckets available in the 90μs bunch revolution time, and bunch length is 200ps. All electronics and particle detection requires unique association with crossing ID.
- Meeting this requirement imposes a fast analog front-end design, with peaking time of about 30ns, as well as a complex readout architecture to associate many hits from contiguous crossings with unique crossing ID with very little confusion or loss.

Threshold, Noise, and Signal Size:

- Lifetime sensor dose of 10^{15} n-equivalent/cm^2 results in end-of-lifetime signal size of 10-15Ke. Final measurements on production sensors gives 13-15Ke at 600V.
- Charge-sharing effects then suggest a minimum in-time threshold (minimum charge for which a hit is associated with correct crossing ID) of about 5-6Ke.
- In-time threshold consists of true threshold plus overdrive required to produce a hit that is within 20ns of the time of a very large charge hit. Operating threshold would need to be 3-4Ke with less than 2Ke overdrive required to be in-time.
- Threshold dispersion plus variations due to temperature and radiation doses over periods of weeks should be less than about 500e. This, combined with noise of less than 400e, allows operation of large number of channels with noise occupancy well below 10^{-6} per pixel per crossing.

Other analog requirements:

- Electronics should remain within specs after lifetime dose of 50MRad.
- Ability to cope with leakage currents of up to about 100nA per pixel.
- Cross-talk (pulse height in reference pixel to fire its neighbor) less than 5-10%.
- Double-pulse resolution adjustable down to 0.5µs or less.
- Capability to provide modest resolution (4-6 bits) analog charge measurement.
- Highly integrated biassing scheme to allow full control of front-end without requirement for any analog signals to be generated outside the front-end chip.
- Charge injection system able to measure all relevant performance parameters.

Other readout requirements:

- Readout system able to store all hits for up to 3.2µs L1 latency.
- Readout system able to record and read out hits with incident hit intensity of up to 3-5x10^7 hits/cm^2/sec with efficiency of 99% or better.
- Event building scheme to allow high-quality checks of event integrity at different levels in the system, to avoid synchronization errors, or data corruption errors.
- Configuration system able to control detailed performance of individual pixels, but SEU-tolerant enough to avoid need to frequently reload configuration data.
- General SEU-hardening of all operational aspects of the on-detector electronics to allow reliable operation at highest beam intensities.

Advantages of pixelated silicon tracking in ATLAS:

- **Radiation tolerance:** greater segmentation of pixel detector reduces capacitance (giving better S/N, operation with smaller signals) and leakage current per channel.
- **Pattern recognition:** very low occupancy of pixel system (few 10^{-4} per crossing) optimizes pattern recognition with a small number of measurement planes, and minimizes confusion in critical vertexing function.
- **Space points:** System must provide high quality tracking with average of 23 14 TeV pp interactions occuring every 25ns (500-1000 charged tracks in pixel acceptance). Measurement of space points optimizes useful information for both fast triggering and for full pattern recognition.
- **Parametric performance:** small pixel dimensions in both x and z gives high point resolution for impact parameter using a single measurement plane.

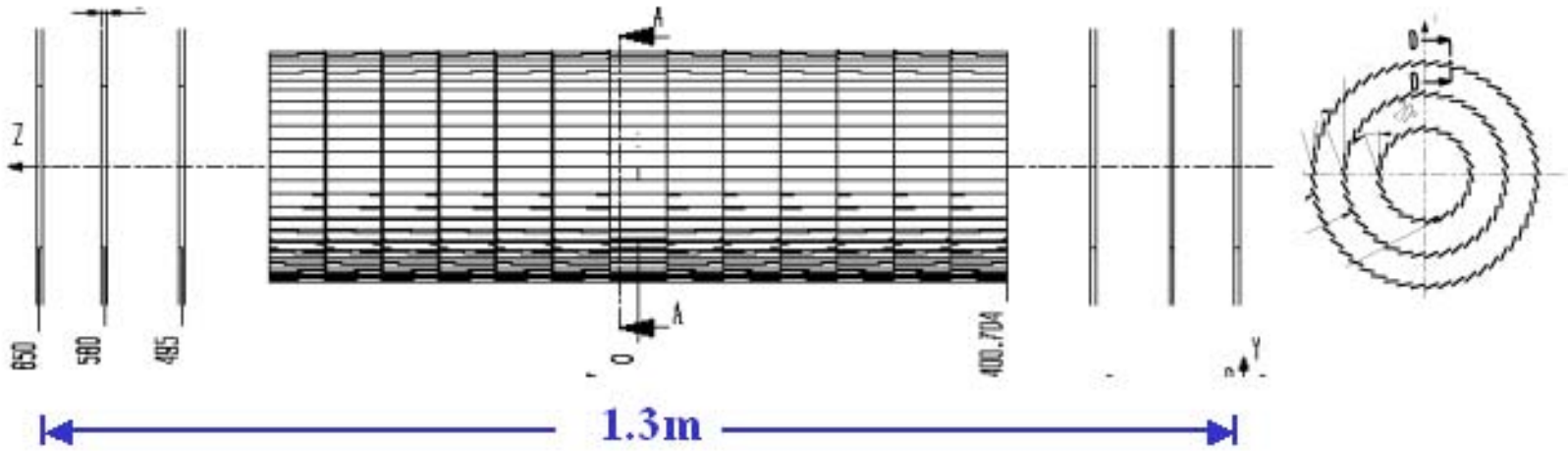
Why hybrid pixel design is the only solution for ATLAS:

- Optimization of sensor design suggests n^+ on n-bulk (or possibly p-bulk) as the only viable solution, primarily due to radiation dose and speed requirements. Need large 10ns electron current pulse to provide timing and reduce impact of trapping.
- Electronics requirements are complex, and appear to be achievable only through the use of state-of-the-art mixed-mode CMOS processes. Radiation hardness also requires thin (< 5-7nm) gate oxides found in 0.25μ or below CMOS.
- Further upgrades require even more highly optimized electronics and sensors.

Pixel Tracking in ATLAS

Pixel concept uniquely addresses many vital tracking issues at the LHC:

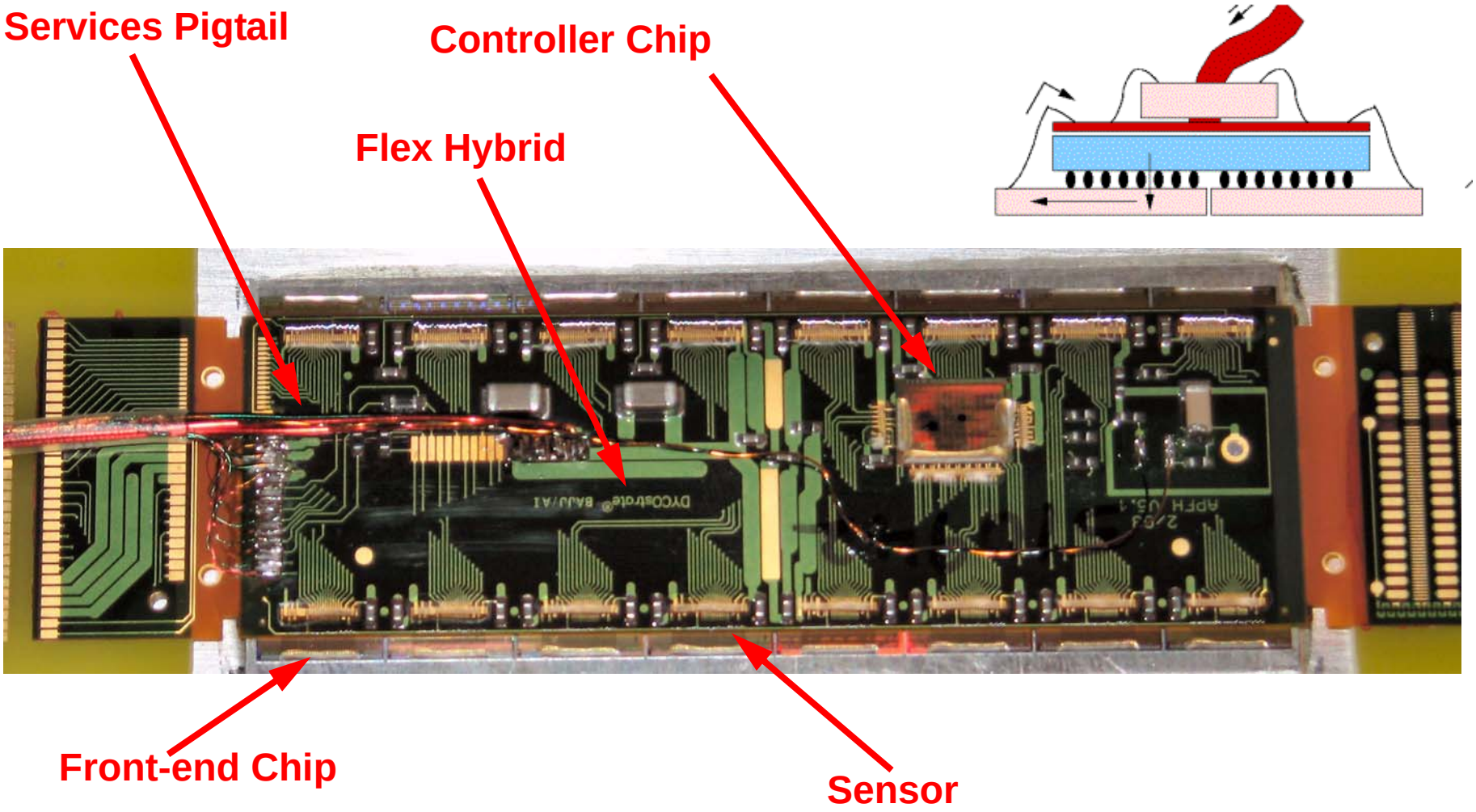
- **Layout:** outer part consists of 2 barrels with radii of 9 cm and 12 cm, plus 2 x 3 disks covering R = 9-15 cm and z = +/-65 cm. There is a small radius barrel at 5 cm ("B-layer") to optimize impact parameter resolution.
- Active area ≈ 1.8 m^2 with ≈ 80 x 10^6 pixels arranged into 1744 pixel modules, providing three hits per track to η = 2.5, one in B-layer, two in outer layers.



Basic Building Block of Pixel Tracker

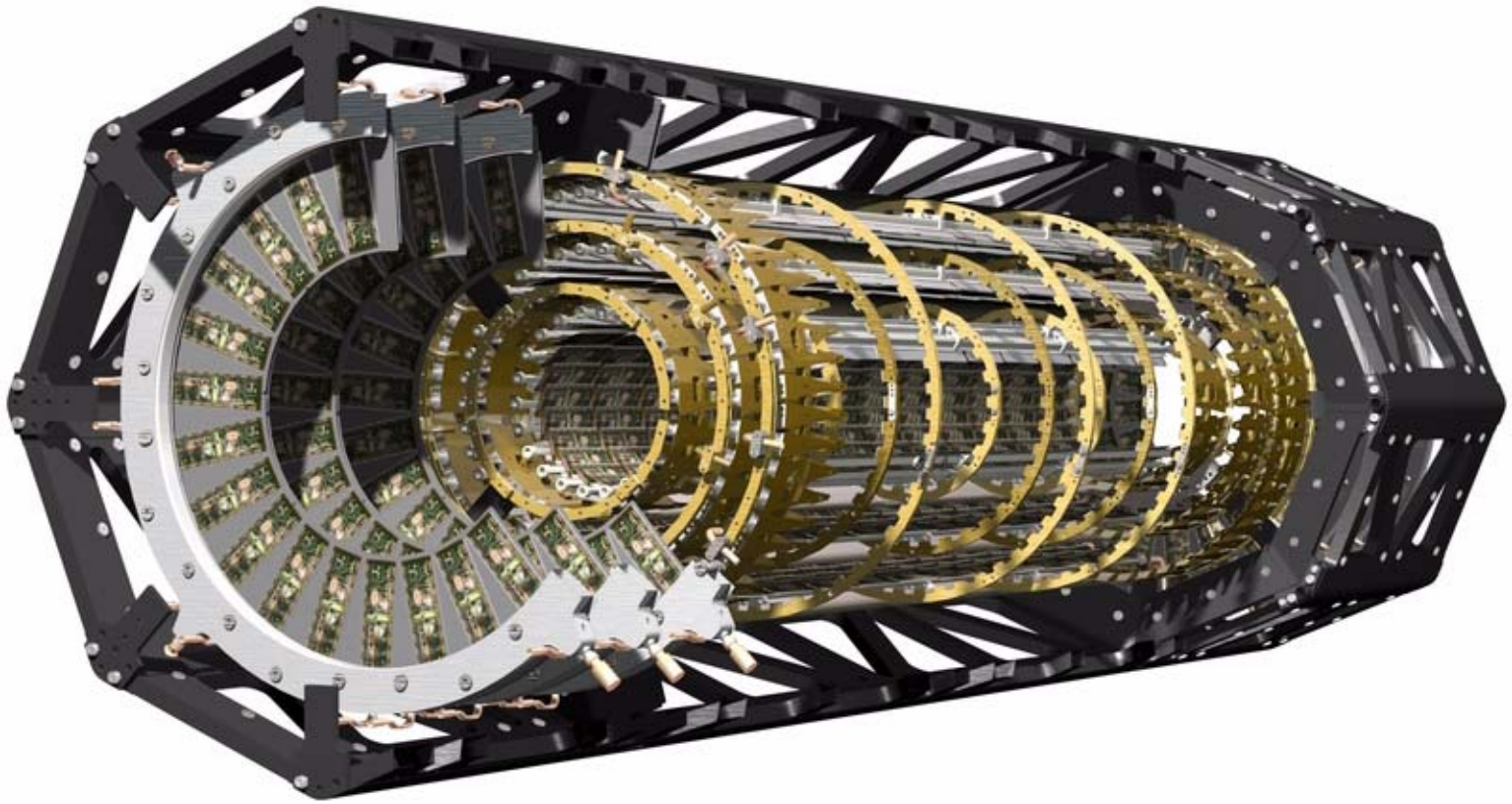
Modules placed on a mechanical support/cooling structure:

- Silicon sensor with 16 FE chips, Controller Chip, Flex Hybrid, and services pigtail:



- A total of 46080 channels in a 10cm^2 active area. Total footprint is about 14cm^2.

- Physical size of pixel tracker is roughly 1.6m long, with 0.2m radius. It contains 1744 modules, spread over three barrel layers (1456 modules) and three disk layers (288 modules).
- Innermost layer is at 5cm radius, providing best possible impact parameter resolution, within the limits of the beampipe radius.
- Operating temperature is -7C for modules, to preserve sensor performance. Use evaporative fluorocarbon cooling system operating at -25C to remove about 10KW.
- Typical power consumption during operation will be about 3500A at 2V.



Sensor Concepts

Basic requirement is operation after 10^{15} NIEL fluence:

- Requires partially depleted operation. Chosen n^+ pixels in n-bulk material as basic configuration (does require double-sided processing).
- Two isolation techniques have been studied for the n^+ pixel implants. First is conventional p-stop method. Second uses low-dose p implantation over the whole wafer (so-called p-spray). With p-spray technique, observe only bulk leakage in I/V curve after full dose (not true for p-stop), a bias grid can be used for wafer-scale testing, and no lithography between n^+ implants is needed.

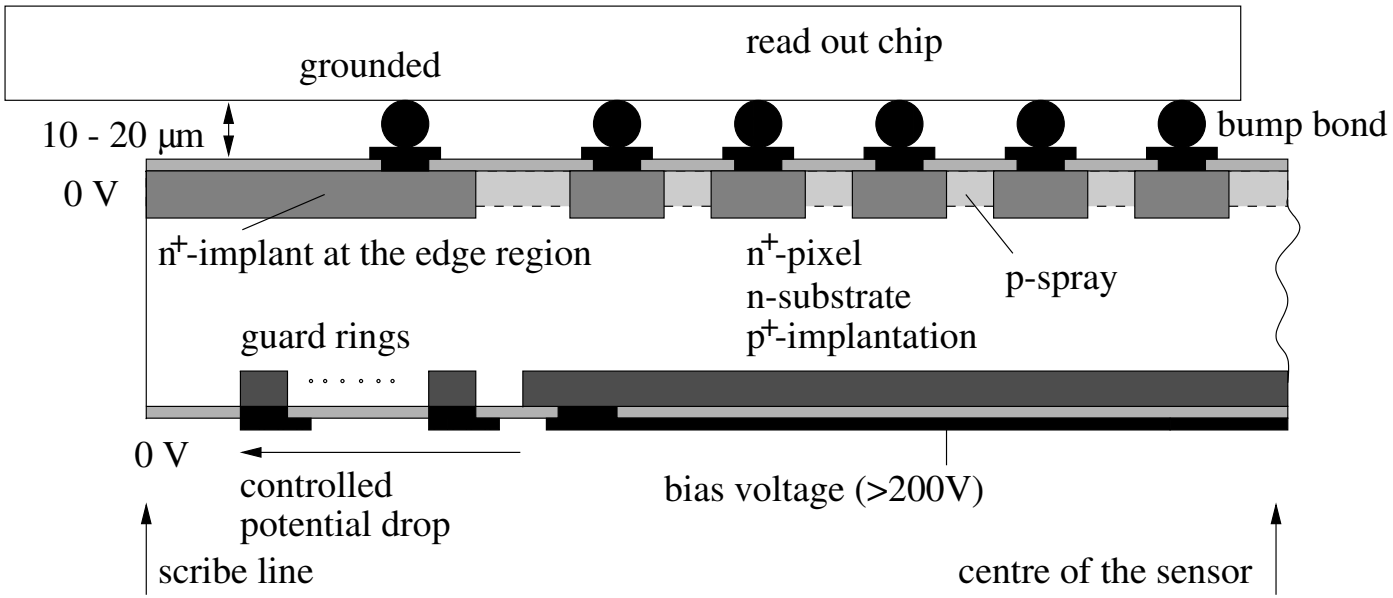


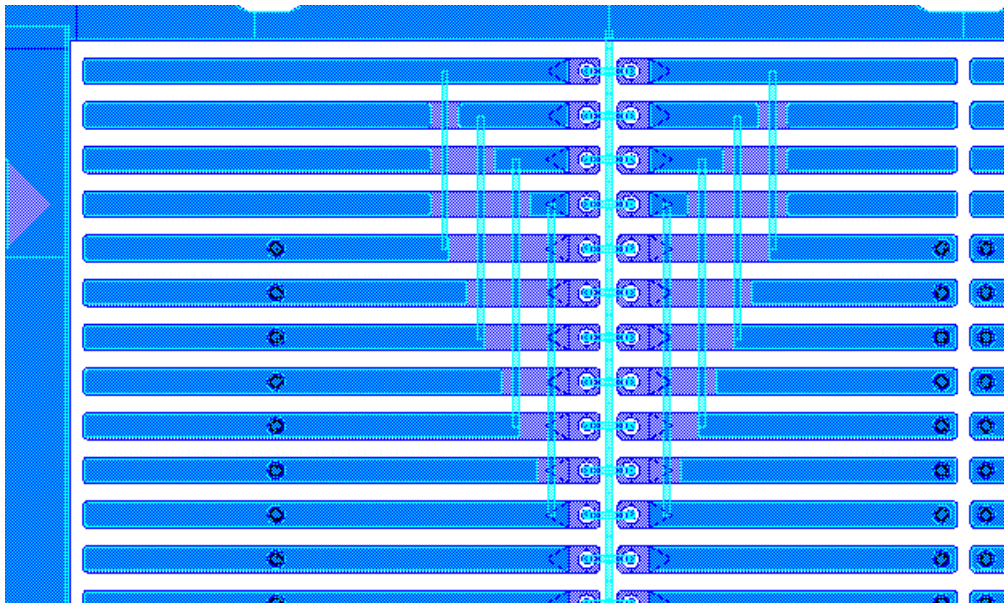
Diagram showing guard geometry near edges of module, designed to operate safely with bias voltages of beyond 700V.

Sensor Prototypes

Geometry of module:

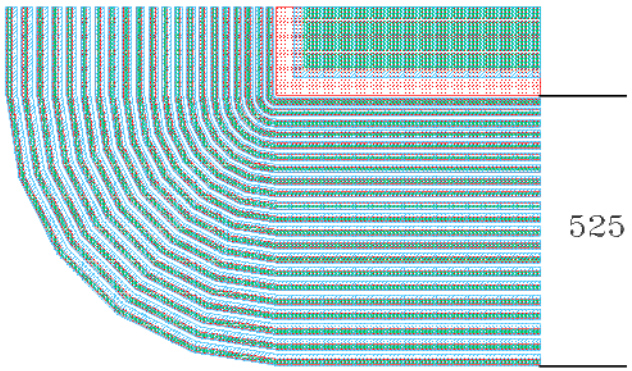
- Design has an active region of 16.4 x 60.8mm, containing 46,080 pixels of 50μ x 400μ. Thickness is 280μ in all layers. An additional 1mm non-active region is used for guard rings. Inter-chip regions are covered using special pixels, either long (600μ) or ganged (2 sensor pixels connect to one electronics channel).

Some highlights of the geometry:



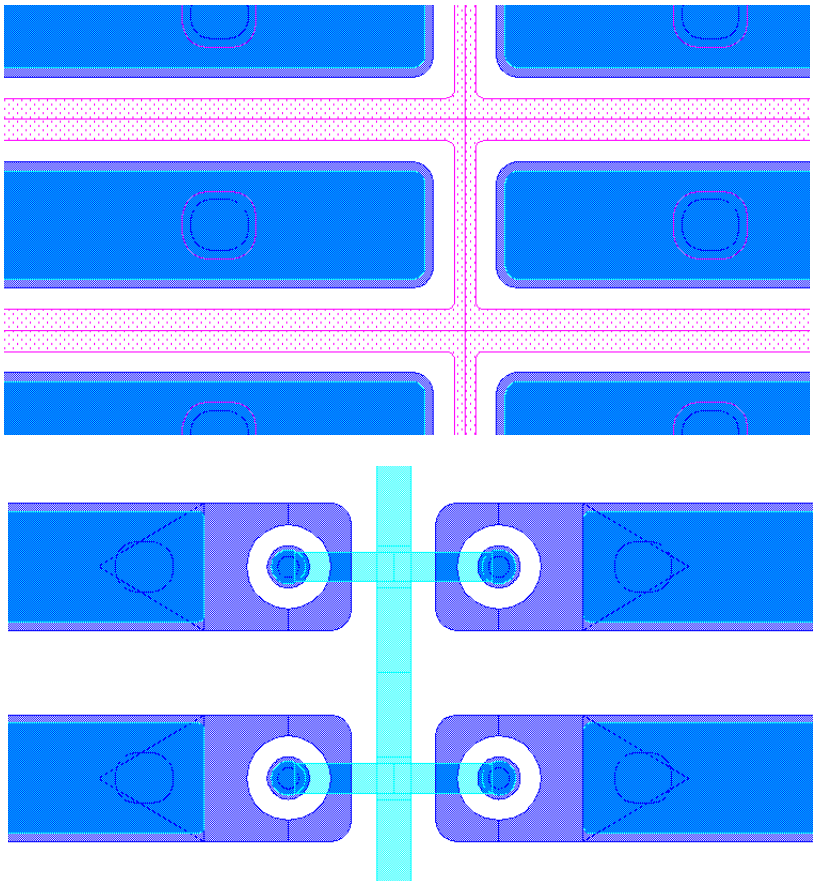
Special pixels in interchip region, including long, ganged, and long-ganged pixels, cover 400μ interchip gaps.

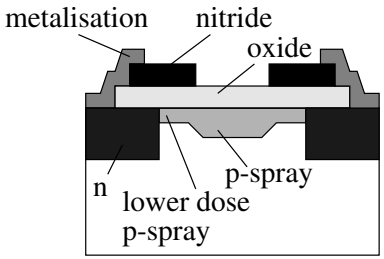
Multi-ring guard structure used to allow very high voltage operation.

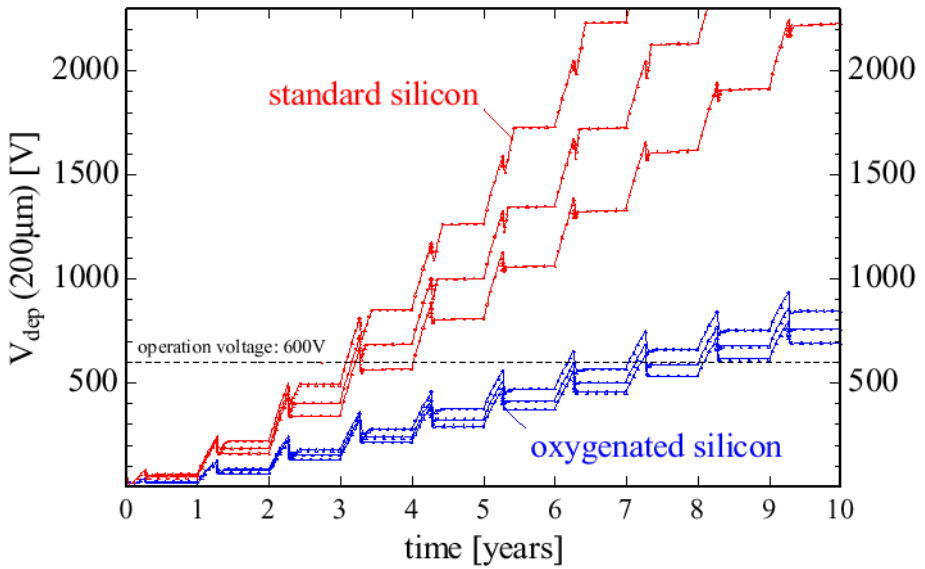


Final Sensor Design

- Final design uses 5μ bias dot for bias grid to allow testing and keep unconnected pixels from floating to large potential in case of bump defects. It uses moderated p-spray technique to improve pre-radiation breakdown. Oxygenated material is used to reduce post-rad depletion voltage and improve reverse annealing.
- Production wafer layout has 3 module tiles and many test structures in 4" wafer. Production with two vendors (CIS plus Tesla/ON), now almost complete:







FE Electronics Concepts

System Design:

- **Pixel Array:** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area contains 2880 channels. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is “requested” by sending a LVL1 signal with correct latency. FE chip then transmits the corresponding digital hits autonomously.
- **Module Controller:** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command and control. The 16 FE chips on a module connect in a star topology to the MCC to eliminate bottlenecks and increase fault tolerance.
- **Opto-link:** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are 8-way VCSEL arrays, receivers are 8-way epitaxial Si PIN diode arrays. Basic link is an 8-way MT-connectorized 7x3mm package. Electronics consists of 4-channel programmable current driver and 4-channel bi-phase mark decoding receiver chips with LVDS interfaces. The fibers are rad-hard silica core multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling used on module (local 0.1μF, global 10μF). Micro-cables reach end of detector at 1m (PP0), compact cables go to remote-sense rad-tolerant regulators at 16m (PP2), followed by conventional cables to US15/USA15 caverns (100m worst-case total cable length to modules).

History of Electronics Prototypes

Several generations of prototypes have been built:

- First “proof of principle” chips were built in 96 in commercial 0.8µ technologies.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C). These prototypes demonstrated the possibility of meeting LHC requirements at the single-chip and module level. Irradiated sensors were combined with rad-soft electronics.
- Two generations of complete chipsets were fabricated in DMILL rad-hard process in 1999 and 2000, but there were major technology problems, giving poor yield and inadequate radiation hardness. This technology was abandoned. Complete Honeywell SOI chip was ready to submit in Summer 2000, but huge cost increases resulted in abandoning that direction also. Total lost time about 2 years !
- Began 0.25µ design in Fall 2000. First complete chipset, including two types of FE chip (different gains), a Module Controller chip, opto-chips, and several test chips, was submitted to IBM in Nov 2001.
- All chips from this run were extensively evaluated, including irradiations in the CERN PS, and testbeam in the CERN SPS. A number of minor improvements were made, and a new generation was fabricated in Apr 2003.
- Final version submitted in Nov 2003, followed by production of 246 wafers. The testing of these wafers is expected to finish in the next few days. A total of almost 58K good die have been produced, over one year, with average yield of 82%.

Features of Final FE Design

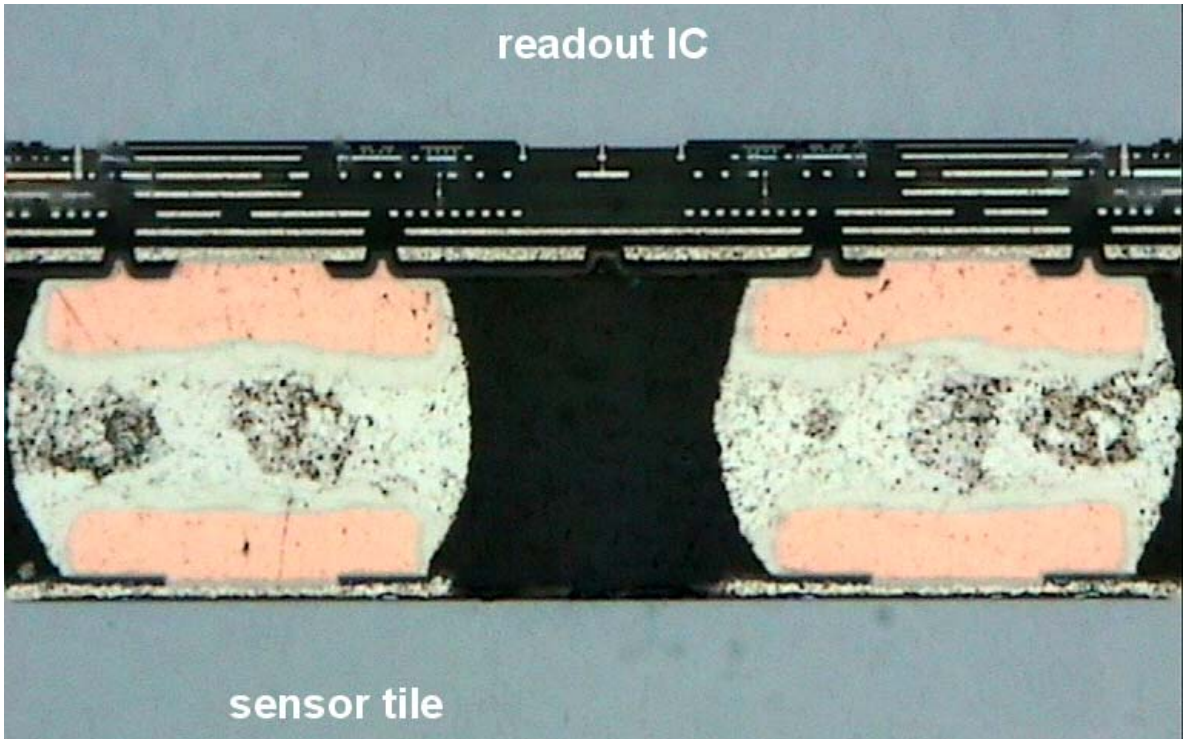
Analog Front-end (designed for VDDA=1.6V operation):

- The FE uses a DC-feedback preamp design which provides excellent leakage current tolerance, close to constant-current return to baseline for TOT, and very stable operation with different shaping times.
- The control logic provides 7-bit threshold trim (TDAC) in each pixel, plus a 3-bit feedback current trim (FDAC) for tuning the TOT response. There are four control bits, including Kill (shut down preamp), Mask (block hit readout), HitBus (enable global FastOR) and Select (enable charge injection), for a total of 14 bits.
- All critical bias currents and voltages on the chip are controlled by internal DACs. There are 11 8-bit DACs for the analog front-end, an additional 10-bit DAC for the charge injection, and a 10-bit DAC for leakage current measurement.

Digital Readout (designed for VDD=2.0V operation):

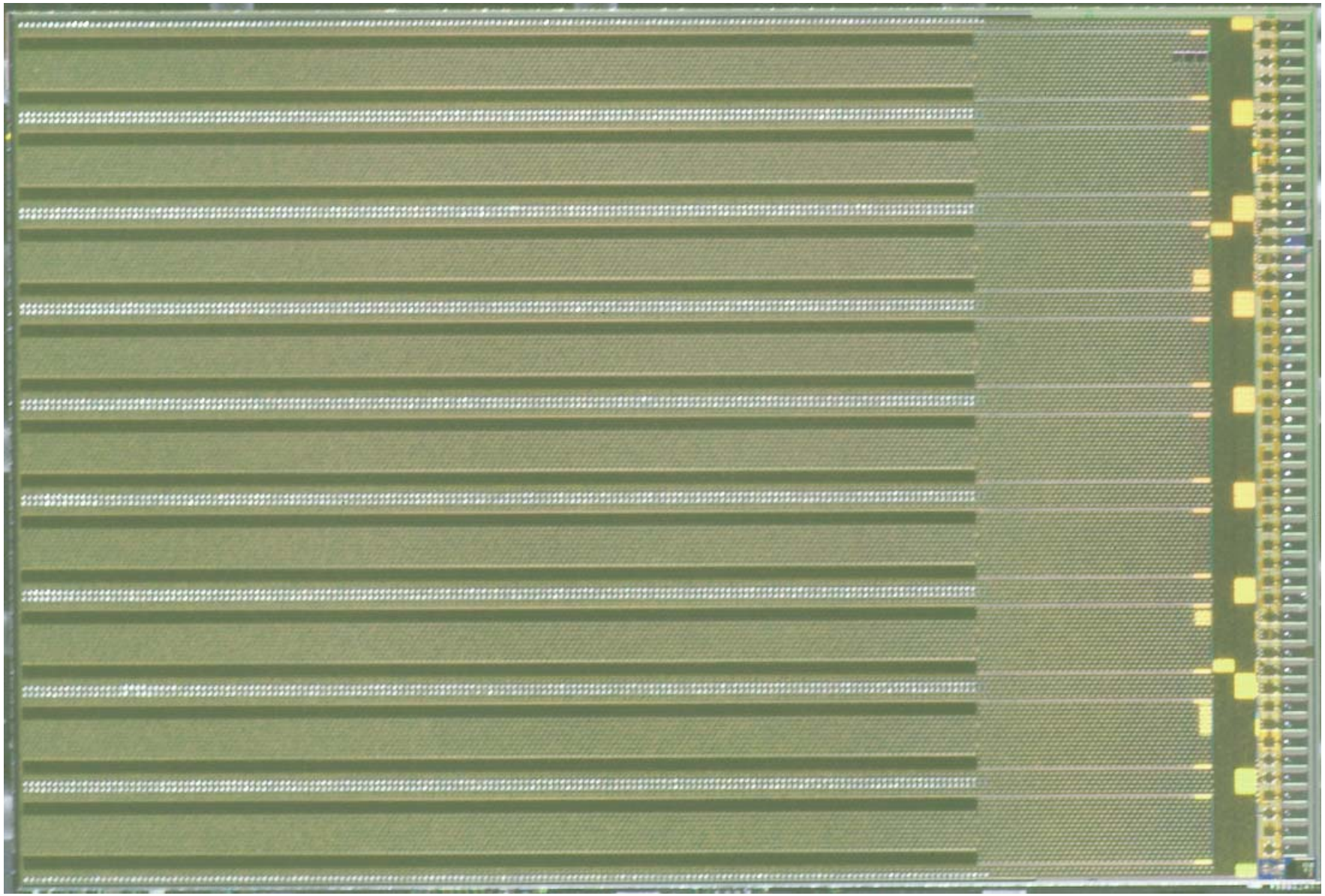
- It uses an 8-bit Grey-coded 40 MHz differential “timestamp” bus as a timing reference throughout the active matrix. All pixels measure their leading and trailing edge timing by asynchronously latching this reference in RAMs.
- Hits (address plus LE/TE timing) are transferred from the pixels as soon as the trailing edge occurs, using a shared bus structure in the pixel column pair. This bus operates at transfer rates up to 20 MHz in order to meet our requirements. Differential signal transmission and sense amplifiers are used to achieve this.

- Significant buffering is provided in the end of column region for hit storage during the L1 latency (up to 6.4μs in this chip). Sixty four buffers are available for each column pair (one for each five pixels). The coincidence with the L1 trigger is performed in this buffer. Hits from rejected crossings are immediately cleared.
- A readout sequencer stores information on up to 16 events pending readout. As soon as the output serial link is empty, transmission of a new event begins. Essentially, sending a L1 trigger corresponds to making a request for all hits associated with corresponding beam crossing.
- FE-I3 (production version) has 3.5M transistors in 80mm^2, MCC-I2.1 (production version) has 650K transistors (33K cells) in 25mm^2



- Section shows 25μ diameter Solder bumps connecting sensor (bottom) and FE chip (top).
- Sensor and electronics are separated by only 10-20μ.
- Can see single-metal sensor design and six-metal CMOS

FE-I3 Front-end Chip with bumps:



- Top two metal layers are largely dedicated to shielding and VDDA bussing.

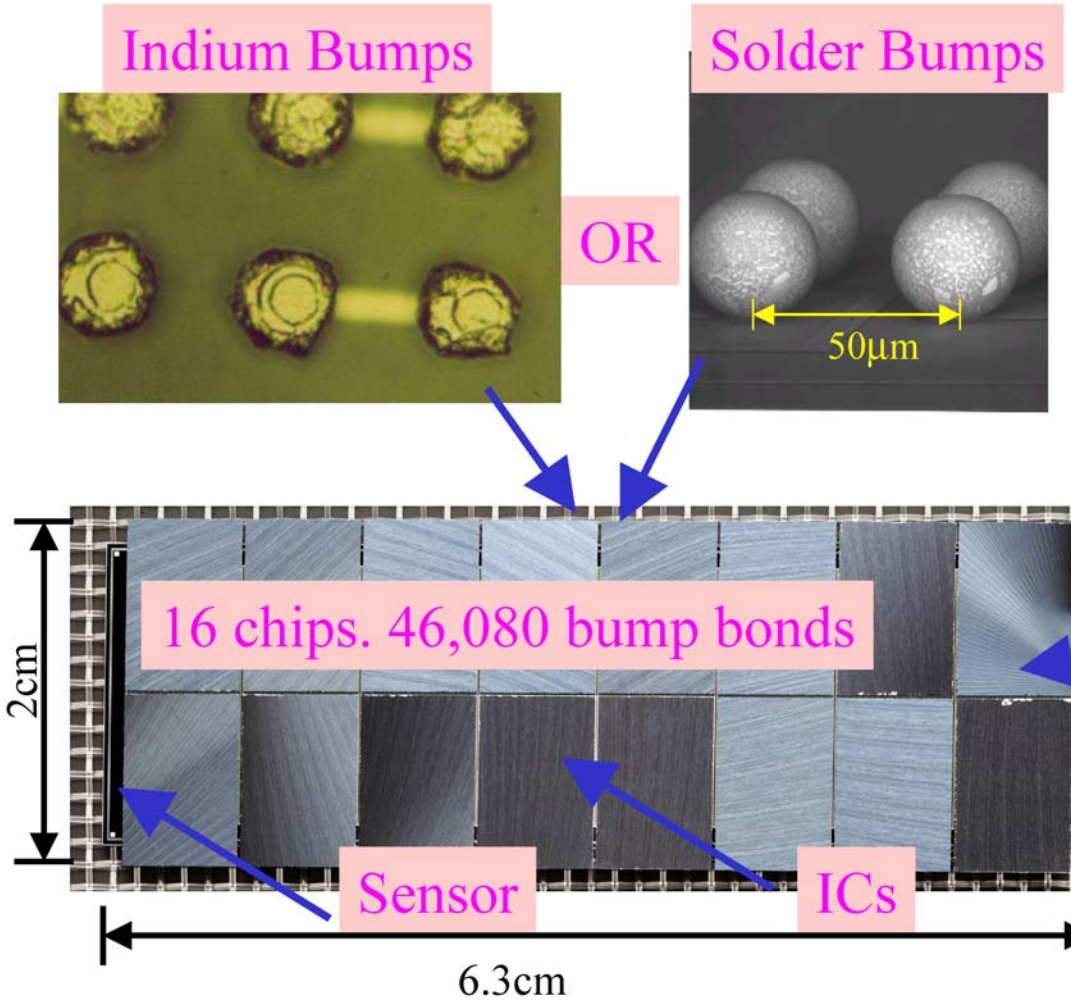
Front-end Chip Testing:

- Perform extensive testing of each die on wafer in order to ensure high-yield multi-chip modules. Test again after bumping, thinning, and dicing. Test again after receipt of “bare module” (sensor + 16 FE chips assembled). Wafer test list:
  - Check initial and operational supply currents
  - Check all control registers for bit errors
  - Characterize current references and DACs using external DVM
  - Measure test structure with injection and feedback capacitors
  - Do digital hit injection scans under different conditions, and check TOT processor
  - Do autotune threshold tune and check resulting TDAC distibution
  - Do threshold scan and check dispersion and noise
  - Do digital and analog TOT scans, and check FDACs
  - Check threshold versus GDAC setting
  - Check in-time performance with digital injection
  - Check error reporting bits
  - Check feedback currents using Monleak scan
- Complete test sequence takes about 8 minutes per FE chip, so a wafer is scanned in two days. All features of the FE chips that will be used during operation are checked. Only a few defective pixels are allowed for any given test. Approximately 150 cuts are applied to select good die. The average yield is 82%.
- All electronics testing, from FE chip on wafer, through module, and local supports is tested with a single common test system developed in parallel with chip design.

Pixel Module Interconnection

Assembly of Pixel Module:

- Key steps are bump-bonding and flip-chipping. Two vendors chosen: AMS (Rome) does Indium bumping, and IZM (Berlin) does solder bumping.



Basic unit is Bare Module, with sensor + 16 FE chips.

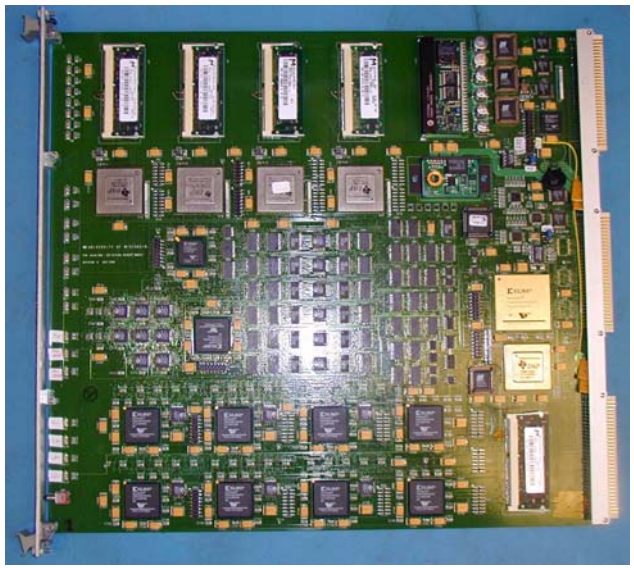
Active area is 10 cm^2, contains 46,080 channels with pitch of 50µ.

Beyond commercial pitches (200µ) Work with non-standard vendors.

Off-Detector Electronics

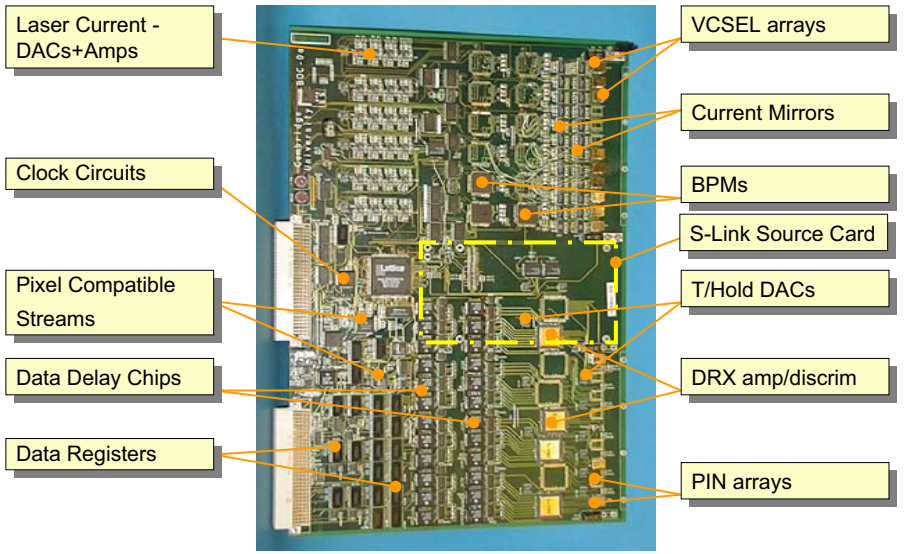
Pixel system uses high performance readout system:

- Must support maximum 100KHz L1 trigger and readout rate. This is done by using 132 9U VME modules, each with 1.6Gbit/s optical link outputs into TDAQ system.
- Provides integrated control and distribution of 40MHz clock and trigger, plus formatting of output data, on single board. Opto-interfaces on VME transition card.
- Real-time processing done by large number of Xilinx FPGA (12 per board). Higher level intelligence provided by C61 fixed-point Master DSP for control and four C67 floating-point slave DSPs for monitoring, analysis, and calibration.
- Significant capabilities implemented for detecting and repairing synchronization and SEU errors on the fly, without significantly disrupting data taking operations.



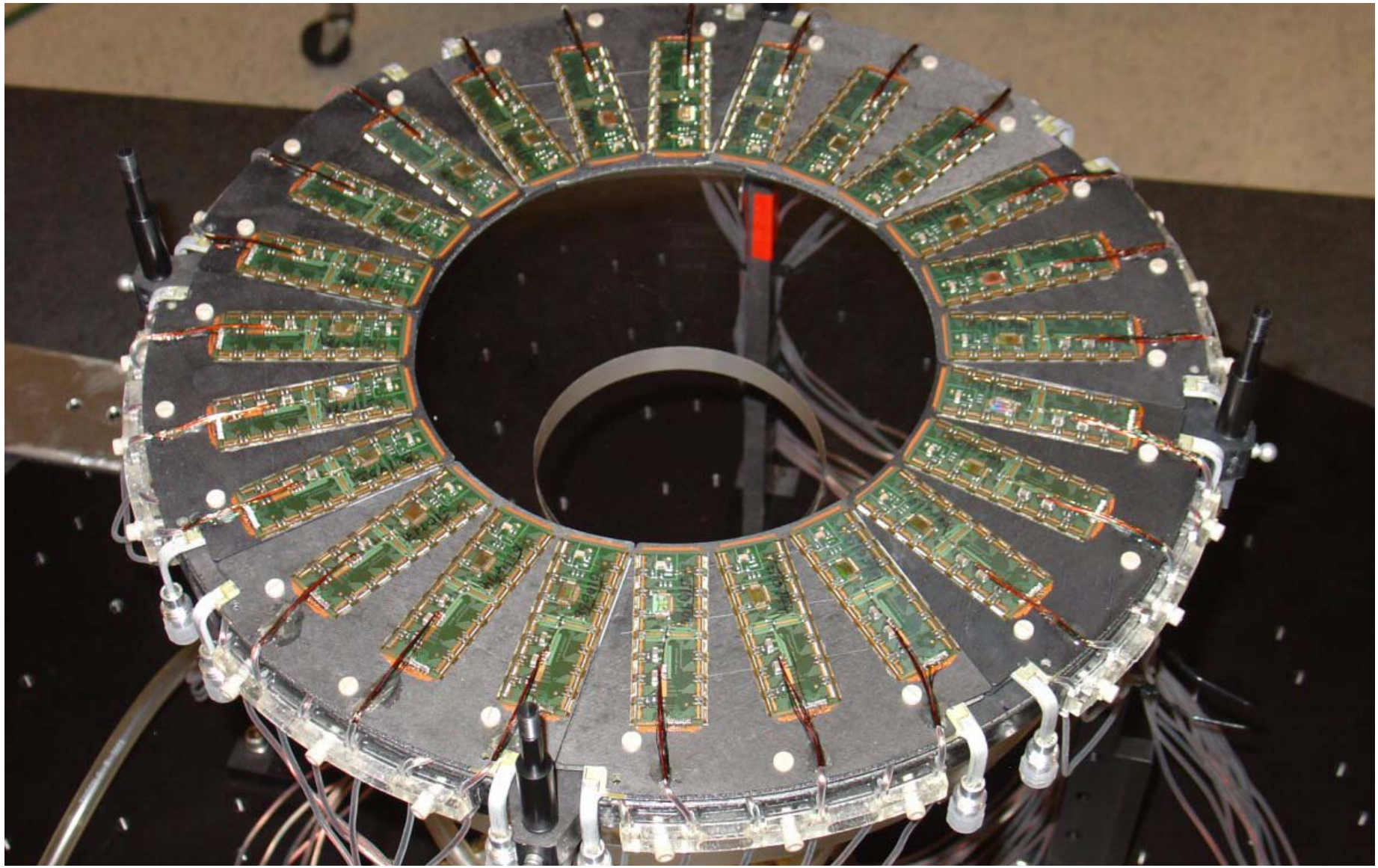
ROD (ReadOut Driver)

BOC (Back-Of-Crate Card)



Pixel Detector Assembly

Assembly of First Complete Disk:

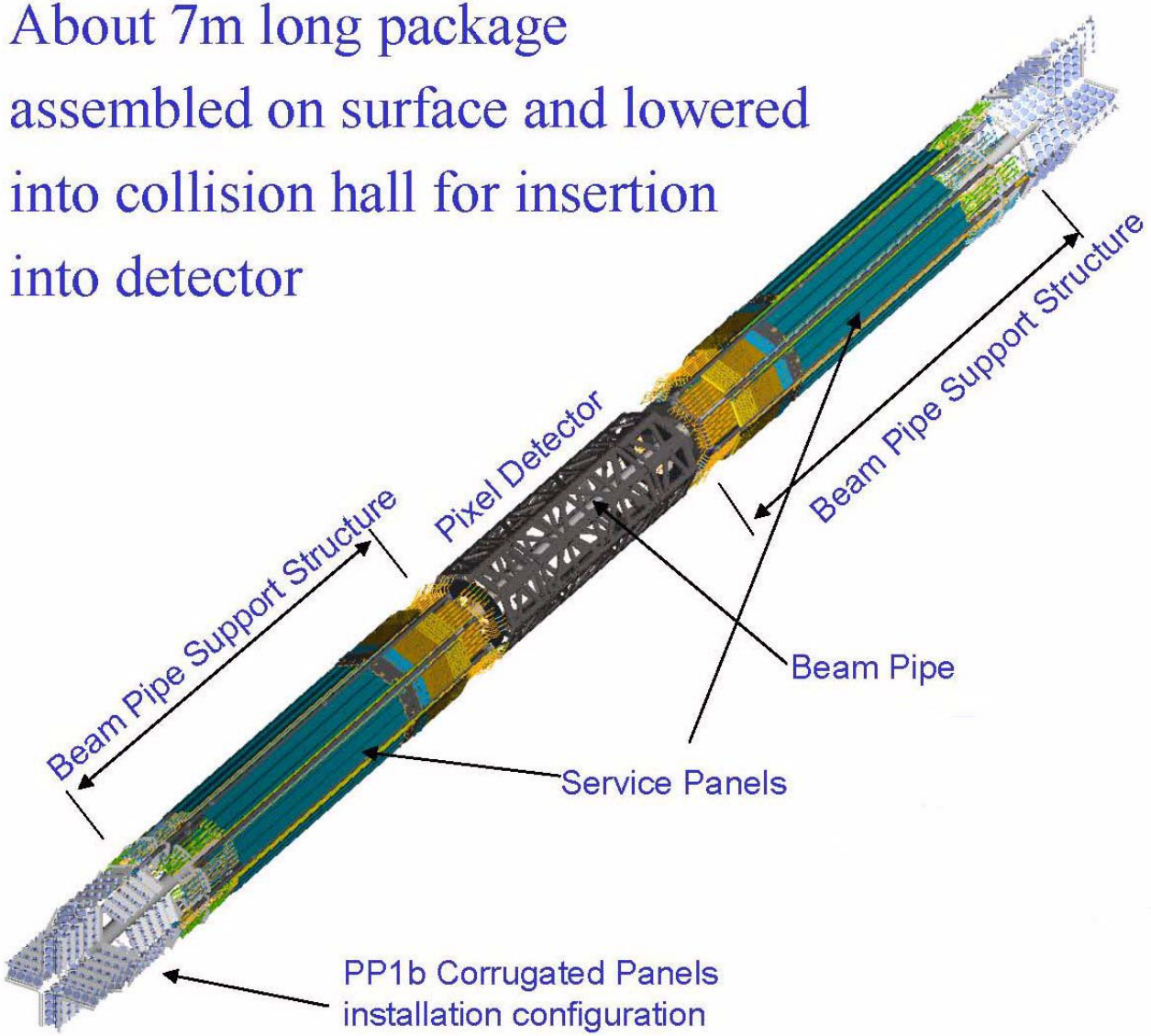


- Total of 48 modules (24 top, 24 bottom), 2.2M pixels. Largest assembly so far.

Overview of Pixel Mechanics

Pixel Package is deliverable to ATLAS, installation in Oct 06:

About 7m long package assembled on surface and lowered into collision hall for insertion into detector



Package includes:

Pixel detector in Global Support Frame

Service panels, containing connections for electrical, optical, and cooling services.

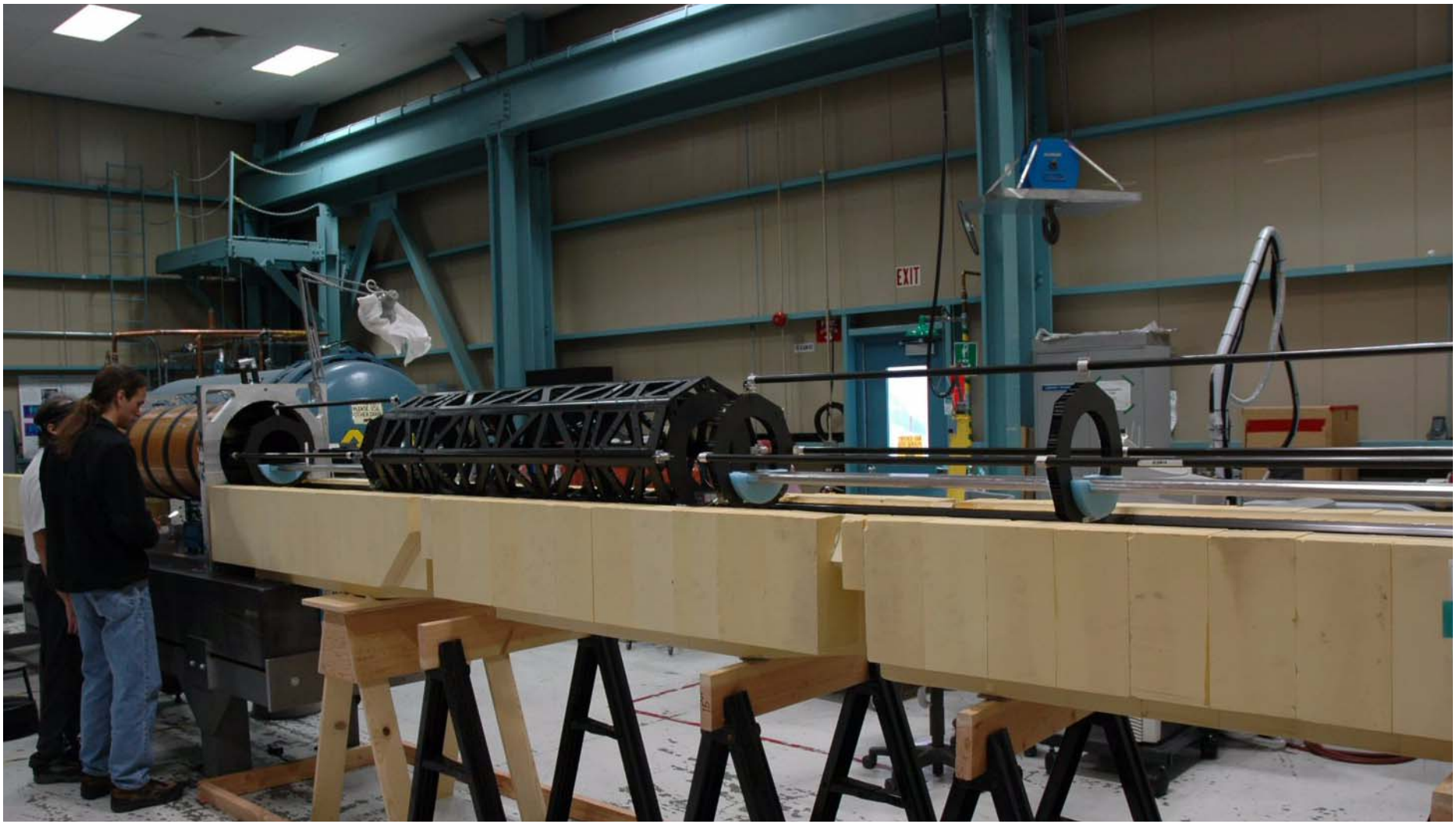
Beampipe (VI) and Beampipe Support System (BPSS).

Pixel Package is then lowered into UX15 inside of DST (Dummy Support Tube), and slides into PST (Pixel Support Tube) pre-installed into SCT.

- Global Support, Service Panels, BPSS, and PST are all LBL deliverables.

Trial fitting of pixel mechanics:

- Test integration of Global Support, Services Supports, dummy beampipe, and trolley plus rail system used for pixel insertion is ongoing this week in Building 77:



- Mechanics of pixel package are being rolled into central portion of PST.

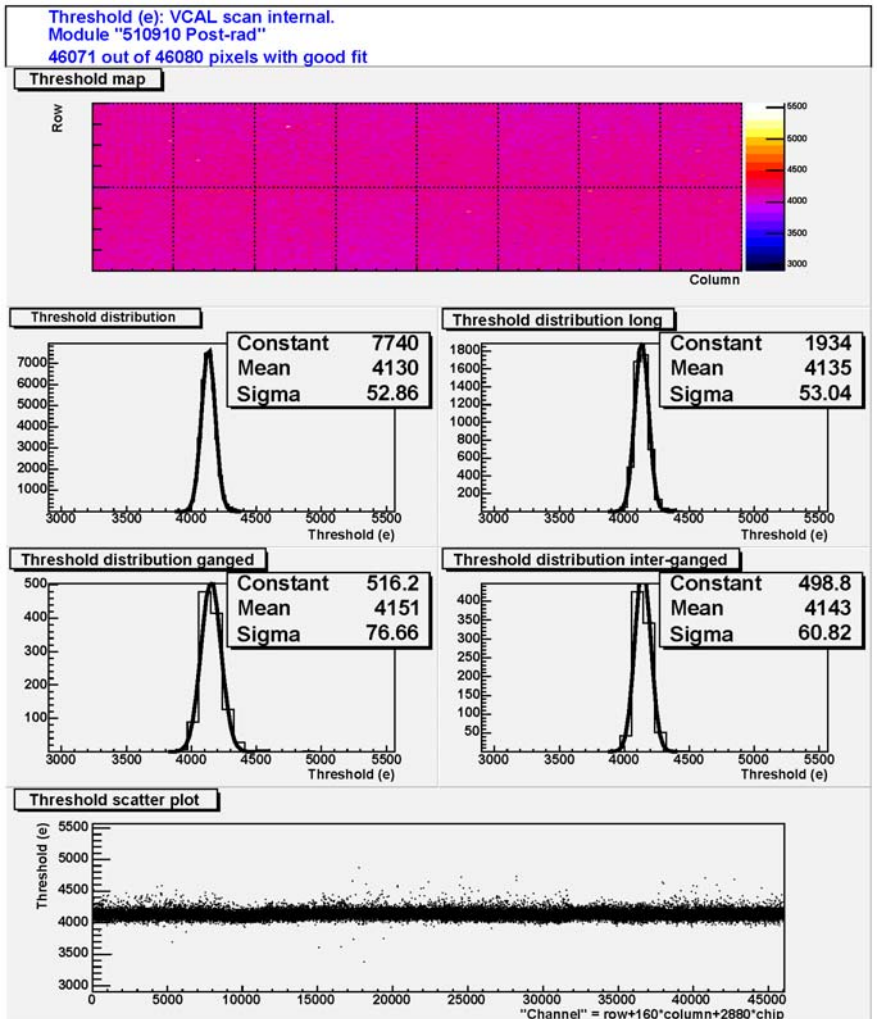
Current Status of Pixel Construction:

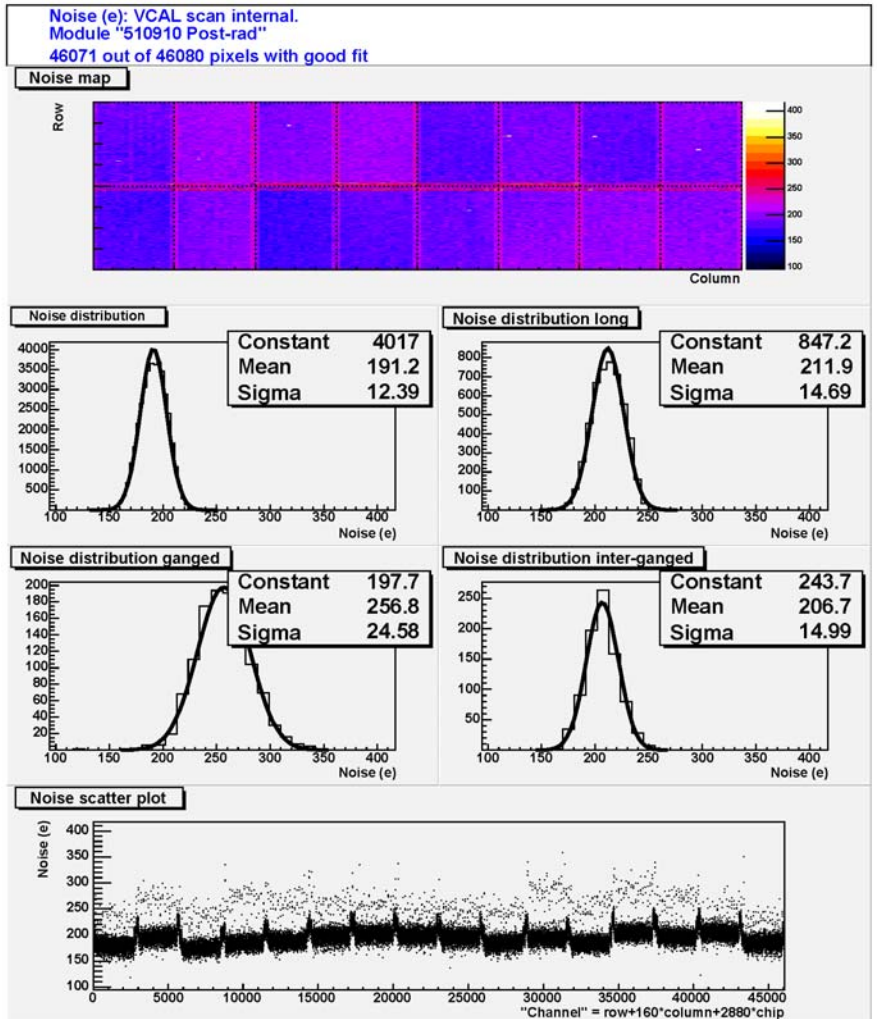
- Wafer probing of electronics will be completed in a few days.
- Off-detector electronics production is underway, will be complete by Summer 05.
- A total of about 700 bare modules have been accepted from bumping vendors.
- About 500 pixel modules have been assembled and tested (about 25% of total).
- A total of 20 disk sectors (out of 48 needed) and 20 staves (out of 112 needed) have been assembled and are partially or completely tested.
- Most of the necessary mechanical objects, including local supports and global mechanics, have been built and tested.
- Services are in production or in procurement. Installation from June - Nov 05.
- Expect to complete assembly of two “endcaps” (3-disk assemblies) by Dec 05.
- Expect to complete assembly of six barrel half-shells by Apr 06
- Plan to integrate complete detector with services from May-July 06.
- Will carry out complete electrical testing on surface, and will be ready to install into ATLAS in Oct 06.
- Current LHC schedule calls for closing machine vacuum in Apr 07, and circulation of single beams in July 07.
- Expect short collider run in Fall 07, with potential for integrated luminosity in the range from 1 pb^{-1} to $1fb^{-1}$

Performance of Production Pixel Modules

Threshold and noise performance:

- Measure threshold and noise for each channel by stepping injected charge through 200 values, with 100 injections each. Fit resulting histograms with error functions.

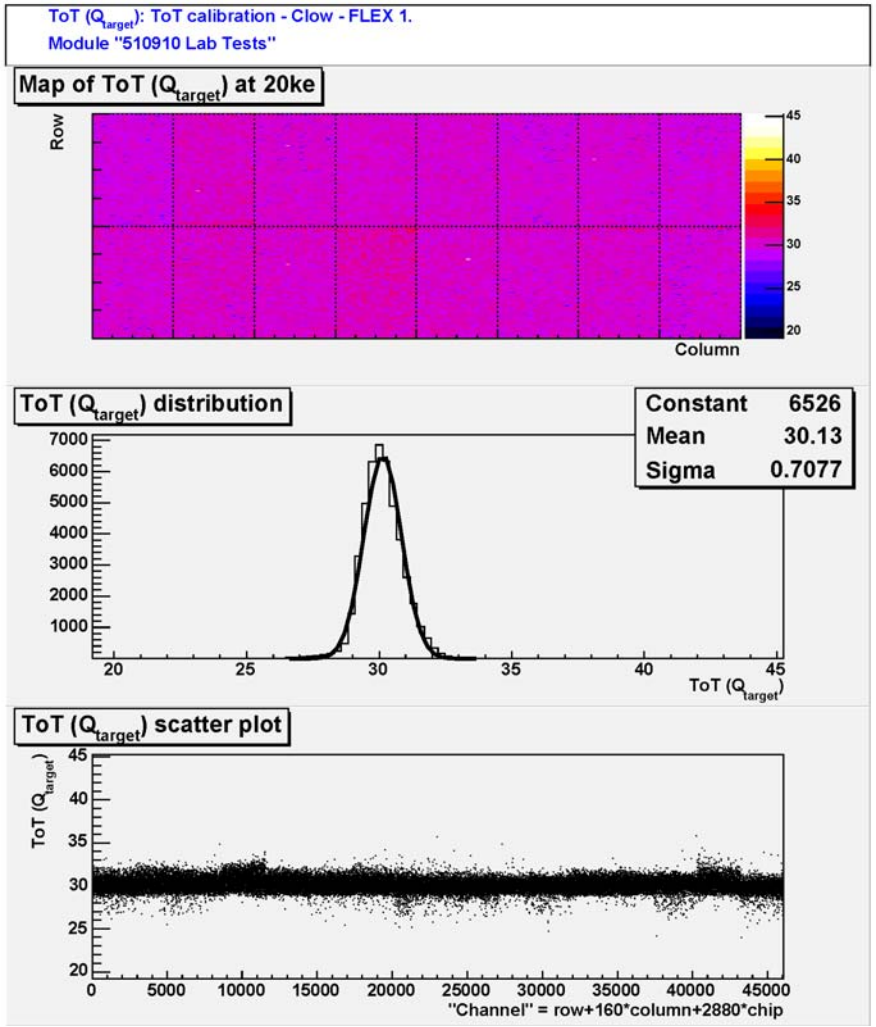


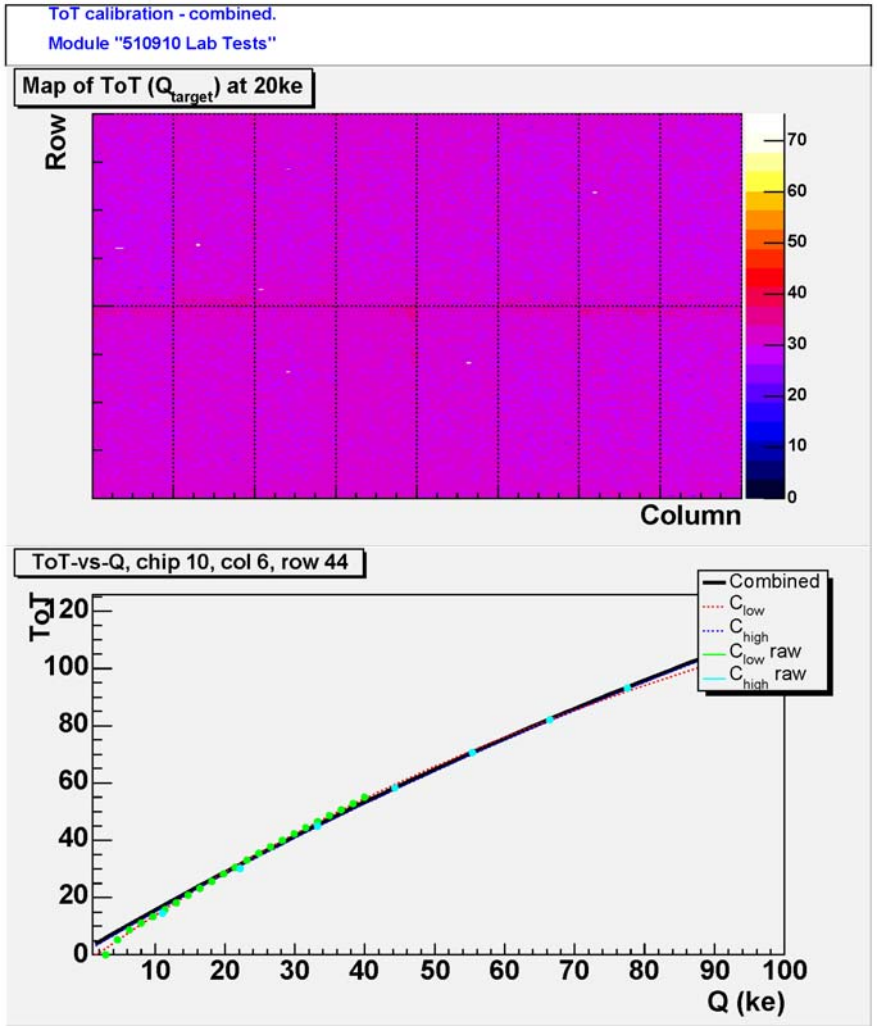


- Left plot is threshold, right plot is noise. Module was irradiated to 50MRad dose.

Charge (TOT) measurement and calibration:

- Left plot uses injection of fixed charge (20Ke) into each pixel to tune individual feedback currents for uniform charge response. FDAC is only 3-bit, so not perfect.

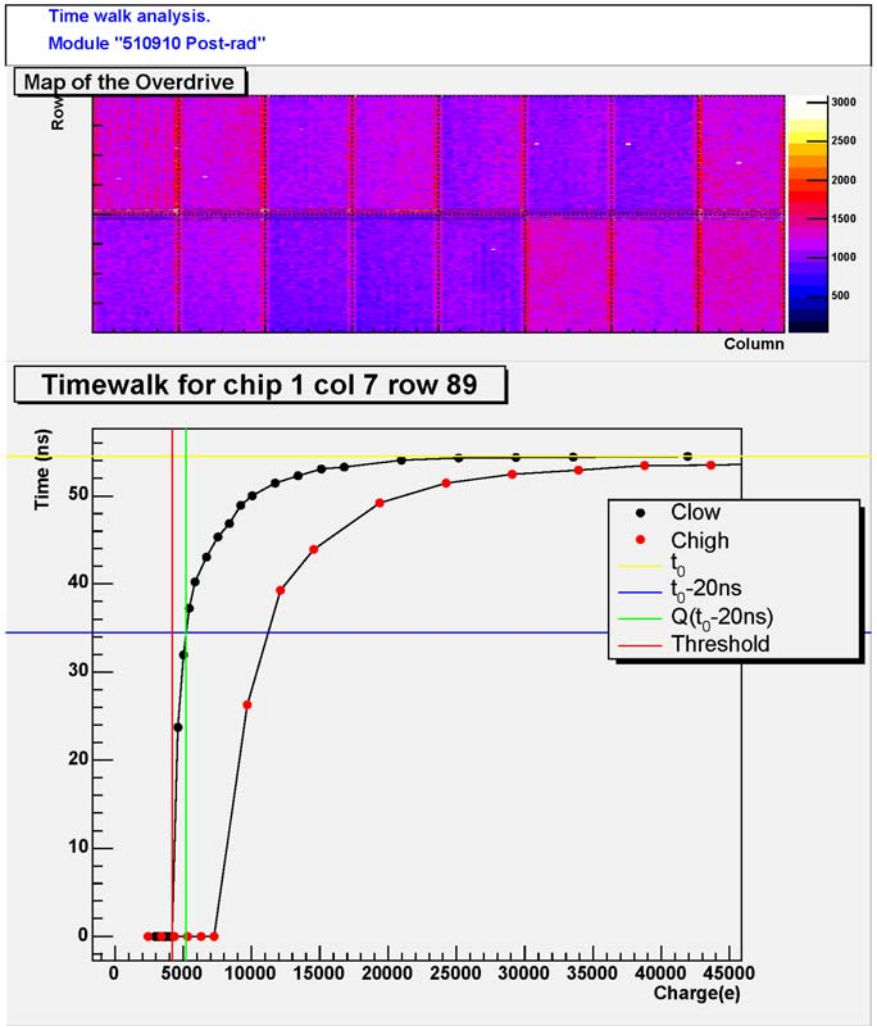


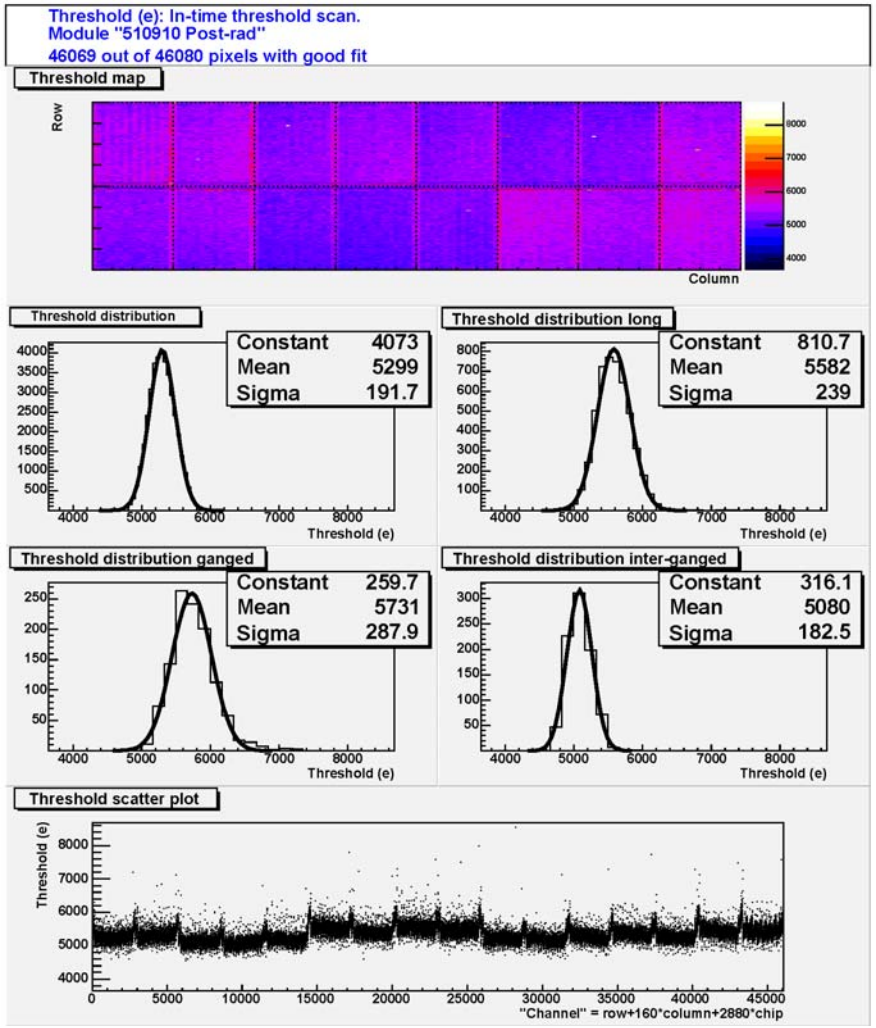


- Right plot shows map of fit results, as well as a typical curve for one pixel. Low injection capacitor covers range to 40Ke, high capacitor covers to about 200Ke.

Measurement of timing performance:

- Left plot shows timing response as a function of injected charge. Map is overdrive (charge above threshold required to be in-time = 20ns later than 100Ke charge).

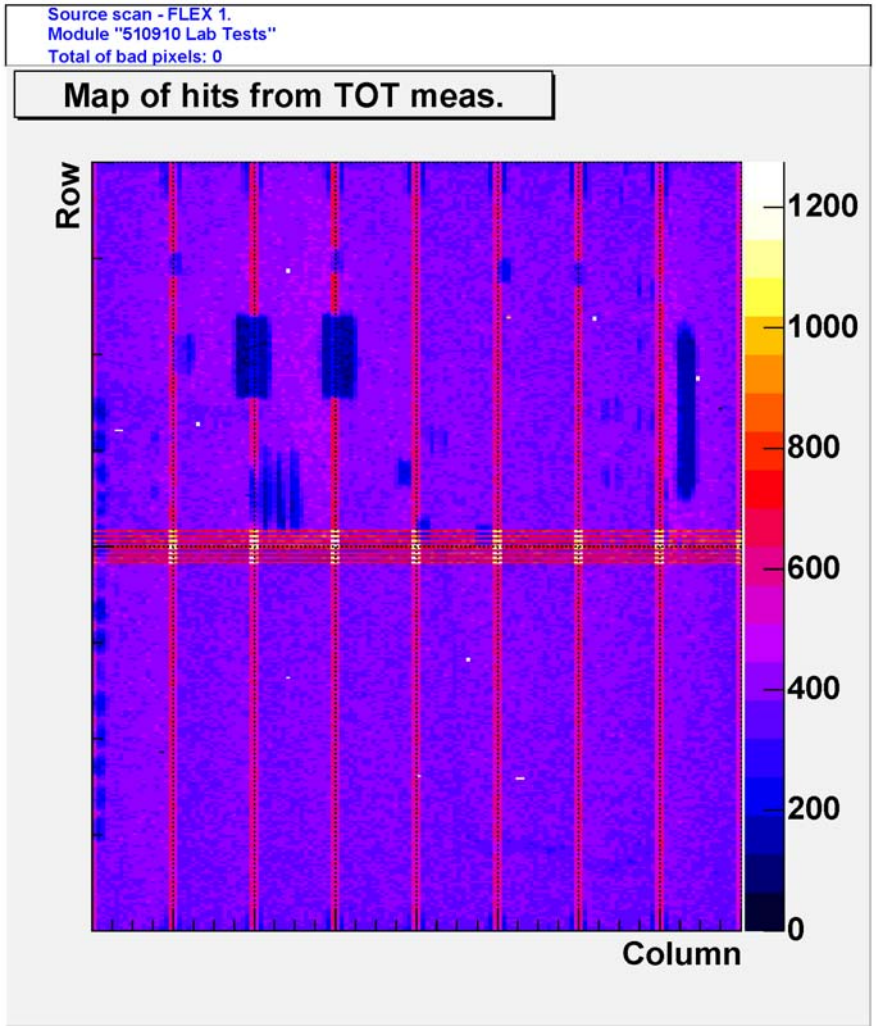


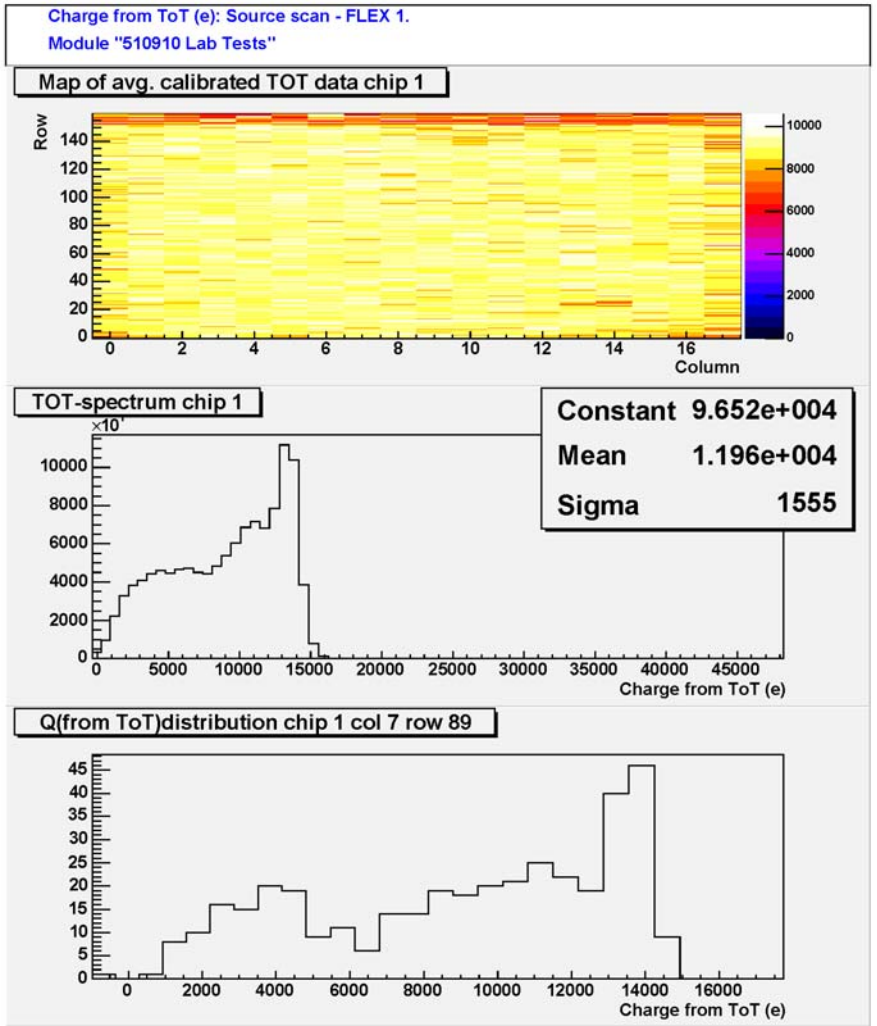


- Right plot shows result of in-time threshold scan, with timing set as it would be in real operation, and data read out only for a single crossing.

Self-trigger operation with Am241 X-ray source:

- Left plot shows hit map for self-trigger run with Am241 60KeV source. See shadowing by passive components on flex hybrid, and see four types of pixels.

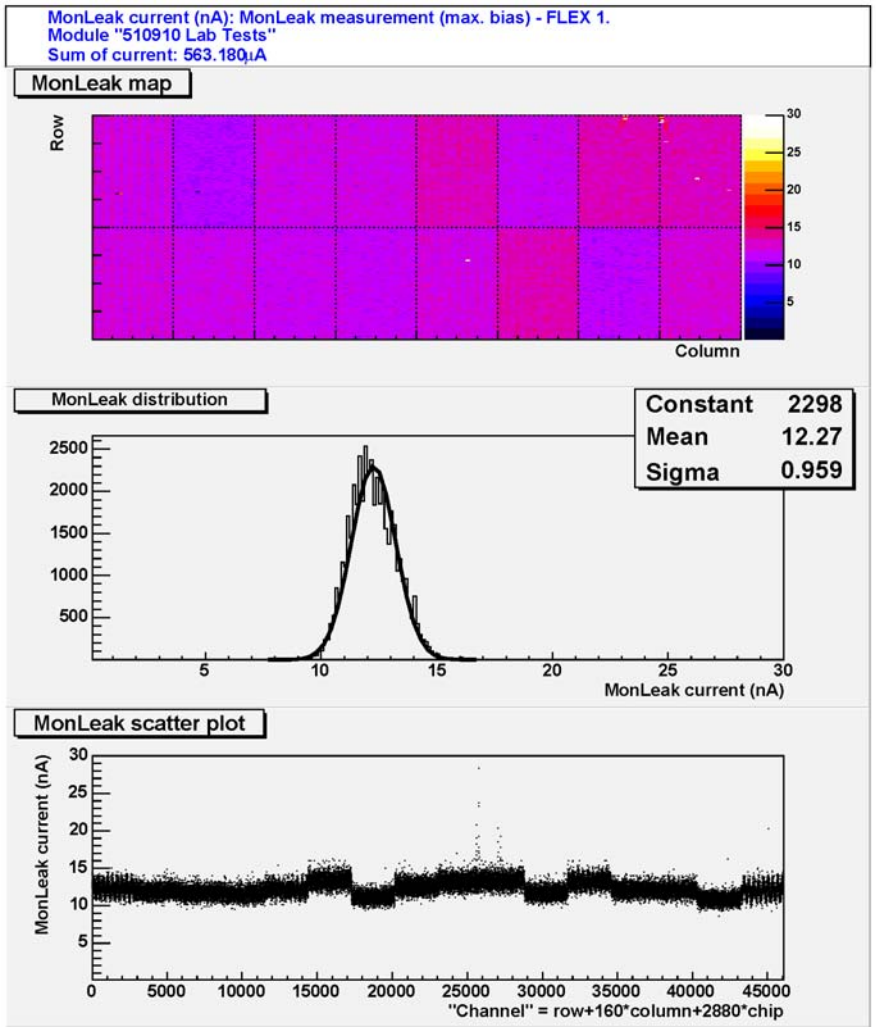


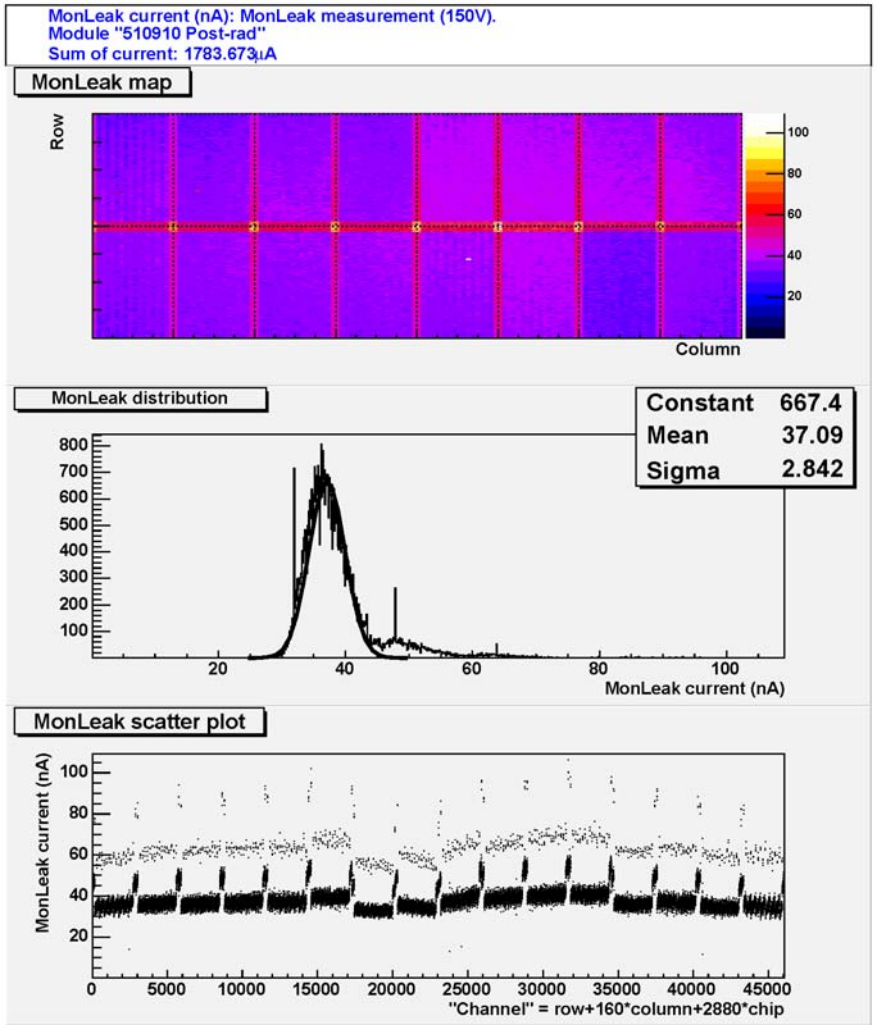


- Right plot shows average TOT distribution for one chip (middle plot) and the TOT spectrum for one pixel (lower plot), showing the Compton peak, should be at 16Ke.

Measurement of feedback current and leakage current:

- Left plot shows measured leakage current for each pixel before irradiation. In this case, the circuit measures roughly twice the feedback current of roughly 6nA.





- Right plot shows leakage current after irradiation to 50MRad, at operating temperature of -7C. Normal pixel has about 25nA, long-ganged pixels have 80nA.

Irradiations and Stand-alone Testbeam (at CERN):

Irradiations:

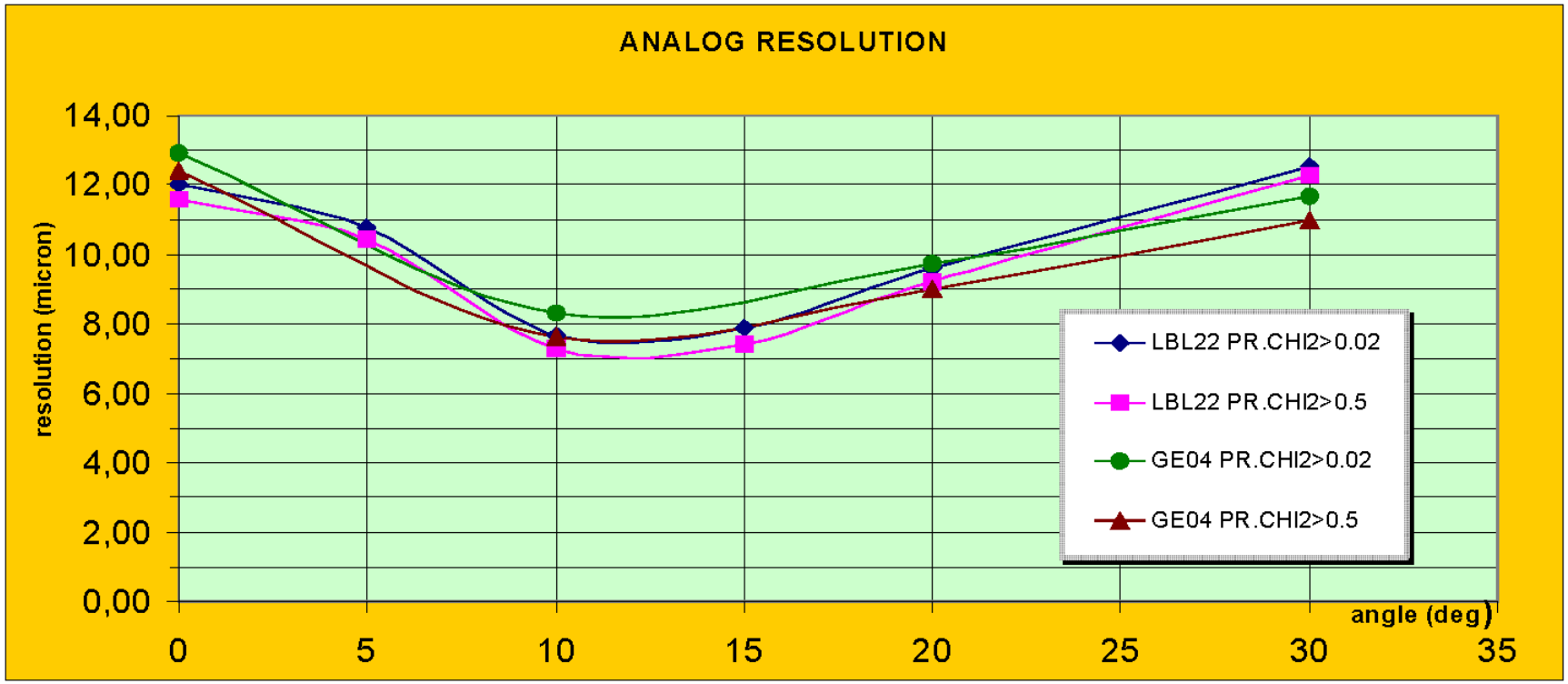
- Use dedicated high-intensity facility at CERN PS using 24 GeV protons. Able to provide roughly 10^{16} p/cm^2 over an area of about 2 cm^2 during a one week period.
- Have used this facility over a period of three years to evaluate three generations of pixel electronics for ATLAS, both single-chips and complete modules.
- All electronics operated and monitored continuously during irradiation.

Test-beam:

- A large dedicated facility for ATLAS detector testing is operated at CERN SPS, providing 180 GeV pions (and many other beams).
- Pixel test setup includes dedicated strip telescope capable of better than 5μ point resolution projected onto pixel assemblies. A superconducting dipole provided a 1.5T magnetic field to evaluate Lorentz angle effects.
- Have used this facility from 1997 - 2004, every year for at least several weeks, to constantly evaluate pixel prototype effort.
- Note beam is not bunched, so record the time difference between trigger particle and 40MHz clock edge used to operate pixel electronics. In following, many plots are made as a function of this ΔT measurement to explore timing performance.

Study position resolution versus angle and algorithm:

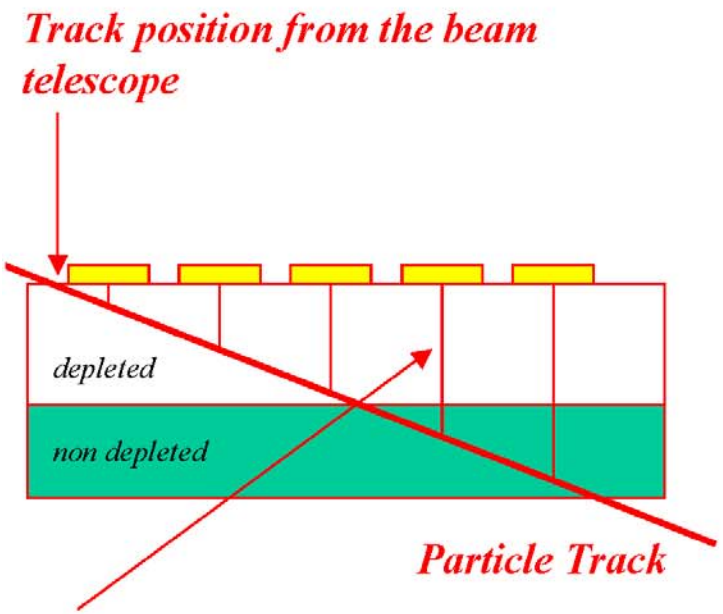
- Effective angle of incidence, including tilt angle and Lorentz angle, varies from about 10 degrees (pre-rad) to about 18 degrees (post-rad) for radial tracks.
- Can use simple digital algorithm for position, where the center of the cluster of hits is chosen. This gives a ϕ resolution of 12-14μ over a wide range of incident angles.
- Improved algorithm uses charge information to compute center of cluster. In this case, get improved resolution in region relevant to radial tracks of 8-9μ.

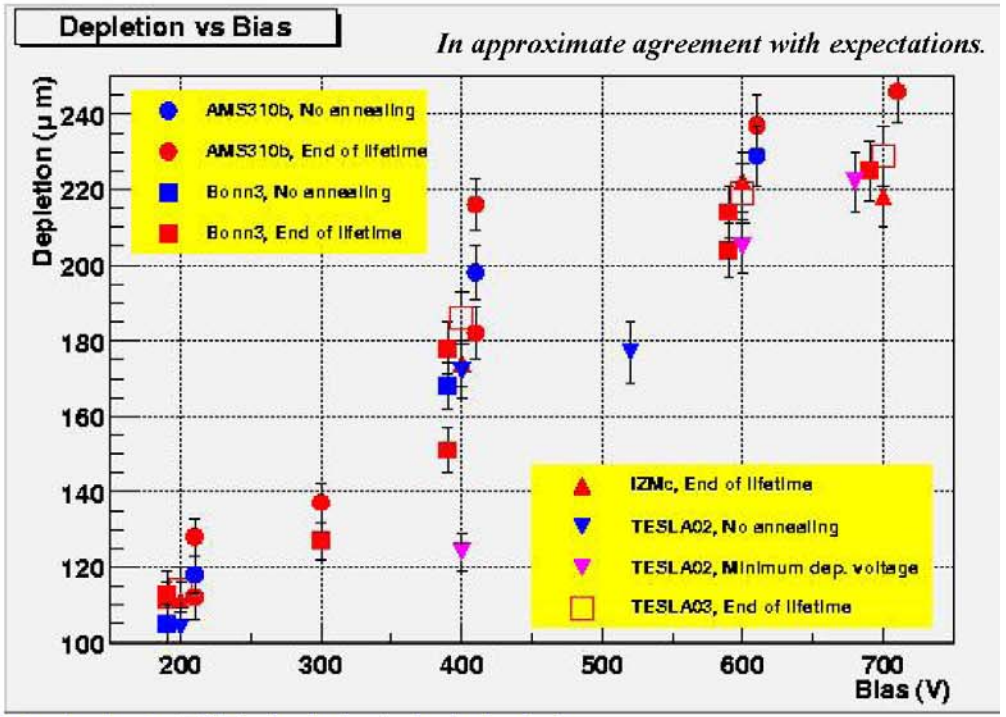


- Plot is for un-irradiated modules. Similar performance can be achieved with irradiated modules, but this requires use of “digital timewalk correction”.

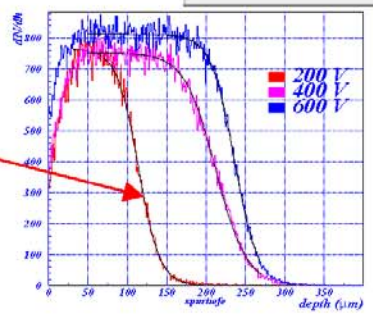
Study depletion depth for irradiated sensors:

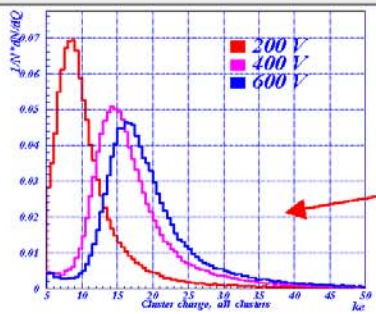
- Old measurements with first irradiated sensor studies using FE-I1. Use track depth to estimate depletion depth of the sensor:





The maximum track segment depth gives the depleted depth



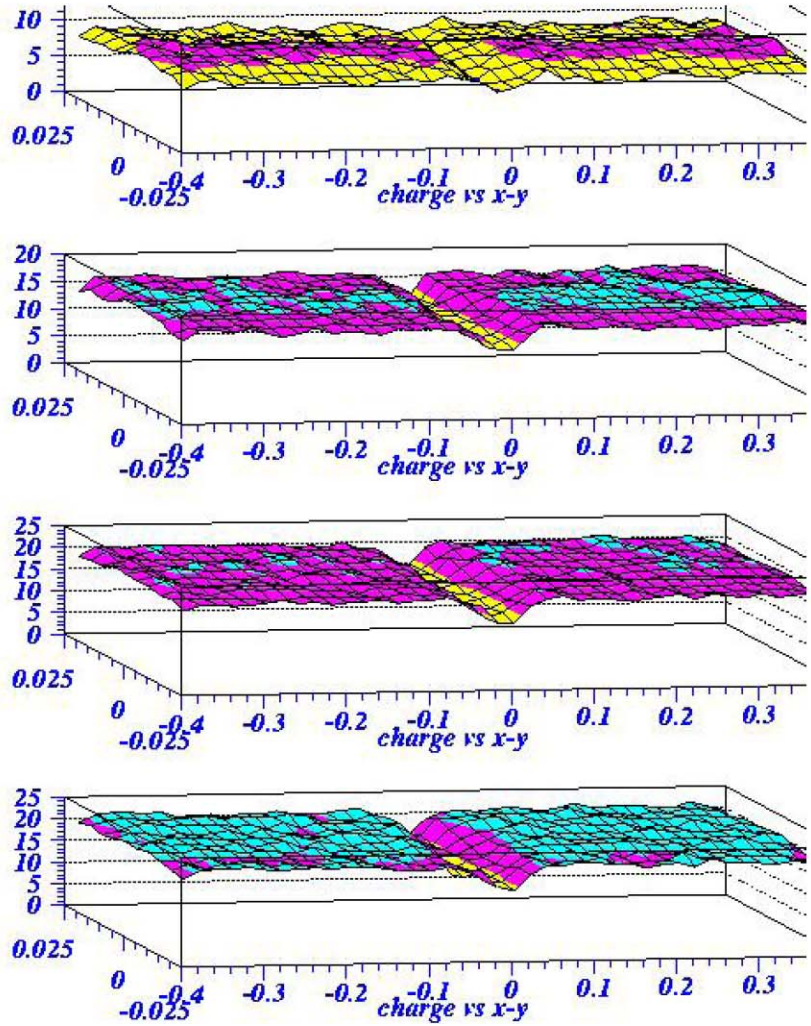


Charge

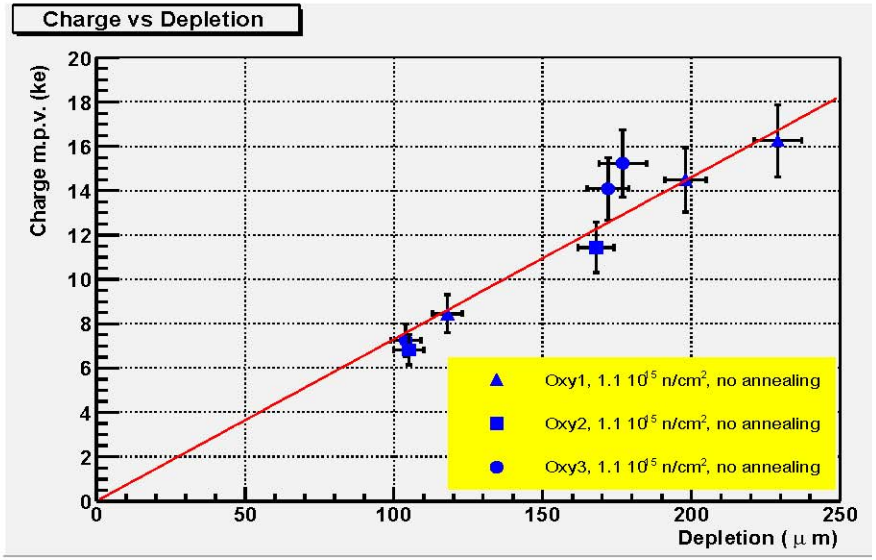
- Observe close to full depletion (250-280μ) for bias voltage of 600-700V.

Examine charge collection in irradiated sensors:

- Measure charge collection uniformity and compare measured charge (most probable) to depletion depth:



Note that absolute charge calibration is not very precise, but suggests that most probable charge after irradiation is about 13-15Ke.

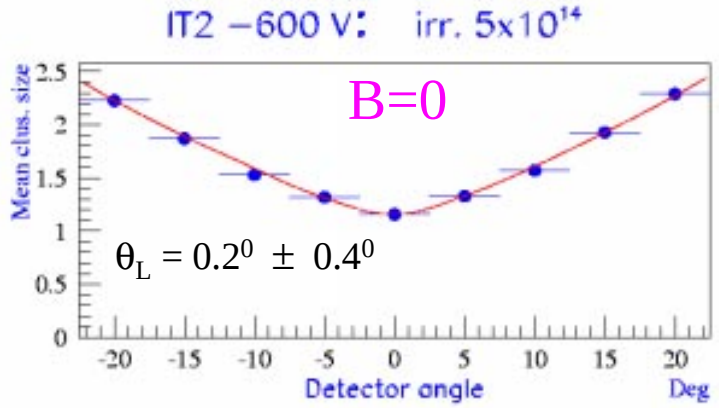


Plots on left are (top to bottom) for 200V, 400V, 600V, and 700V bias voltage.

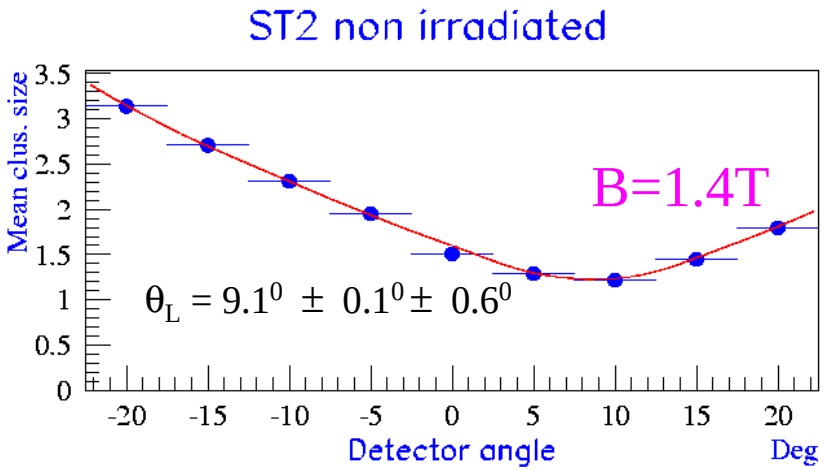
- Region with reduced charge collection, surrounding the bias dot area, is responsible for loss in in-time efficiency for irradiated sensors (average of 2%).

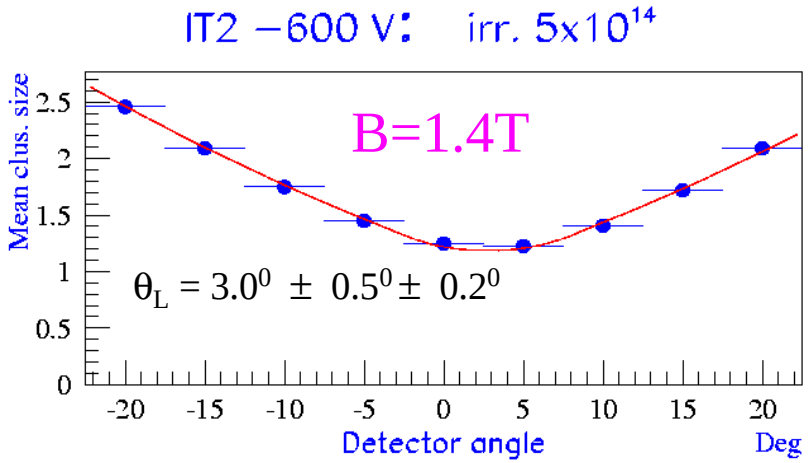
Measure Lorentz angle in sensors:

- Use cluster width versus angle of incidence, doing parallel runs with and without magnetic field, to extract angle at which cluster width is minimum:



not irradiated	**$9.1^0 \pm 0.1^0 \pm 0.6^0$**
dose 5 10^{14} n/cm²	**$3.0^0 \pm 0.5^0 \pm 0.2^0$**
dose 10^{15} n/cm²	**$3.2^0 \pm 1.2^0 \pm 0.5^0$**

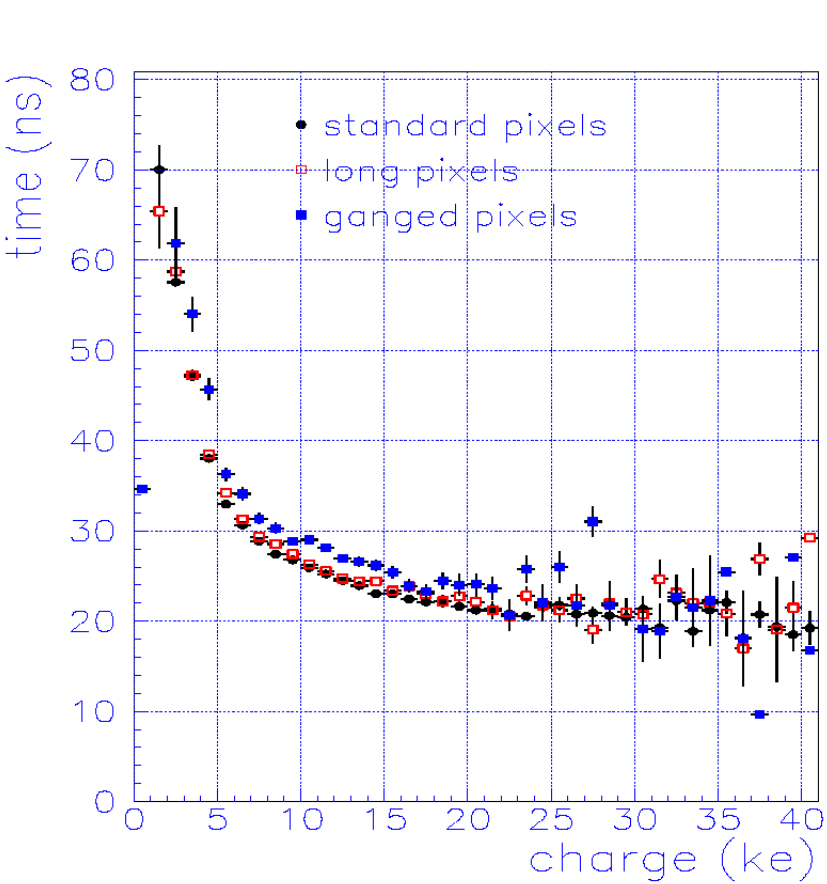


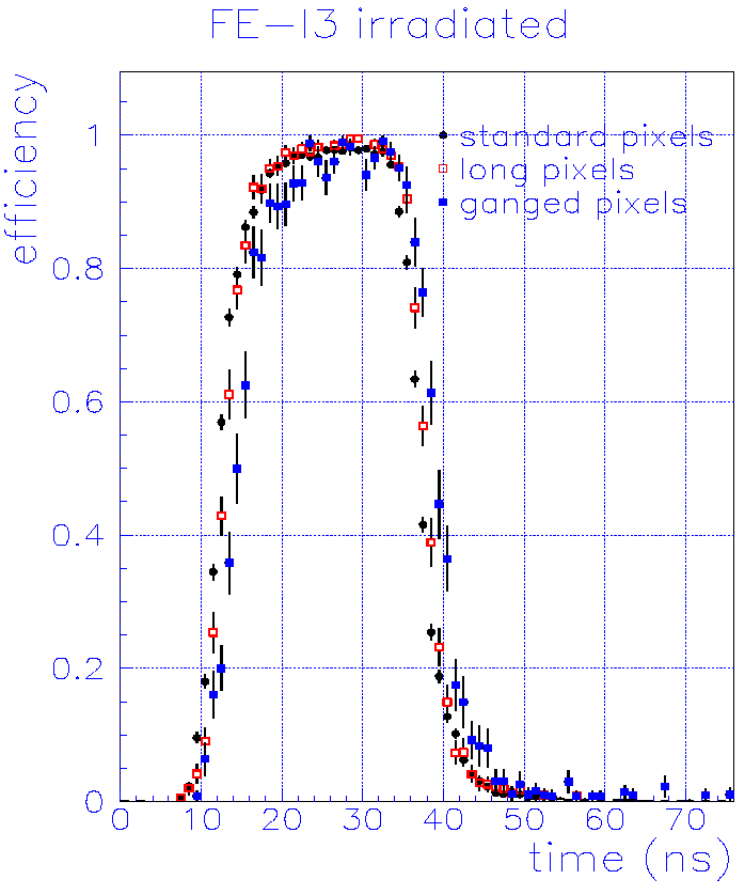


- Reduction after irradiation due to reduced mobility at higher E fields. Simple model reproduces data well. For barrel, effective angle (Tilt-Lorentz) varies from about 10 degrees (pre-rad) to about 18 degrees, implying significant charge sharing in ϕ.

Study timing performance of final production modules:

- Detailed studies of production modules, both un-irradiated and irradiated, in H8 testbeam. In-time ε=99.9% (pre-rad), ε = 98% averaged over 7 (post-rad) modules.

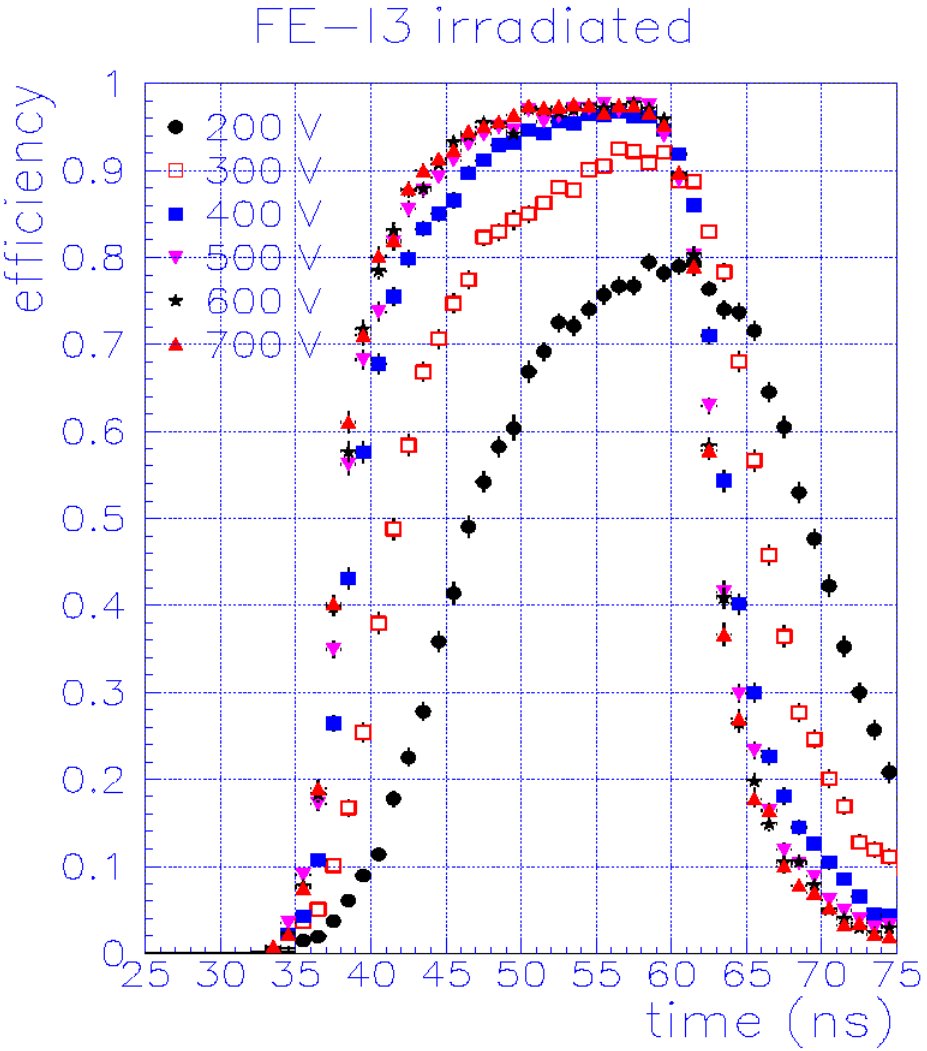




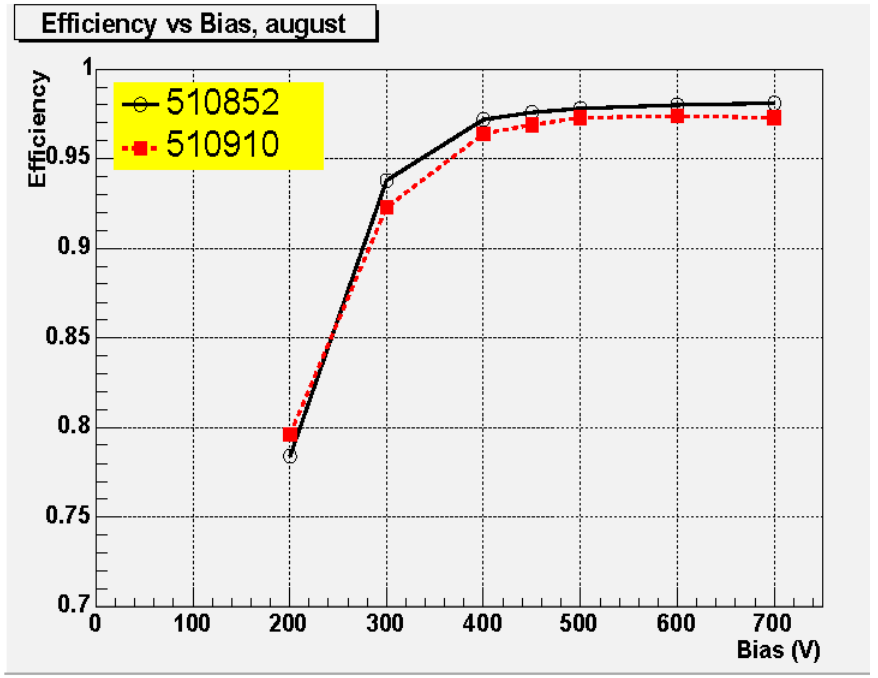
- Plot on left is timing performance versus charge for hit, showing excellent performance down to about 5Ke charge, as indicated by in-time threshold plots.
- Plot on right is in-time efficiency for different pixel types, showing uniform results, and efficiency plateau of about 10ns width. All pixel types behave well.

Study irradiated sensor performance versus bias voltage:

- Left plot shows efficiency versus timing for different sensor bias voltages for irradiated module. Width of timing plateau is about 8ns above 500V:



Full efficiency at 400-500 V

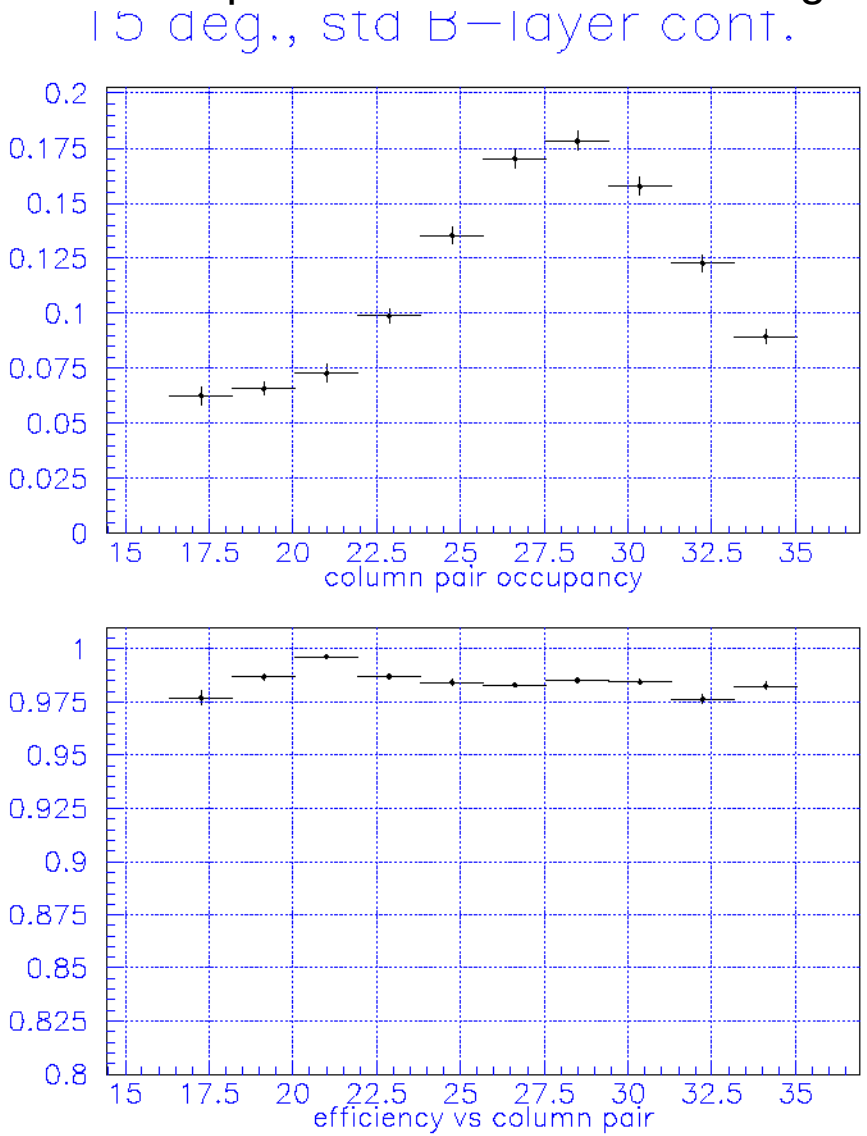


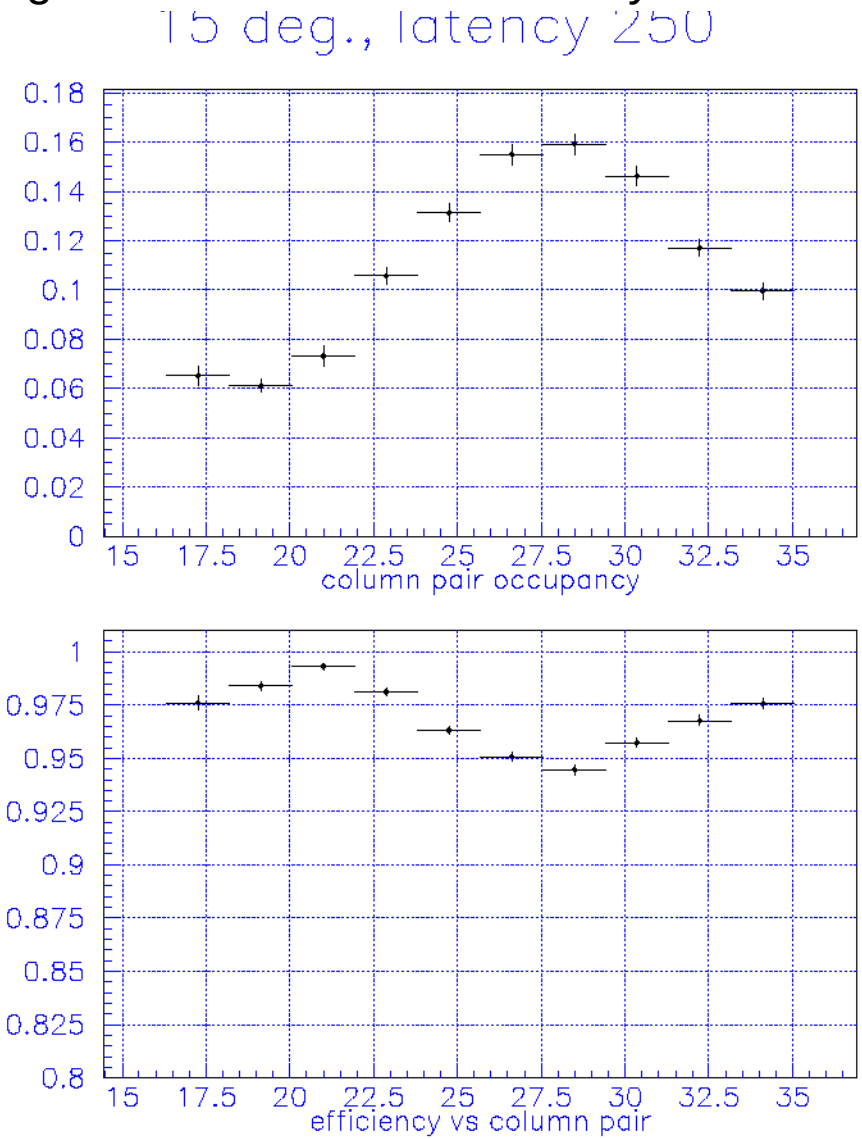
- Right plot shows in-time efficiency for irradiated module versus sensor voltage, again showing plateau at about 500V.

Study performance of modules at high intensity:

- Special beam setup with lots of concrete block shielding was prepared, in order to operate at maximum intensity. Just barely able to operate at B-layer intensity ($3x10^7/cm^2/s$) before triggering radiation protection alarms nearby.
- Study four production modules, three irradiated to lifetime dose. At low intensity, use strip telescope and trigger system to evaluate performance. At high intensity, not even small scintillators or PIN diodes were useful to monitor performance.
- All high intensity measurements were made by using four pixel modules for tracking, requiring three to provide points for track and looking at fourth module.
- As the off-module readout and DAQ was not capable of operating at high trigger rates (only several KHz), this test was really an evaluation of the readout architecture in the front-end chip, and its capability of handling high intensity.
- Various effects relevant, :
  - * Occupancy of a pixel (time required to process hit before a new hit can be accepted)
  - * Occupancy of column pair readout while transferring hits into EOC buffers at bottom of column pair
  - * Length of time hits must be stored in EOC buffers before trigger decision (latency)
  - * Occupancy of EOC buffers themselves.
- Rate variable is column pair occupancy (#hits/colpair/crossing), B-layer 0.10 - 0.15.
- Dominant effect observed to be occupancy of EOC buffers, despite the fact that there is one buffer for every 5 pixels (on average). Observe safety factor of about 1.5 - 2.0 over worst-case B-Layer occupancy estimate at LHC design luminosity.

- Lower left plot shows in-time efficiency for irradiated module at full B-layer intensity versus position in module at 15 degree angle. No reduction in efficiency seen.





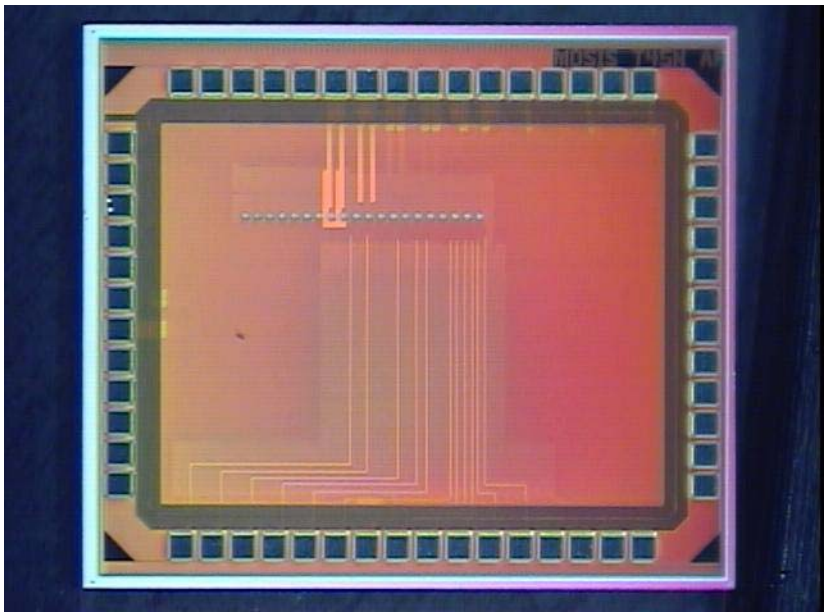
- Lower right plot shows in-time efficiency when latency (hit storage time in EOC buffers) has been doubled. Efficiency losses seen above occupancy of 0.12.

Pixel Detector Upgrade Activities at LBL

- Expect to replace innermost pixel layer (B-layer) on a timescale of 2011-2012. This layer defines impact parameter resolution for B-tagging, and is critical to ATLAS performance. Will concentrate on improvements in micro-electronics and sensors.
- Longer term CERN planning has targeted next upgrade as a factor 10 luminosity increase to 10^{35}, known as SLHC, perhaps in about 2015.

Upgrade R&D in Electronics and Sensors:

- Designed a first test chip in IBM 0.13µ CMOS technology (most advanced mixed-mode CMOS process available to us today), and submitted in May 04 via MOSIS:

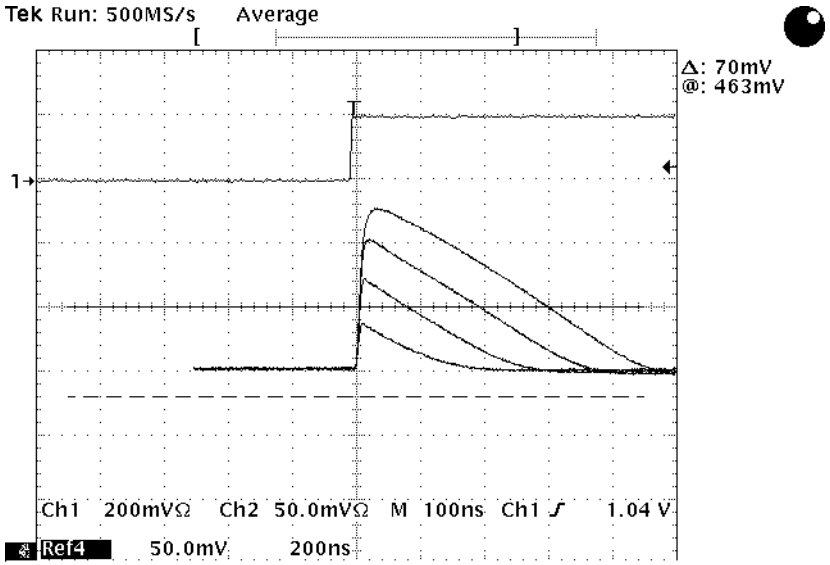


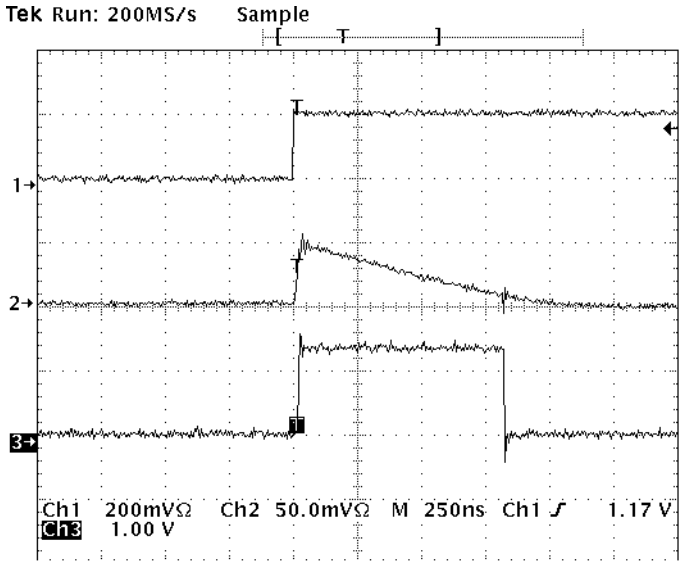
Test chip addresses two sets of issues:

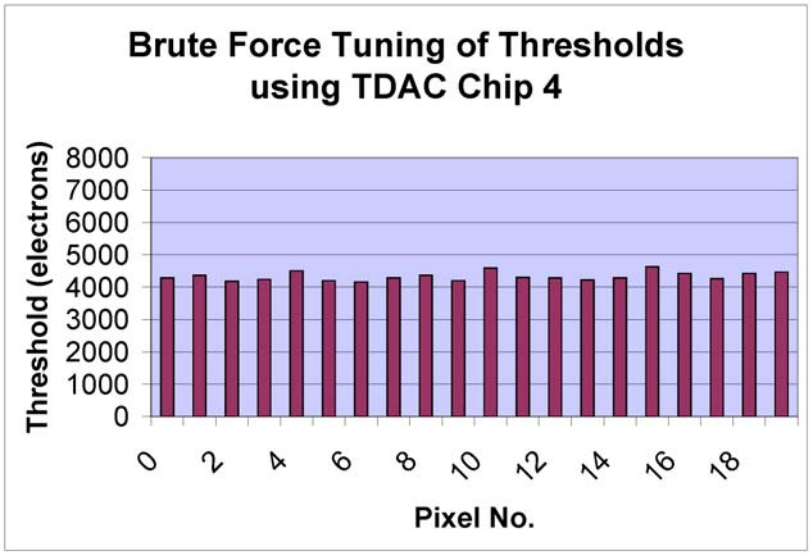
- First, will examine performance of different SEU-tolerant storage schemes.
- Second, will study agreement between simulation and measurements for pixel front-end design (preamp/discriminator) based on present FE-I3 design, to learn more about pixel analog design issues.

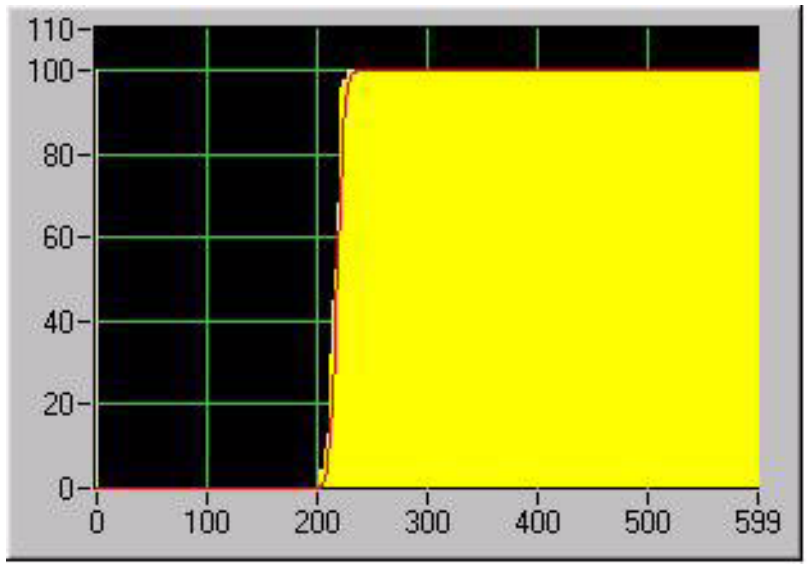
- Plan to develop improved individual building blocks over next 2-3 years, with a first full-scale engineering run for B-Layer upgrade in 2008.

- First results from 0.13µ test chip (counterclockwise from upper left):



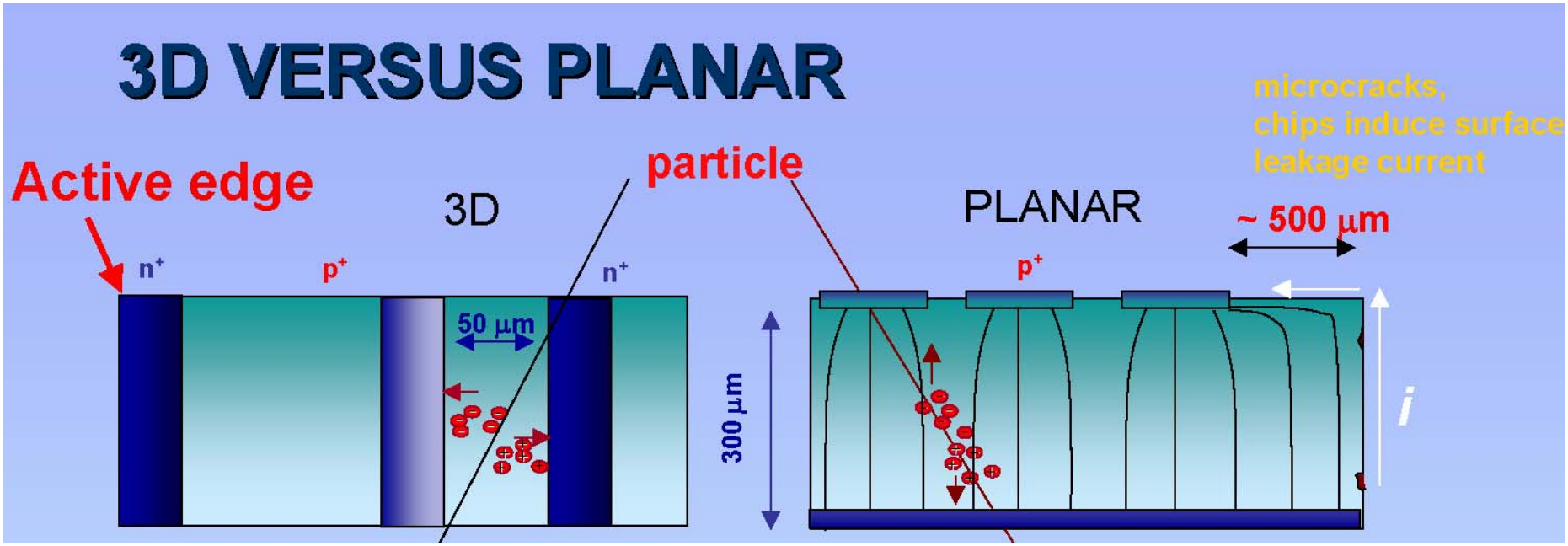




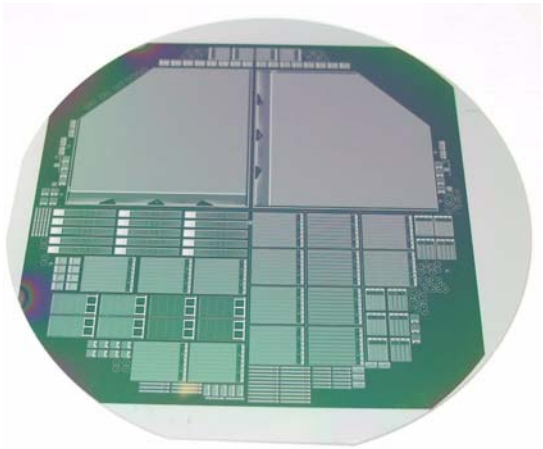


- Preamp output versus charge, preamp and discriminator output, S-curve for threshold scan of one channel, tuned thresholds for twenty pixels in test chip.

- Proceeding in collaboration with 3D sensor effort, and will evaluate performance of this novel sensor concept using current production pixel electronics.



- 3D design approach is radical departure from traditional planar silicon sensors, and has potential to provide greater radiation hardness due to short collection length.



First prototype run by C. Kenney and S. Parker at Stanford Microsystems Lab has produced prototype 3D sensors matching the existing pixel FE-I3 geometry.

Have bump-bonded several of these devices to FE-I3 single chips. Unfortunately, present sensors appear to suffer from very high defect rate, so biassing is not possible

Comments on LBL and Instrumentation Development

- Development and construction of ATLAS pixel detector involves more than 100 dedicated scientists and engineers from Bonn, Dortmund, Genova, Marseille, Milano, Prague, Siegen, Udine, Wuppertal, as well as New Mexico, Ohio, Oklahoma, and of course LBL.
- After spending more than 10 years on the development of the ATLAS pixel tracker, with LBL playing a leading intellectual role in most areas, offer reflections:
- Development of “beyond state-of-the-art” instrumentation relies on tightly integrated teams of scientists and engineers, something that LBL is uniquely good at.
- Pixel electronics chain required team of several IC designers plus board level designers, over 10 years, constantly following technology developments. After working this long on one problem, much specialized knowledge is developed.
- Major failure of LBL in this respect is to treat instrumentation of this type seriously at the highest levels in the lab, in order to create a strong intellectual center, and build an atmosphere to train and retain the best people in diverse technical areas.
- We achieve sporadic success, but hard to keep momentum and generate synergy across broad areas of instrumentation. Much ATLAS experience already lost.
- Success requires a certain continuity in projects and funding that is very difficult to achieve in highly project-oriented DoE environment. Lab Director can help !!!
- Convinced that this type of sophisticated instrumentation, suitably targeted at many other science communities at LBL/UCB can have a revolutionary impact.