# NERSC/LBNL UPC Compiler Status Report 

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## UPC Compiler - Status Report

$\square$ Current Status:

- UPC-to-C translator implemented in open64. Compliant with rev 1.0 of the UPC spec.
- "Translates" the GWU test suite and test programs from Intrepid.


## UPC Compiler - Future Work



## UPC Compiler - Future Work



- Integrate with GasNet and the UPC runtime
- Test runtime and translator (32/64 bit)

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- Investigate interaction between translator and optimization packages (legal C code)
-UPC specific optimizations
-Open64 code generator


## UPC Optimizations - Problems

$\square$ Shared pointer - logical tuple (addr, thread, phase)

```
    {void *addr; int thread; int phase;}
```

$\square$ Expensive pointer arithmetic and address generation

```
    p+i -> p.phase=(p.phase+i)%B
    p.thread=(p.thread+(p.phase+i)/B)%T
```

$\square$ Parallelism expressed by forall and affinity test
$\square$ Overhead of fine grained communication can become prohibitive

## Translated UPC Code


\#include <upc.h>
shared float *a, *b;
int main() \{
int i, k;
upc_forall(k=7; k <234; k++; \&a[k]) \{
upc_forall $(\mathrm{i}=0 ; \mathrm{i}<1000 ; \mathrm{i}++; 333)\{$
$\mathrm{a}[\mathrm{k}]=\mathrm{b}[\mathrm{k}+1] ;$
\}
\}
\}

```
\(\mathrm{k}=7\);
    while( \(\mathrm{k}<=233\) )
    Mreturn_temp_0 0 uper_add_shared (a.u0, 4, \(k, 1\) ):
    commal = uper_threadof_shared(Mretum_temp_0);
    if(MYTHREAD \(==\) commal)
    \{
        \(\mathrm{i}=0\);
    while (i <= 999)
    \{ Mreturn_lemp_2 = uper_add
        Mreturn temp \(1=\) uper ate \(\operatorname{shared}(b, u 0,4, k+1,1)\) :
        _comma \(=\) uper_get_nb_shared_float(Mreturn_temp_1,0).
        comma0 \(=\) uper_wait_syncnb_valget_float(__comma);
        uper_put_nb_shared_float(Mreturn_temp_2, 0, __comma0)
        _3:;
        \(\mathrm{i}=\mathrm{i}+1\);
\(\frac{\text { ! }}{\frac{1}{2}}\)
    \(\mathrm{k}=\mathrm{k}+1\);
\}
```


## UPC Optimizations

- "Generic" scalar and loop optimizations (unrolling, pipelining...)
$\square$ Address generation optimizations
- Eliminate run-time tests
- Table lookup / Basis vectors
- Simplify pointer/address arithmetic
- Address components reuse
- Localization
$\square$ Communication optimizations
- Vectorization
- Message combination
- Message pipelining
- Prefetching for irregular data accesses


## Run-Time Test Elimination

$\square$ Problem - find sequence of local memory locations that processor $P$ accesses during the computation
$\square$ Well explored in the context of HPF
$\square$ Several techniques proposed for for block-cyclic distributions:

- table lookup (Chatterjee,Kennedy)
- basis vectors (Ramanujam, Thirumalai)
$\square$ UPC layouts: cyclic, pure block, indefinite block size - particular case of block cyclic


## Table Array Address Lookup

```
upc_forall(i=l; i<u; i+=s; &a[i])
    a[i] = EXP();
```

i=1;
while(i<u) \{

if (MYTHREAD =a comma1) 1 (
t_2 = upcr_add_shared (a.u0, 4, i, 1);
upcr_put_shared_float (t_2, 0, EXP ()) ;
翟
_1:
i+= s;
\}

```
compute T, next, start
base = startmem;
i = startoffset;
while (base < endmem) {
    *base = EXP();
    base += T[i];
    i = next[i];
}
```

Table based lookup （Kennedy）

## Array Address Lookup

$\square$ Encouraging results - speedups between 50:200 versus run-time resolution
$\square$ Lookup - time vs space tradeoff . Kennedy introduces a demand-driven technique
$\square$ UPC arrays - simpler than HPF arrays
$\square$ UPC language restrictions - no aliasing between pointers with different block sizes
$\square$ Existing HPF techniques also applicable to UPC pointer based programs

## Address Arithmetic Simplification

- Address Components Reuse
- Idea - view shared pointers as three separate components (A, T, P) : (addr, thread, phase)
- Exploit the implicit reuse of the thread and phase fields
- Pointer Localization
- Determine which accesses can be performed using local pointers
- Optimize for indefinite block size
- Requires heap analysis/LQI and a similar dependency analysis to the lookup techniques


## Communication Optimizations

$\square$ Message Vectorization - hoist and prefetch an array slice.
$\square$ Message Combination - combine messages with the same target processor into a larger message
$\square$ Communication Pipelining - separate the initiation of a communication operation by its completion and overlap communication and computation

## Communication Optimizations

$\square$ Some optimizations are complementary
$\square$ Choi\&Snyder (Paragon/T3D -PVM/shmem), Krishnamurthy (См5), Chakrabarti (SP2/Now)
$\square$ Speedups in the range 10\%-40\%
$\square$ Optimizations more effective for high latency transport layers (PVM/Now) ~ 25\% speedup vs 10\% speedup (shmem/SP2)

## Prefetching of Irregular Data Accesses

$\square$ For serial programs - hide cache latency
$\square$ "Simpler" for parallel programs - hide communication latency
$\square$ Irregular data accesses

- Array based programs : a [b[i]]
- Irregular data structures (pointer based)


## Prefetching of Irregular Data Accesses

$\square$ Array based programs

- Well explored topic ("inspector-executor" - Saltz)
$\square$ Irregular data structures
- Not very well explored in the context of SPMD programs.
- Serial techniques: jump pointers, linearization (Mowry)
- Is there a good case for it?


## Conclusions

$\square$ We start with a clean slate
$\square$ Infrastructure for pointer analysis, array dependency analysis already in open64
$\square$ Communication optimizations and address calculation optimizations share common analyses
$\square$ Address calculation optimizations are likely to offer better performance improvements at this stage

The End

## Address Arithmetic Simplification

$\square$ Address Components Reuse

- Idea - view shared pointers as three separate components (A, T, P) : (addr, thread, phase)
- Exploit the implicit reuse of the thread and phase fields

```
    shared [B] float a[N],b[N]
upc_forall(i=l;i<u;i+=s;&a[i])
    a[i] = b[i+k];
```


## Address Component Reuse

| B1 | B2 | B3 | B4 | B5 | B6 |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :---: | :---: | :---: |
| P0 |  |  |  |  | P1 |  |  |  |
|  |  |  |  |  |  |  |  |  |

$$
\begin{aligned}
& \mathrm{B}_{\mathrm{i}} \\
& \text { a[i] }=\mathrm{b}[\mathrm{i}+\mathrm{k}] ; \\
& a->\left(A_{a}, T_{a}, P_{a}\right) \\
& b->\left(A_{b}, T_{b}, P_{b}\right) \\
& \mathrm{T}_{\mathrm{a}}=\mathrm{T}_{\mathrm{b}} \\
& \mathrm{P}_{\mathrm{b}}=\mathrm{P}_{\mathrm{a}}+\mathrm{k}
\end{aligned}
$$

## Address Component Reuse

```
Ta = 0;
for (i=first_block; i<last_block; i=next_block) {
    for(j=bi,Pa=0; j < ei-k; j++,Pa++)
        put(Aa,Ta,Pa, get(Ab,Ta,Pa+k));
    for(; j<ei; j++)
        put(Aa,Ta,Pa, get(Ab,Ta+1,Pa-j));
}
```

