E835 Data Acquisition (Run 1999/2000)

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1.0 Introduction

This memo describes the E835 Data Acquisition system. It shows a layout of the crates and the organization of the hardware.

Fig.1 shows the E835 Data Acquisition system. It utilizes three SGI computers and one Motorola MVME167 processor. The computers are: an Indy (fn835x) for the Run Control, Data Acquisition Monitor Program (DAMP) and to talk to the CAMAC branches; a Challenge-L (fn835y) with four 150 MHz processors for the event building, filtering and logging; and an Indigo (fn835z) for detector monitoring and Event Display.

Data from the detectors are read out by FERA ADC (LRS4300) and TDC (LRS3377) and PCOS Latches (LRS2731). All modules transfer the data through their front ECL-ports to Damn Yankee Conrollers (DYCs). The DYCs can store the data in their FIFOs before they send them out to two pairs of Access Dynamics DC2/DM115s. Each DC2 receives the data of a group of DYCs connected in daisy-chain via a DART cable. The DC2 writes the data it receives to a Dual Ported Memory (DPM) via the VSBus of the VME crate. A 32-bit word is reserved in the beginning of each event for a header. The DC2 writes this word when it receives an End-Of-Event (EOE) from the last DYC in the chain. The header contains an event count (upper 4 bytes) and an inclusive word count in bytes (lower 4 bytes). When the event count reaches 0xffff it is reset to 0x0. The DC2 uses the “ping-pong” algorithm to fill the DPMs. According to this algorithm the DC2 writes the “ping” memory with exactly N events before it switches to the “pong” memory. The number of events N is kept in the experiment’s configuration database. A process running on the Challenge, called “gateway”, reads the data from the “ping” memory while the DC2 writes to the “pong” memory. When all the data from “ping” have been read, the gateway allows the DC2 to write to “ping” and then switches to read out the “pong”. Both processes are polling to see if the other has finished using a DPM. The communication between the DC2 and the “gateway” is done using a third DPM as a mailbox. This way neither the DC2 nor the gateway interrupt the data transfers of the other while they are polling for a DPM. The format of the DDD buffers (DDD from the three initials of DC2/DM115/DPM) is shown in fig.2. Each DDD buffer has N consecutive sub-events. Each sub-event consists of the data of the DYCs that are on its DART cable.

FIGURE 1. E835 Data Acquisition System.

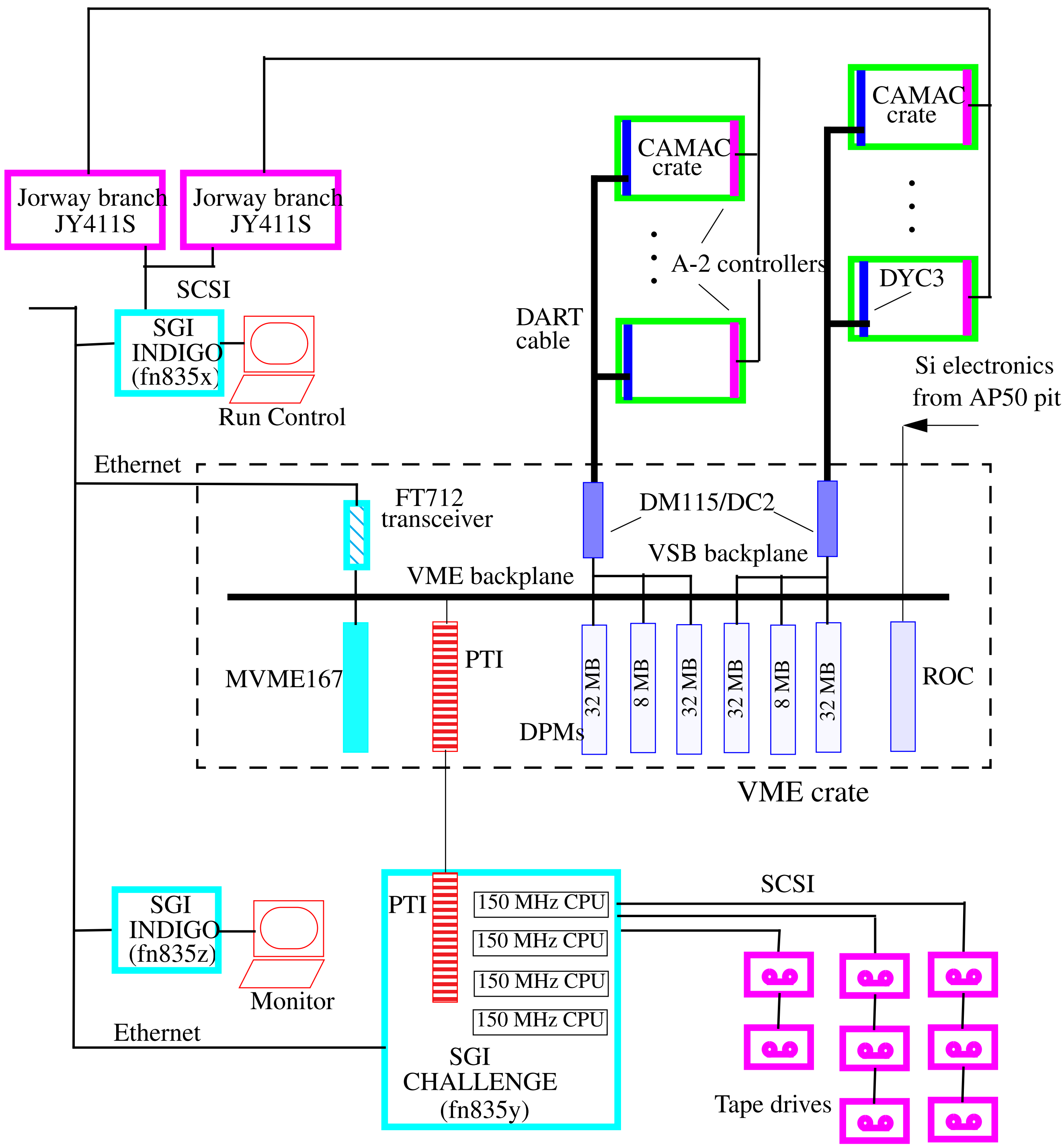
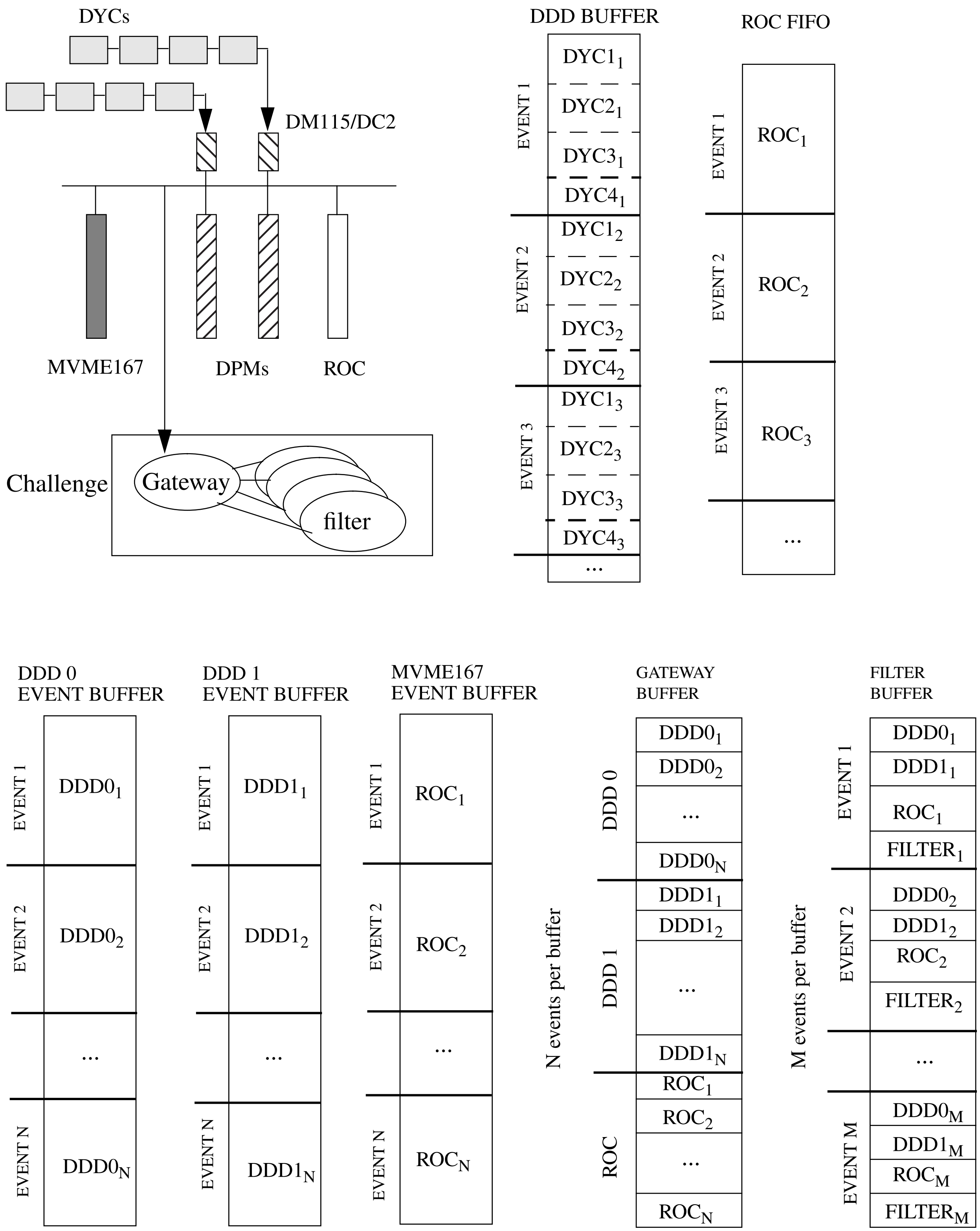


FIGURE 2. Event Building scheme.



2.0 Hardware triggers

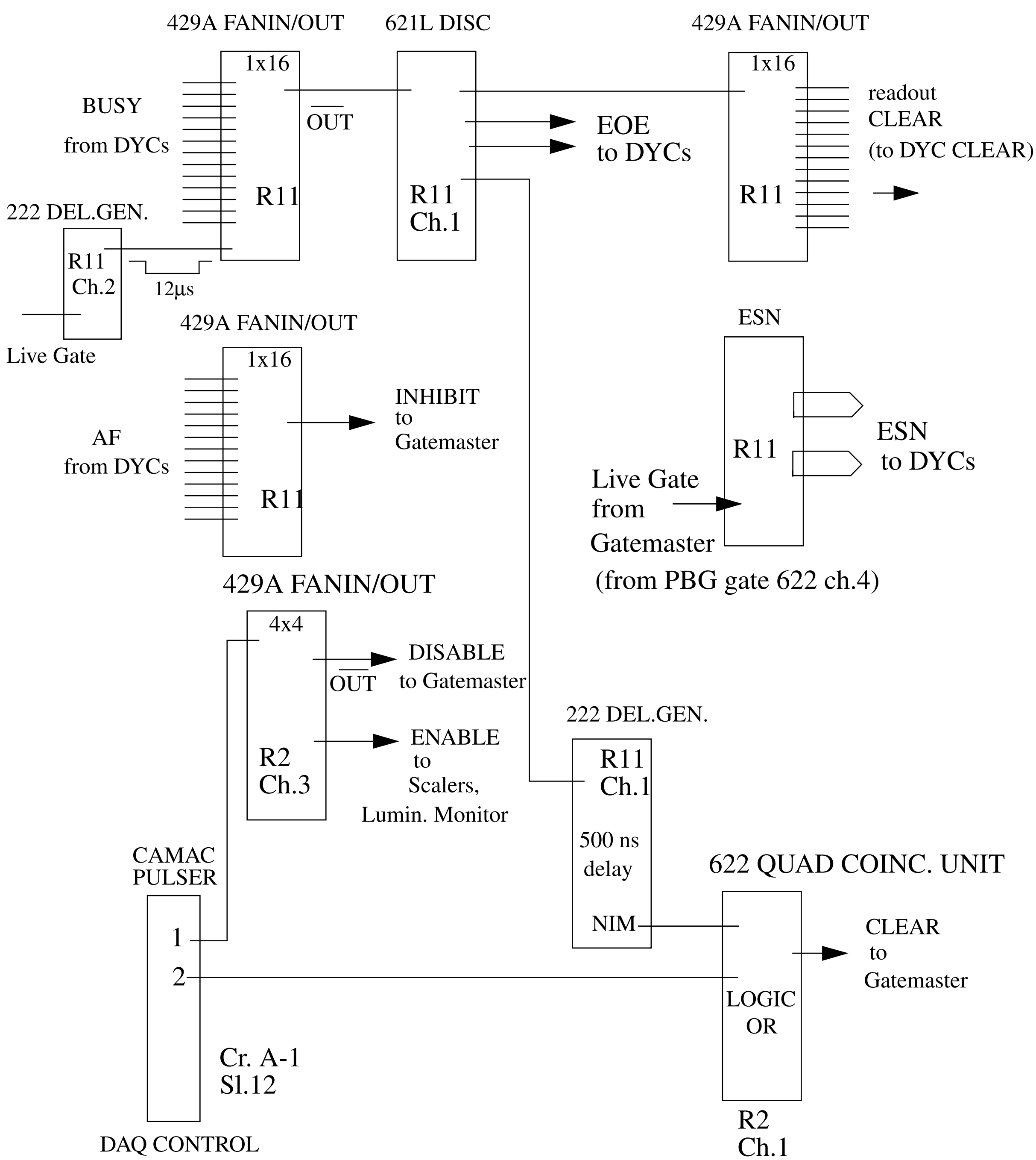
The hardware triggers are ORed in the Gatemaster module to form the gates to the electronics of the experiment. A 16-bit trigger word is read by a TDC and defines the hardware trigger. The assignment of the inputs to the Gatemaster is the following:

GATEMASTER INPUT	MEANING
1	E+E-
2	PI+PI-
3	PHI-PHI
4	GAMMA-GAMMA
5	ETOT>80%
6	PbarP CONTROL
7	NEUTRAL EFFICIENCY (ETOT NO VETO)
8	ETOT>70%
9	PB-G LASER PULSER
10	Si STROBE
11	
12	MINIMUM BIAS
13	TEST / PEDESTAL PULSER
14	FCAL COSMIC TRIGGER
15	CHARGED EFFICIENCY
16	

All triggers contain data from all the crates. The data from the Silicon Barrel detector are irrelevant in the case of neutral triggers.

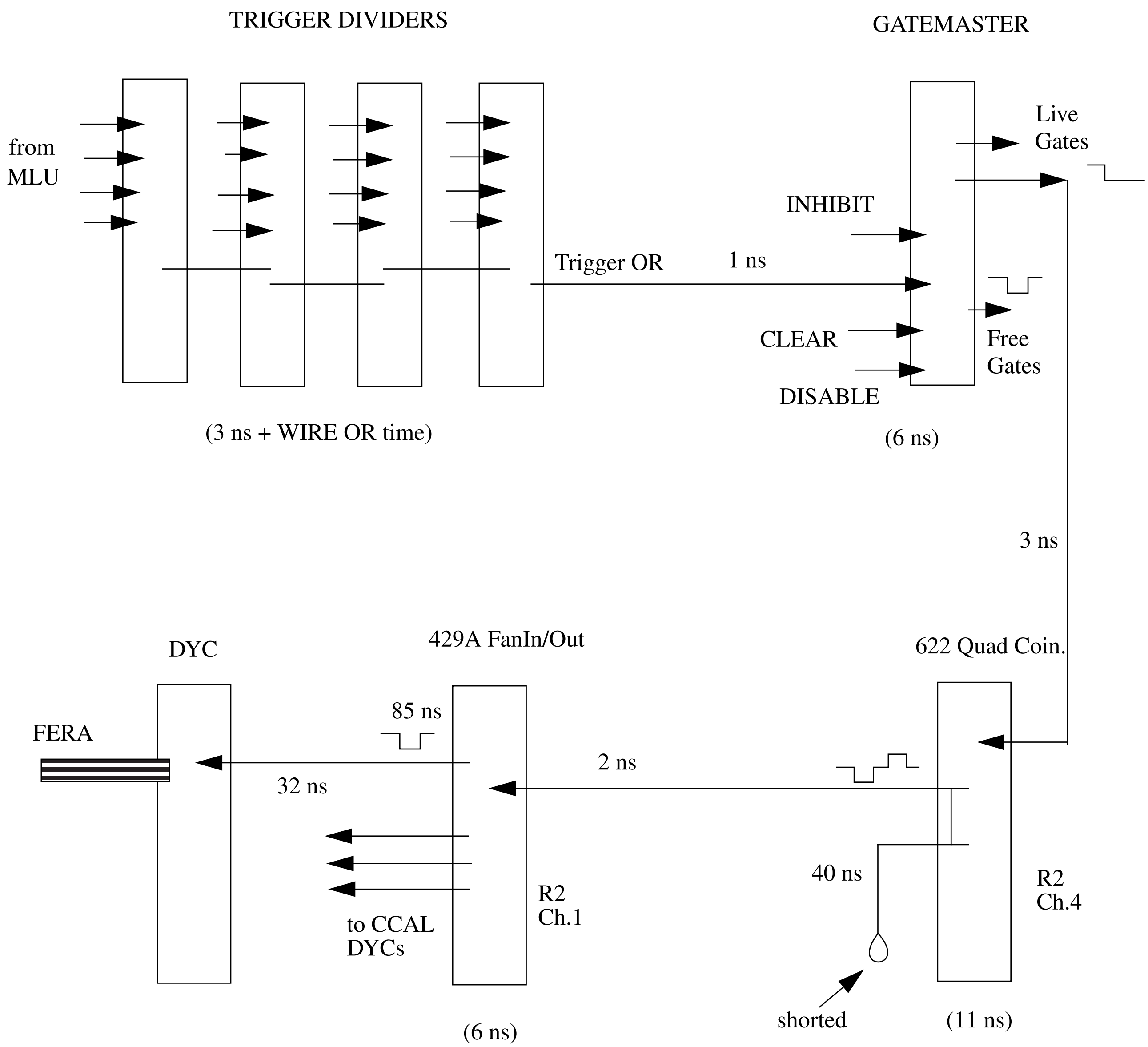
The Gatemaster - DYC logic is shown in Fig 3. The Trigger OR and the gate formation is shown in Fig.4.

FIGURE 3. GATEMASTER and DYC connections



Rxx refers to the rack where the module resides, Ch. to the channel used. For camac modules the crate number (Cr.) and slot (Sl.) are given.

FIGURE 4. TRIGGER OR and CCAL Gate



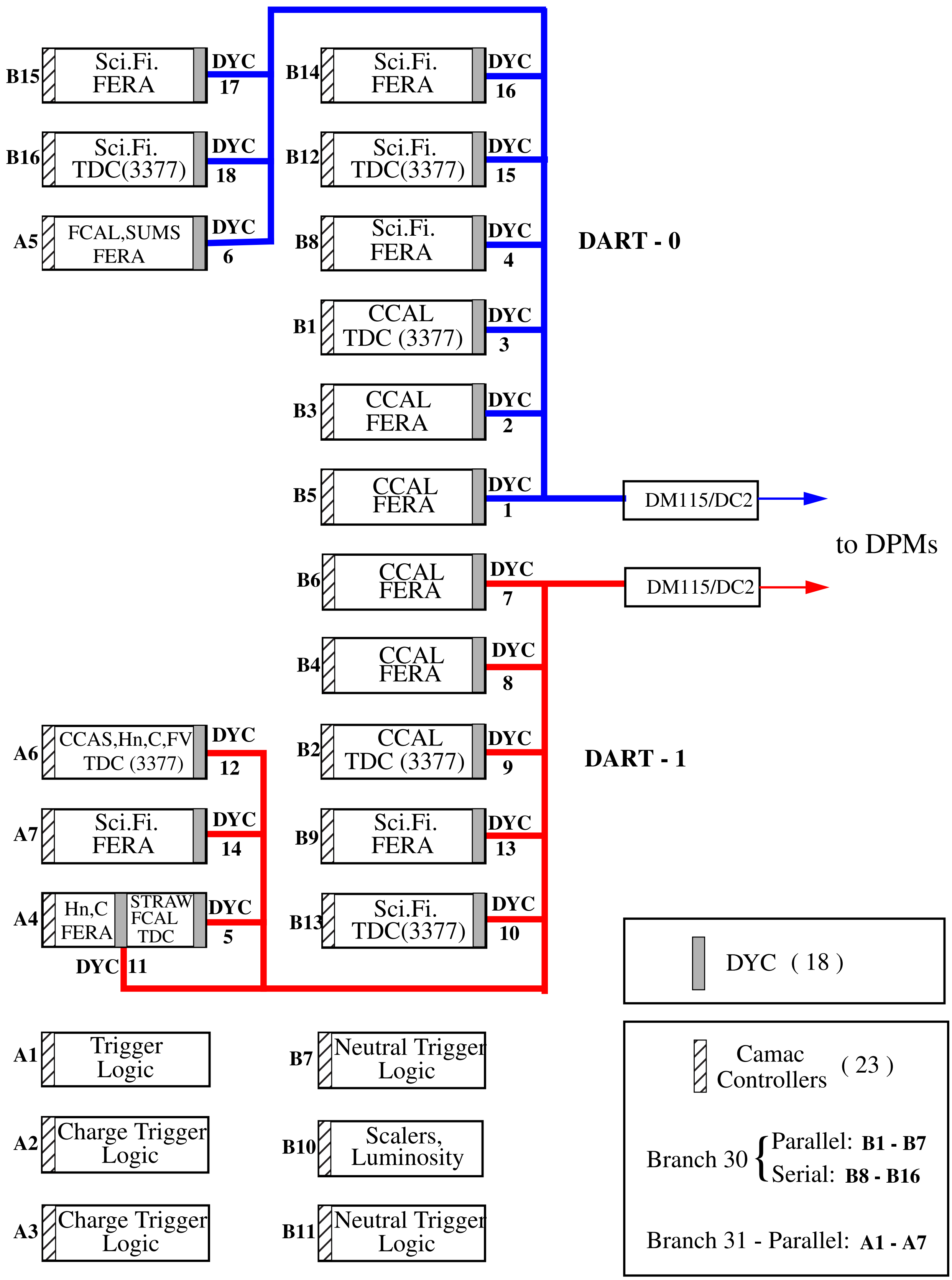
For INHIBIT, CLEAR and DISABLE signals see previous page. The Live Gate output of the Gatemaster is a level that stays on for as long as the readout of the electronics is in progress and it can be used to define the Dead Time. The Trigger Dividers and the Gatemaster are CAMAC modules, residing in crate A-1, slots 6-11. The delays of the Trigger Divider and the Gatemaster are 3 ns and 6 ns correspondingly. The formation and timing of the gate to the CCAL DYCs is shown as an example. The cable used to set the gate is 40 ns and the actual width of the gate is 85 ns. The total time from the Trigger Dividers to the DYC is 64 ns assuming zero delay for the wires of the Trigger OR.

3.0 CAMAC crates

E835 utilizes a total of 19 crates. The crates are addressed by the SGI Indy computer through two SCSI 411 Jorway Interfaces. They are arranged in 3 CAMAC branches, two parallel and one serial. One of the two Jorways (branch #30) drives both a parallel (B1-B7) and a serial (B8-B10) branch, while the other (branch #31) drives the second parallel (A1-A7). Crates with numbers greater than 7 belong to the serial branch. The PCOS crate does not belong to any branch and they are controlled by a LeCroy 4299 Databus Interface. The data from various systems are read out by 14 Damn Yankee Controllers (DYC) residing on the CAMAC crates. The DYCs are arranged in two groups, forming two data streams (Fig.4). The DYCs of each stream feed their data to a “DART cable” which is connected to a DM115 at the back of the VME crate. The two “DART cables”, each consisting of a 25-pair and a 17-pair twist and flat cables, are labeled as *DDD-0* and *DDD-1*, corresponding to the two DDDs.
The hardware is organized as follows:

#	CAMAC CRATE	BRANCH NUMBER	DYC NUMBER	DDD	CONTAINS MODULES
1	A-1	31			MLU, GATEMASTER, TRIGGER LOGIC
2	A-2	31			CHARGED LOGIC
3	A-3	31			PHI-PHI TRIGGER LOGIC
4	A-4	31	5	0	STRAW, FCAL TDC
			11	1	H1, H2, H2’, C, FCV FERA
5	A-5	31	6	0	FCAL FERA, PB-G SUM FERA
6	A-6	31	12	1	TRIGGER, H1, H2, H2’, C, PB-G SUM TDC
7	A-7	31	14	1	SCI-FI FERA
8	B-1	30	3	0	PB-G TDC
9	B-2	30	9	1	PB-G TDC
10	B-3	30	2	0	PB-G FERA
11	B-4	30	8	1	PB-G FERA
12	B-5	30	1	0	PB-G FERA
13	B-6	30	7	1	PB-G FERA
14	B-7	30			NEUTRAL LOGIC
15	B-8	30	4	0	SCI-FI FERA
16	B-9	30	13	1	SCI-FI FERA
17	B-10	30			LUMIN.MON. ADC, SCALERS
18	B-11	30			NEUTRAL LOGIC
19	B-12	30	15	0	SCI-FI TDC
20	B-13	30	10	1	SCI-FI TDC
21	B-14	30	16	0	SCI-FI FERA
22	B-15	30	17	0	SCI-FI FERA
23	B-16	30	18	0	SCI-FI TDC

FIGURE 5. CAMAC crate layout



3.1 Organization of PB-G FERA data

Crate B-3, DYC-2

FERA	VSN	BLOCKS
1	1	wedges 1-16, ring 1
2	5	wedges 1-16, ring 2
3	9	wedges 1-16, ring 3
...	...	
20	77	wedges 1-16, ring 20

Crate B-4, DYC-8

FERA	VSN	BLOCKS
1	2	wedges 17-32, ring 1
2	6	wedges 17-32, ring 2
3	10	wedges 17-32, ring 3
...	...	
20	78	wedges 17-32, ring 20

Crate B-5, DYC-1

FERA	VSN	BLOCKS
1	3	wedges 33-48, ring 1
2	7	wedges 33-48, ring 2
3	11	wedges 33-48, ring 3
...	...	
20	79	wedges 33-48, ring 20

Crate B-6, DYC-7

FERA	VSN	BLOCKS
1	4	wedges 49-64, ring 1
2	8	wedges 49-64, ring 2
3	12	wedges 49-64, ring 3
...	...	
20	80	wedges 49-64, ring 20

The unpacking of the FERA words is described in the 4300B FERA manual. All FERA data will be read out in the “zero suppressed” mode.

3.2 Organization of PB-G TDC data

Crate B-1, DYC-3

TDC	VSN	BLOCKS
1	1	wedges 1-32, ring 1
2	3	wedges 1-32, ring 2
3	5	wedges 1-32, ring 3
...	...	
20	39	wedges 1-32, ring 20

Crate B-2, DYC-9

TDC	VSN	BLOCKS
1	2	wedges 33-64, ring 1
2	4	wedges 33-64, ring 2
3	6	wedges 33-64, ring 3
...	...	
20	40	wedges 33-64, ring 20

The unpacking of the TDC words is described in the LeCroy 3377 TDC manual. All TDC data will be read out in the "zero suppressed" mode.

3.3 Organization of FCAL and PB-G SUM FERA data

Crate A-5, DYC-6

FERA	VSN	CHANNELS			
1	81	fcal 1-16			
2	82	fcal 17-32			
3	83	fcal 33-48			
4	84	fcal 49-64			
5	85	fcal 65-80			
6	86	fcal 81-96			
7	87	fcal 97-112			
8	88	fcal 113-128			
9	89	fcal 129-144			
10	90	fcal sums A-F (6 channels only)			
11	91	pb-g sum:	chan0	wedges 1-9,	rings 1-4
			chan1	wedges 9-17,	rings 1-4
			chan2	wedges 17-25,	rings 1-4
			.....		
			chan7	wedges 57-64,1,	rings 1-4
			chan8	wedges 1-9,	rings 4-8
			.....		
			chan15	wedges 57-64,1,	rings 4-8
12	92	pb-g sum:	chan0	wedges 1-9,	rings 8-12
			.....		
			chan15	wedges 57-64,1,	rings 12-16
13	93	pb-g sum:	chan0	wedges 1-9,	rings 16-20
			.....		
			chan7	wedges 57-64,1,	rings 16-20
		monitor tubes chan???			
14	94	pb-g delayed sums corresponding to VSN 91			
15	95	pb-g delayed sums corresponding to VSN 92			
16	96	pb-g delayed sums corresponding to VSN 93 (8 channels)			
17	97	pb-g Ring summers			
18	98	pg-g Ring summers and ETOT			

The unpacking of the FERA words is described in the 4300B FERA manual. All FERA data will be read out in the “zero suppressed” mode. The gate to the FCAL FERAs is sent by the DYC, while the gate to the CCAL summers is sent by a 4301 FERA driver.

3.4 Organization of MINIMUM BIAS, COUNTERS and TRIGGER TDC data

Crate A-6, DYC-12

TDC	VSN	CHANNELS
1	41	chan0-15 gatemaster inputs (see page 3 for definitions)
		chan16-31 CMLU inputs
2	42	chan0-15 SciFi bundles 3-7,9-19
		chan16-18 SciFi bundles 1,2,8, chan19-31 ϕMLU inputs
3	43	chan0-15 Ring Sum1,1-16
		chan16-23 SR5,SW1-8, chan24-27 Ring Sum2,17-20
4	44	chan0-7 SR1,SW1-8, chan8-15 SR2,W1-8
		chan16-23 SR3,SW1-8, chan24-31 SR4,W1-8
5	45	chan0-15 MMLU 0-15, chan16-31 NMLU 0-15
6	46	chan 0-7 H1 counters (1-8), chan 8-15 Veto counters (1-8)
		chan16-31 CER counters (1-8 downstream, 9-16 upstream)
7	47	chan0-31 H2 counters (1-32)
8	48	chan0-11 H2’ counters (1-12), chan16-27 H2’ counters (13-24)
9	49	chan0-15 MinBias 001-016, chan16-31 MinBias 017-032
10	50	chan0-15 MinBias 033-048, chan16-31 MinBias 049-064
11	51	chan0-15 MinBias 065-080, chan16-31 MinBias 081-096
12	52	chan0-15 MinBias 097-112, chan16-31 MinBias 113-128
13	53	chan0-15 MinBias 129-144, chan16-31 MinBias 145-160

The unpacking of the TDC words is described in the LeCroy 3377 TDC manual. All TDC data will be read out in the “zero suppressed” mode.
The signals to be read out by TDCs 41-45 are:

- 42 Neutral trigger signals (40 summers + 2 Etot)
- 20 Ring sums
- 19 bundles of SciFi
- H1OR, H2OR, H2’OR, 1H, 2H, 1e, 2e, H2=2, H2>=3, H2>=5, H2=3,4, SCIFI=3 OR 4, SFUP>=2, C OR, FV OR, FCAL OR, H1*H2’ OR, COPL+, CCAL RING(1-3,18-20), H2-Logic, H2+SF=7,8, KIN2B, KIN$p\bar{p}$1, KIN$p\bar{p}$2, SF(#8), SF(#2*#17) (27 signals: 16 CMLU and 11 ϕMLU)
- 16 MLU signals

3.5 Organization of STRAW and FCAL TDC data

Crate A-4, DYC-5

TDC	VSN	CHANNELS
1	60	straws inner 1-32
2	61	straws inner 33-64
3	62	straws inner 65-96
4	63	straws inner 97-128
5	64	straws outer 1-32
6	65	straws outer 33-64
7	66	straws outer 65-96
8	67	straws outer 97-128
9	70	fcal 1-32
10	71	fcal 33-64
11	72	fcal 65-96
12	73	fcal 97-128
13	74	fcal 129-144 chan 0-15

The unpacking of the TDC words is described in the LeCroy 3377 TDC manual. All TDC data will be read out in the “zero suppressed” mode.

3.6 Organization of COUNTERS FERA data

Crate A-4, DYC-11

FERA	VSN	CHANNELS
1	140	chan 0-7 H1 counters (1-8), chan 8-15 H2’ (1-8)
2	141	H2’ counters (9-24)
3	142	H2 counters (1-16)
4	143	H2 counters (17-32)
5	144	CER counters (1-8 downstream, 9-16 upstream)
6	145	chan0-7 Veto counters (1-8)

The unpacking of the FERA words is described in the 4300B FERA manual. All FERA data will be read out in the “zero suppressed” mode.

3.7 Organization of SCIntillating FIbers FERA data

Crate B-8, DYC-4

FERA	VSN	CHANNELS
1	138	
2	137	
3	136	
4	135	
5	134	
6	133	
7	132	
8	131	
9	130	
10	129	
11	128	
12	127	
13	126	
14	125	
15	124	
16	123	
17	122	
18	121	
19	120	
20	119	
21	118	

Crate B-9, DYC-13

FERA	VSN	CHANNELS
1	101	
2	102	
3	103	
4	104	
5	105	
6	106	
7	107	
8	108	
9	109	
10	110	
11	111	
12	112	
13	113	
14	114	
15	115	
16	116	
17	117	

Crate A-7, DYC-14

FERA	VSN	CHANNELS
1	151	
2	152	
3	153	
4	154	
5	155	
6	156	
7	157	
8	158	
9	159	
10	160	
11	161	
12	162	
13	163	
14	164	
15	165	
16	166	
17	167	
18	168	
19	169	
20	170	
21	171	

Crate B-14, DYC-16

FERA	VSN	CHANNELS
1	201	
2	202	
3	203	
4	204	
5	205	
6	206	
7	207	
8	208	
9	209	
10	210	
11	211	
12	212	
13	213	
14	214	

Crate B-15, DYC-17

FERA	VSN	CHANNELS
1	215	
2	216	
3	217	
4	218	
5	219	
6	220	
7	221	
8	222	
9	223	
10	224	
11	225	
12	226	
13	227	
14	228	
15	229	
16	230	
17	231	
18	232	

The unpacking of the FERA words is described in the 4300B FERA manual. All FERA data will be read out in the “zero suppressed” mode.

3.8 Organization of SCIntillating FIbers TDC data

Crate B-12, DYC-15

TDC	VSN	CHANNELS
1	75	
2	76	
3	77	
4	78	
5	79	
6	80	
7	81	
8	82	
9	83	
10	84	
11	85	
12	86	
13	87	
14	88	
15	89	
16	90	
17	91	
18	92	
19	93	
20	94	

Crate B-13, DYC-10

TDC	VSN	CHANNELS
1	95	
2	96	
3	97	
4	98	
5	99	
6	100	
7	101	
8	102	
9	103	
10	104	
11	105	

Crate B-16, DYC-18

TDC	VSN	CHANNELS
1	105	
2	106	
3	107	
4	108	
5	109	
6	110	
7	111	
8	112	
9	113	
10	114	
11	115	
12	116	
13	117	
14	118	
15	119	
16	120	
17	121	